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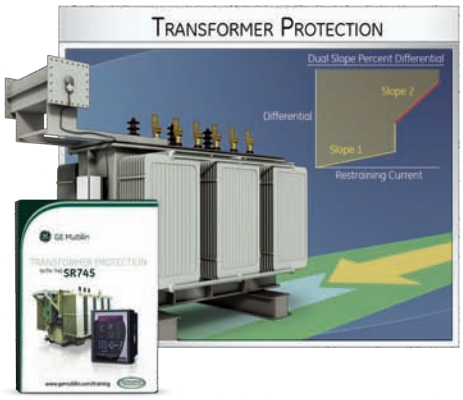

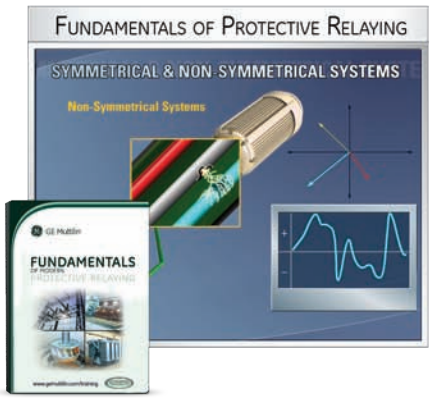

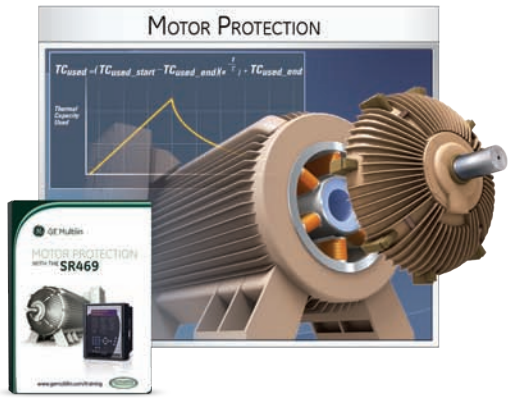

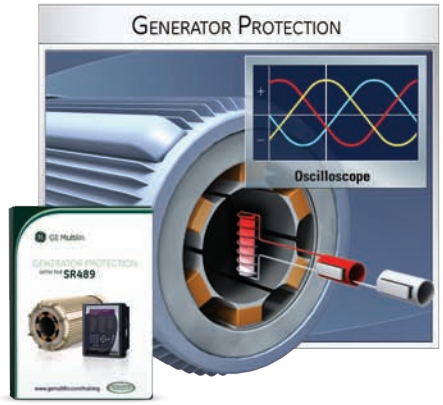

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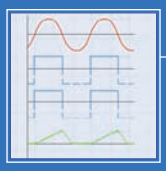

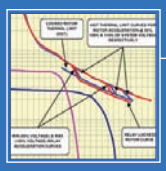

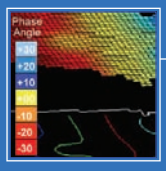

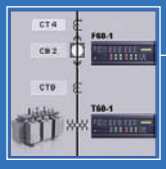

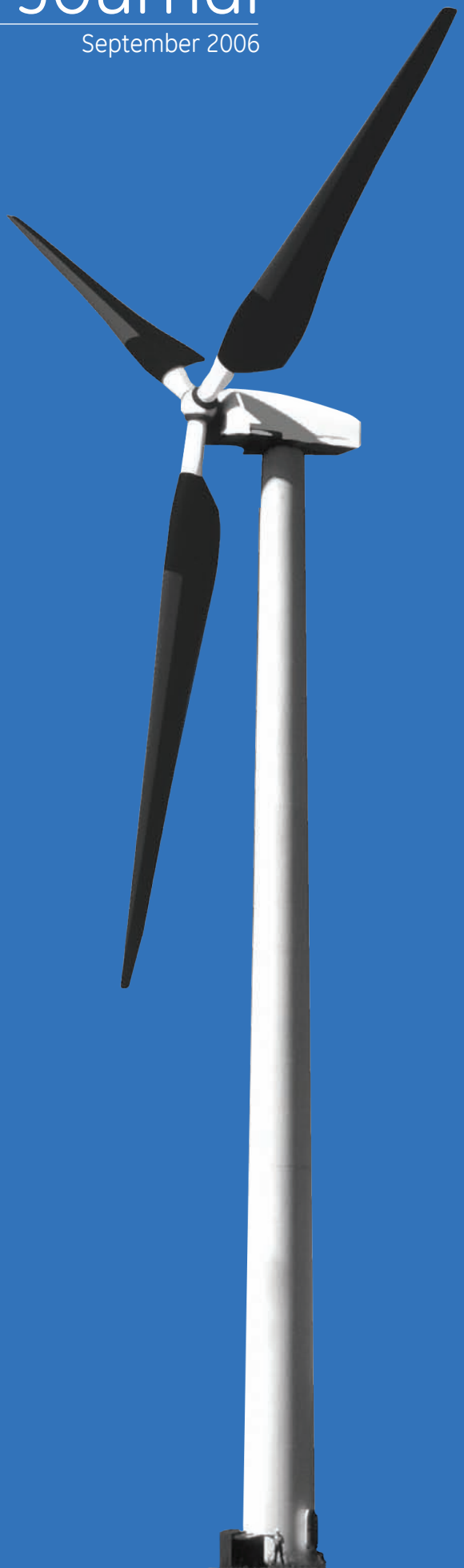

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Rebirth of the Phase Comparison Line Protection Principle

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1. Introduction

Relay engineers face growing application challenges for transmission line protection - heavy line loading, system operation near limits with high risk of stable or unstable swings, and fast clearing-time requirements. At the same time, overloaded engineering organizations find it difficult to keep line relay settings up-to-date as the system evolves. Current comparison pilot line protection overcomes these challenges, and can be a better choice for simplifying and improving line protection on modern stressed systems with less attention on applications. It works on long or short lines, has minimal or no settings that are impacted by power system topology or evolution, and resists tripping on swings (except where desired).

A widely-used form of current comparison is current differential relaying. However, not all potential users can afford the data communications infrastructure that current differential relays need in order to exchange current values. Another form of current comparison, used for decades in earlier design implementations, is Phase Comparison (PC) pilot line protection. The Phase Comparison protection principle gives users the important performance benefits of Current Comparison, with reduced pilot channel investment. Using simple on/off or frequency-shift communication equipment, such as power-line carriers, PC uses timing of binary channel signals to compare analog values at all line terminals. It offers excellent sensitivity, very fast tripping, immunity to power swings, effective protection for long or short lines and reduced need for setting calculations and settings maintenance. Performance is superior to that of pilot distance or directional comparison schemes. The Phase Comparison principle is an attractive choice for a company line protection standard, inexpensive and easy enough to use for retrofits on second tier transmission, yet well suited for secure, dependable protection of the most important transmission lines. We explain below how a modern implementation of Phase Comparison pilot protection meets the technical and management demands for protective relaying of today's systems.

In the era of analog solid-state relays, Phase Comparison was performed with relatively simple circuits that performed dependably in straightforward applications. A more sophisticated, expensive, and communications-intensive form of PC, segregated-Phase Comparison, worked well in difficult applications including series-compensated EHV lines whose distorted fault currents could fool the more basic PC relays of that generation. In North America PC had evolved into a niche methodology, used enthusiastically by a few major utilities and only in spot applications by many others. Until now, it has not enjoyed the development attention given to directional comparison and distance relaying products, or even to current differential relays. Internationally, the principle has been used more widely for decades. Early implementations of PC on microprocessor-based relay platforms poorly emulated the analog solid-state designs, and seemed to underuse the potential for advancement of Phase Comparison capabilities. Thus, PC has remained a niche application here. However, the mathematical and signal analysis capabilities of today's processors enable measurements and discrimination that were never possible before. This paper goes to the core of the operating principle to demonstrate new design approaches that handle the most difficult relaying situations, exceeding the capabilities of the earlier analog schemes.

Application of Phase Comparison relays calls for attention to communication channel performance. The measurement and computing capabilities of modern relay platforms provide tools for accurate interpretation of Phase Comparison channel signals, as we discuss further below. In critical ways, an updated PC relay can actually perform better than current differential, given the bandwidth limitations of digital communication channels practically available and used for protection (64 or 128kbps), and the length and cost limitations of dedicated fiber optic cables.

This paper presents Phase Comparison protection in the following sequence:

1. How popular Phase Comparison schemes work, in logic block diagrams.

2. Channel requirements and limitations, including the impact of typical channel misbehaviors on protection.

3. Application rules, benefits, and limitations including handing of multi-terminal and weak feed situations.

4. Relay designs in use to date – early and late analog solid-state relays, and microprocessor implementations. Drawbacks of schemes available until now.

5. Capabilities of latest-generation multi-microprocessor platforms, and the resulting solutions to drawbacks of existing schemes.

6. Why PC is the ideal standard scheme for many or most utilities (and when other choices make sense). Pros and Cons of PC versus Directional Comparison (DC) pilot relaying.

2. Phase Comparison Schemes

2.1. Basic principles

Protection engineers are familiar with current differential protection, in which all the currents entering and leaving the zone of protection for a phase are summed. Normally the sum equals zero according to Kirchoff's current law. A fault in the zone yields a nonzero sum equal to the fault current.
A percentage differential tripping characteristic is a common security measure used to distinguish between fault currents and measurement errors in current transformers or other components of the current measurement chain. The differential current Idiff is the phasor sum of the currents entering the zone. The restraint current $I_{restraint}$ is derived from the magnitude of the currents flowing into the zone – typically the largest current, or the summation of the individual current magnitudes (not their phasor summation). With this characteristic, the relay sensitivity is reduced (more differential current is needed to trip) when the fault current is large, lessening the risk of tripping due to CT saturation, CT ratio matching imperfection or other error sources. It is worth noticing that measurement errors can affect the magnitude and/or phase information with respect to the currents. The differential principle uses both magnitude and phase, and is therefore exposed to both sources of errors, calling for restrained characteristics or other means of enhancing security.

Line current differential protection is a specific variant of this core principle, in which currents from the two (or more) ends of a transmission line are summed in this way. Because of the distances between line terminals, the current values must be encoded for transmission over a communications channel. Compared to direct-wired comparison of CT signals for bus or transformer protection, long-distance modulated communications introduce a time-shift delay in the transmitted value. The receiving terminal must therefore delay its locally measured current by an amount equal to the channel delay so that the comparison signals are properly time-aligned, before summation and comparison of the characteristics for a tripping decision. In addition, being measured by separate relays at various geographical locations, digital line current differential protection needs to solve the synchronization issue by employing self-synchronization of individual relays as a group (the so-called "ping-pong" method), synchronization to a master, synchronization to an external source (typically GPS), etc. Typically these are proprietary complex technical solutions.

In basic Phase Comparison (PC) protection, the channel does not attempt to send the entire waveform between terminals. Instead, the channel conveys only the phase information with respect to the current, by sending only one of two states; either the sending-end waveform is above the zero axis, or it is below the axis. The same two-state logical determination is made for the local current signal at the receiving terminal. After delaying the local signal to align with the received signal, the states of the two signals are compared (see Figure 2-1). For normal load flow or for an external fault, the situation is as shown on the right. Current flows into one end, and out of the other. If the CT circuits are consistently polarized at the two ends, then the local and remote mark signals (positive phase position of respective current signals) have little or no coincidence – if we combine them with an AND gate, its output will be false, or will have at most two short true pulses per power cycle if the current waves are not exactly out-of-phase. For an internal fault, as shown on the left, current flows into the line from both ends. The local and remote mark signals are now aligned for all or most of the positive half-cycle. The output of the AND gate now comprises a positive or true pulse lasting about one-half cycle, alternating with a false or zero output of the same duration. If the AND gate output feeds a timer of about one quarter power cycle pickup delay, the output can be used to initiate tripping of the local breaker.

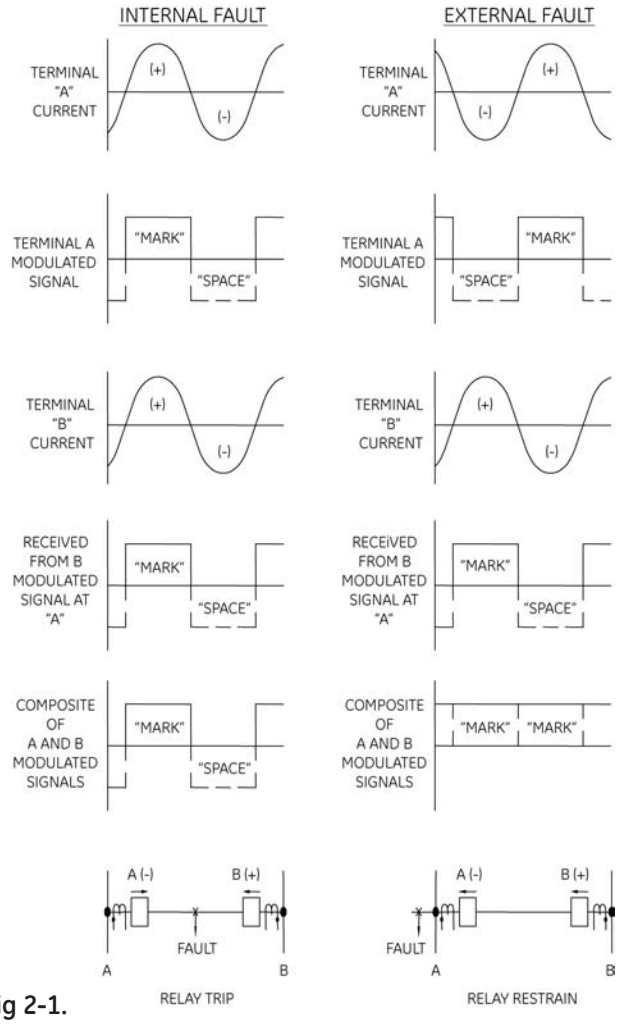


Fig 2-1.
Basic phase comparison operation.

To complete the basic concept, we note that at each end, we are independently performing both the sending-end and receiving-end functions. So the receiving logic at each end can make the trip decision and trip the local breaker. A bi-directional channel is used; in each direction the channel need convey only two states. Specifically, on-off or frequency-shift power line carrier channels, and other simple two-state channels, are well suited to the job. If the channel accurately conveys the logic signal, then both ends are looking at exactly the same comparison signals, and both ends will always make the same decision at the same time.

Note that the system, even if implemented digitally, does not call for synchronization of the individual relays. This is because the information exchanged is encoded via timing of the pulses related to the same "analog" or "continuous" time.

Note that the core trip decision may be as fast as 6 to 8 ms, and is generally under one cycle, plus channel delays and processing delays in the relays.

Let us go back to one of the key differentiators between the Current Differential and Phase Comparison principles. Current Differential uses both magnitude and phase information, and is therefore prone to errors in either of these two components. Phase Comparison, in turn, uses the phase information only in terms of timing a particular current polarity, and therefore is much less sensitive to magnitude errors. As a rule, Phase Comparison is a more secure principle except in cases where low signal magnitude makes the phase information less accurate (such as on series-compensated lines). Response to CT saturation of a segregated Phase Comparison is a good example of the philosophical difference between 87L and 87PC principles.

2.2. Practical three-phase implementations

So far, we have sidestepped a key point. The above description talked about comparing one current wave, but of course there are at least three currents at each end. If we want to compare the residual currents at the two ends for ground fault detection, we have four choices. The straightforward but expensive approach is to run three or four comparisons in parallel, with multiple channels. The comparison method is robust for each of the three phases and for the residual current. With these four comparisons, two or more will provide a fault indication for any particular fault type (phase to ground, phase to phase, two phase to ground, three-phase). This segregated Phase Comparison approach has been successfully used for decades on important transmission lines where the economics of the channel needs are not a drawback. More recently, the four comparisons have been encoded using a modem on a single data channel to reduce channel demand, although this approach is not compatible with power-line carrier channels.

For the broadest range of applications on lines with familiar types of power-line carrier, we need to develop a single current wave at each end, that can be compared in order to detect any type of fault. This is traditionally accomplished by deriving the sequence components of the currents at each end. The relay then recombines or mixes the sequence currents with predetermined weighting factors to yield a single composite comparison current wave whose phase position gives robust discrimination of all fault types.

The three phase currents are transformed to three sequence currents using the familiar symmetrical components definition (for the ABC phase rotation):

$$\begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} I_A \\ I_B \\ I_C \end{bmatrix} \quad (2\text{-}1)$$

where $a = 1\angle 120^0$

Analysis of how these currents behave during faults shows the following:

TYPE OF FAULT	SEQUENCE COMPONENTS		
	POSITIVE	NEGATIVE	ZERO
Single-phase-to-ground	YES	YES	YES
Phase-to-phase	YES	YES	NO
Double-phase-to-ground	YES	YES	YES
Three-phase	YES	NO	NO

Relay designers carry out detailed evaluation of the behavior of the sequence current phasors during the various fault types, while considering difficult boundary conditions such as high-resistance fault currents and heavy load flow before the fault.

For now, we point out that negative sequence current has the unique property of being a robust indicator of nine out of the ten fault types, as well as being clearly different for load versus fault current conditions. Comparing the negative sequence current waves at the two ends gives excellent fault protection, unless we experience a three-phase fault.

The only current with which to compare for a three-phase fault is the positive sequence current. To overlay this comparison with the negative-sequence comparison using the same channel, we mix a small quantity of positive sequence current with the negative sequence current according to:

$$I_C = I_2 - K \cdot I_1 \quad (2\text{-}2)$$

Where I_C is the comparison current wave developed at each line terminal and K is the design or settable positive-sequence weighting factor. A typical value for K is about 0.2. The comparison is thus dominated by negative sequence current, with only enough positive sequence mixing to ensure tripping for all three-phase faults that produce no I_2.

Note that expression (2-2) is a vectorial difference, which has an impact on the amount of current seen during various fault types. For example, the amount of current is lowered during single-line-to-ground faults in the phase used as a reference for calculating the symmetrical currents, but not in the two other phases.

Early analog solid-state PC relays developed sequence currents using electromagnetic filters based on iron-core reactors, capacitors, and resistors. These filters were acceptably accurate

in steady-state operation. However, transient conditions could drive the reactors into nonlinear operation, and there was no guarantee that the filters at the two ends of the line would behave correctly, or identically, for badly distorted waves. In particular, the highly distorted fault currents of series-compensated lines would cause these relays to malfunction, and utilities with these lines adopted other methods including the segregated Phase Comparison that had no sequence filters.

Modern microprocessor-based PC relays use mathematical filtering techniques that are not subject to the same misbehavior. The sequence-filtering calculations are linear and well behaved, whether the wave is sinusoidal or distorted. An important fact is that both ends can be made to have the same response. Thus, modern relays using mixed-sequence components can handle difficult applications, such as series capacitors in the line, that confused older design generations.

2.3. Control of comparison and tripping

Practical systems do not exchange square waves constantly. In some power-line carrier systems, monitoring requires that the channel not be actively relaying most of the time. When light-load currents are flowing or the line is floating, there may be a net current inflow to the zone from line charging, that is not a fault. To restrict comparison to potential fault situations, we add fault detector elements in both the transmitting and receiving logic.

A fault detector can be a disturbance detector (delta I), an overcurrent element or an overreaching distance element. The latter is typically provided at no or marginal cost in modern microprocessor relays, and if used, is set with enough reach that it never fails to pick up an internal fault. Severe overreach of such supervisory elements is not a problem.

A practical relay uses separate fault detectors for the transmitting and receiving logic. The low-set or long-reach fault detector that triggers transmission of "square waves" (FDL) is always set more sensitively than the high-set or shorter-reach trip-supervising fault detector at the receiving end (FDH). We must ensure that the tripping end can never make a decision to trip based on the absence of carrier if the sending-end fault detector fails to pick up. Note that, since there are actually two mirror-image logic systems making comparisons, we find an FDL setting and an FDH setting in the relay at each end.

Overcurrent elements can almost always be coordinated so that FDH at terminal A never picks up without FDL at Terminal B for an internal line zone fault. Using overcurrent is much better than using distance elements, because it completely eliminates the use of voltage in the PC protection scheme. This makes PC fast, as well as immune to CVT transients or to potential blown fuses or CVT failures.

2.4. Single-phase comparison blocking PC

The most commonly used PC logic is the single-Phase Comparison blocking type. The use of an on-off carrier channel or functional equivalent is similar in concept to the very familiar directional comparison blocking.

See the simplified single-Phase Comparison blocking logic in Figure 2-2. We have already explained the development of sequence currents from the phase currents, the mixing to obtain a single comparison current, the use of an on-off carrier channel, and the supervision of transmission and tripping by FDL and FDH fault detectors respectively. The squaring amplifier provides logic TRUE and FALSE signals based on the composite current wave phase position. Note that there is logic for transmitting PC signals (AND2, lower right) and for comparing the received wave

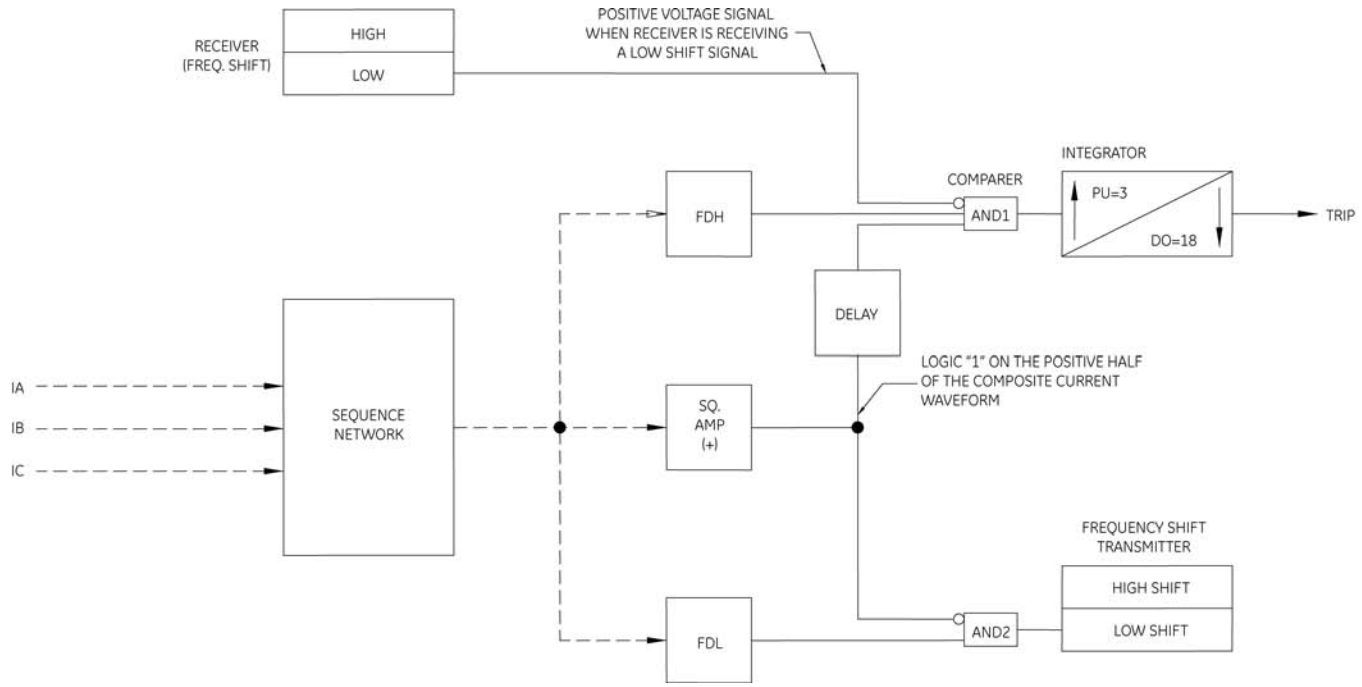


Fig 2-2.
Single-Phase Comparison Blocking PC Logic.

with the local wave (AND1, upper right). A delay line function delays the local square wave by the same amount of time that the carrier channel delays the received square wave, so we can treat the local and remote square waves as perfectly aligned for currents that are exactly in phase. The output of AND1 feeds a tripping timer, also called the coincidence timer. Note that the term "square wave" is used for simplicity and education. In general the wave is not symmetrical but should reflect the positive and negative polarities of the current. Relay design solutions based on the term "square" (i.e. assuming or forcing the transmission to be symmetrical within the cycle), used to cause problems (on series-compensated lines for example).

Consider the behavior of this logic with the internal and external fault situations shown in Figure 2-1. Assume that the faults cause both FDL and FDH to pick up. The FDH input to AND1 will allow tripping at this terminal only if FDH is TRUE. The FDL input to AND2 enables the squaring amplifier output to key the blocking transmitter ON and OFF according to the phase position of the composite wave. Note that, since the square wave input to AND2 is inverted, the transmitter is keyed ON (blocking state) when the composite current wave is negative and keyed OFF (blocking removed) when the current is positive.

Now consider what happens in the receiving logic at the other end. Figure 2-1 shows that, if the fault is external or if only load is flowing, the positive half-cycles occur in alternating (rather than coincident) half-cycle time frames. When the local current is positive, the squaring amp and delay line are feeding a true or mark input to the bottom of the comparer, AND1. But at the same instant, the remote wave is negative and the blocking carrier is received. The blocking signal is fed into the inverter input of AND1, where it prevents the output of AND1 from running the 3-millisecond timer that leads to a trip decision. Thus, the remote end blocks tripping using the carrier signal whenever the local delay line is feeding a TRUE signal to the comparer.

For internal faults, the phase position of the remote square wave is reversed by roughly 180 degrees. In this case, when the local wave is positive, the carrier from the remote terminal is OFF. For an ideal fault, the conditions for AND1 are met during the entire positive half-cycle of over 8 ms. After just 3 ms, the logic issues a trip output. This comparison result is mirrored at both terminals.

An important feature of the blocking PC scheme is that transmitters at both (or all three) line terminals can transmit on the same frequency, as is true for blocking DC. Using a single carrier frequency conserves valuable carrier spectrum, especially with a three-terminal line. When the local transmitter sends the blocking signal, both the local and remote receivers respond to it. The logic of Figure 2-2 shows that, when the transmitter is keyed ON (when the local square wave is negative), the local comparer is blocked by the pickup of the local receiver. For an internal fault, both (or all) transmitters must go silent for the 3 ms coincidence time, at which point all terminals are able to trip.

As with DC blocking – if the blocking carrier channel isn't able to send a blocking signal during a fault, the local pilot logic is not restrained from tripping. The important benefit of this logic is apparent for an internal fault, which shorts line conductors and may attenuate or completely short out the blocking carrier signal; tripping can still take place with no loss of time. If the channel equipment has actually failed, this can lead to a false trip for an external fault. Thus, ON-OFF carrier should be tested often, preferably by an automatic check-back test that runs several times per day.

2.5. Trip time

The time to reach this decision depends on the phase position of the measurement currents at fault inception. For the logic shown and an ideal fault, the decision time ranges from 3 to about 12 ms. Add to these the channel delay time (also set as the local delay time), which can range from 4 ms to 12 ms depending on the carrier channel bandwidth. Also, add the current signal filtering and processing time, and the time for the trip output device to pick up. A relay contact output adds 2-4 ms unless a fast solid-state output is used. For a fast carrier channel, total trip times range from 1/2 cycle to 1 cycle depending on the fault inception angle. The upper end of this trip time range can be drastically reduced with dual-comparison logic described below.

Sections 4.3 and 6.8 below explain how the setting of the coincidence timer (typically about 3 ms) is determined, and how the timer is implemented in the most effective design.

Narrowband carrier sets that conserve spectrum and handle longer lines with greater attenuation, also unavoidably use selective filters that reject adjacent channel signals and the out-of-band corona noise. These receiver filters respond slowly to changes in the transmitted signal, and the output appears after a relatively long delay. This necessarily requires coordinating delays in the PC (or DC) logic, which slows down the pilot protection. For fast tripping, use wideband carrier sets or configurations. Ensure that the transmitted power can overcome coupling and channel losses with adequate margin at the receiver. Section 3 gives more guidance on this point.

2.6. Dual-phase comparison blocking PC logic

As we explained above, the actual trip time for single-Phase Comparison PC can vary, depending on the polarity and phase of the ac wave at fault inception. It is clear that the longer trip times could be reduced if the relay were able to compare phase relationships on both half-cycles instead of just one. It is also clear from the logic explanation, that this can't be done with security using a single ON-OFF channel.

If the user is willing to upgrade the carrier channel to a frequency shift keying (FSK) system of a two-frequency or three-frequency type, the relay can implement more complex logic that compares both polarities in alternation. While the fastest trip times will be at best the same as with single-Phase Comparison PC, this enhancement cuts over 8 ms from the

longest trip times, narrowing the variation of trip times to the 3-5 ms range. In making this comparison of trip times, we assume, of course, that the channel delay did not change when the ON-OFF carrier was exchanged for FSK. The potential user must check this point carefully when selecting the FSK carrier; looking at the class averages, FSK transmitters and receivers operate in narrower bands than blocking ON-OFF carriers, and have longer channel delays. Fast wideband FSK carriers are available with large frequency shifts at a cost of increased spectrum consumption and reduced tolerance of carrier-path attenuation (due to increased noise in the wide-open passband of the receiver).

An FSK carrier transmitter is constantly sending a signal – a guard or monitoring frequency – which shifts to another frequency (or choice of two other frequencies in a 3-frequency system) on command from the relay. Because of this, the transmitter at each end of the line must have its own assigned frequency slot, to which the remote receiver is set. If the line has 3 terminals, then 3 frequency slots are consumed, and each terminal has two receivers to hear each of the two other transmitters independently. In analyzing how the logic works, keep in mind that an internal fault can still short out the carrier signal, causing a loss of guard at the moment of fault inception. Also remember that in this case, the local receiver(s) will not change state in response to the local transmitter, as it hears only the companion remote transmitter.

Figure 2-3 shows simplified dual-Phase Comparison blocking PC scheme logic, used with a two-frequency FSK channel. Comparing this to Figure 2-2, note the use of both positive and negative squaring calculations, feeding the two independent comparers AND1 and AND2. For simplicity, the channel delay compensation is not shown, but is applied where the local squared wave enters each comparer gate (the squared signal that shifts the local transmitter to high during the negative half cycle is not delayed). The local receiver has two outputs that alternate according to the remote current. In this logic, since the transmitter is sending at all times in any case, the FDL element is deleted and the channel is keyed constantly with phase information. The FDH overcurrent or overreaching distance element at the receiving end enables tripping.

For external faults, the channel signal alternations block one comparer and then the other in turn when the local input would enable tripping. For an internal fault, the received square wave aligns out of phase with the local squared wave, so that it does not block the comparer, and the coincidence time delay expires. If the internal fault kills the received carrier, blocking is removed from both gates and either local wave polarity can pick up its comparer gate and trip the terminal. For security and channel monitoring, tripping can only occur if the channel loss coincides with pickup of FDH, and is only allowed for 150 ms after pickup of FDH. For complete loss of carrier at other times, PC tripping is blocked. Sustained channel failure should be alarmed.

A popular variation of this logic is dual-Phase Comparison unblocking. It is a cross between blocking and tripping (next section) in that it operates in the blocking mode but the blocking signal is sent continuously as a guard signal during non-fault times. Unblocking logic uses a two-state FSK carrier. The squaring amp output is used to shift the carrier to the trip frequency, removing the block at the remote terminal if the waves are aligned. Unblocking logic can also trip if an internal fault shorts the carrier signal; tripping can occur if the carrier loss coincides with FDH pickup, and is limited to a 150 ms window after fault inception, as for the blocking logic. The scheme must include some means to stop the blocking signal from being transmitted from an open terminal in the event of a fault. For example, a breaker 52b auxiliary contact.

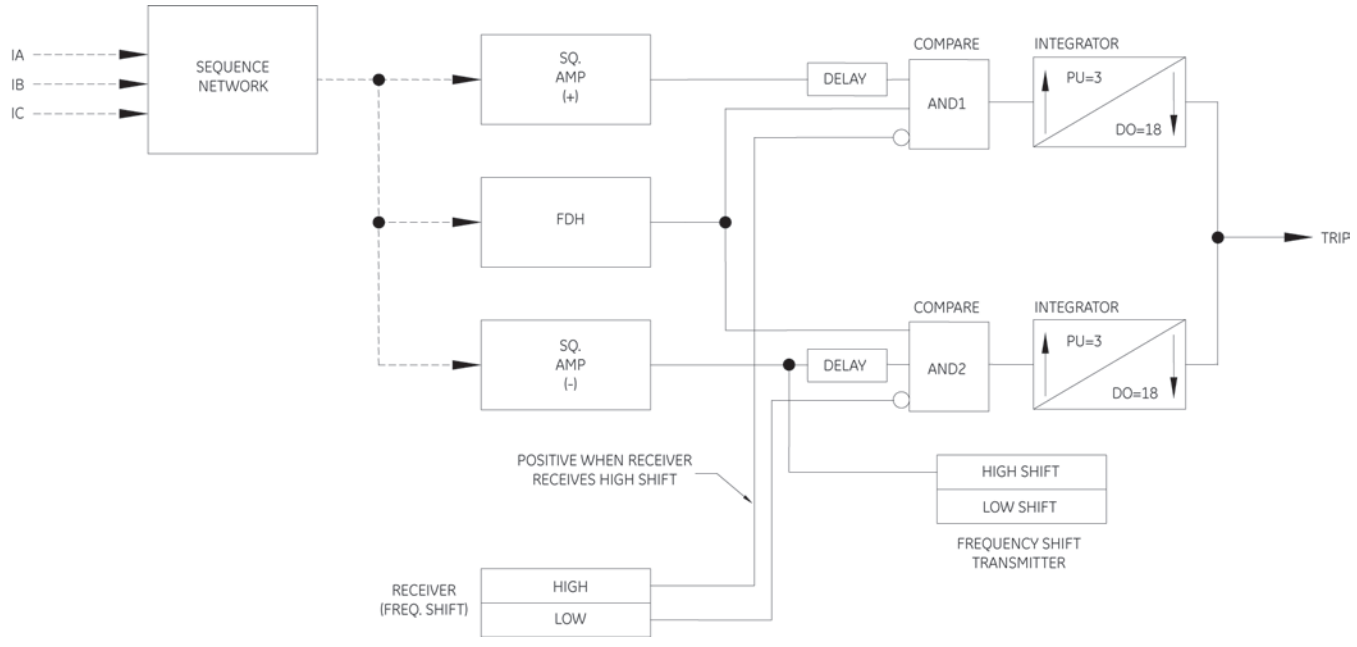


Fig 2-3.
Dual-Phase Comparison Blocking PC Logic.

2.7. Dual-phase comparison tripping PC logic

Figure 2-4 shows the more elaborate logic of the dual-Phase Comparison tripping scheme. Compared with the dual-Phase Comparison blocking logic of the last section, this logic offers the better security, but requires a three-frequency channel. The center frequency of the three-frequency channel is not used for protection logic, but provides continuous monitoring of the channel integrity, important for security during non-fault times.

The fault detector FDH supervises tripping by either positive or negative comparisons. For the positive half-cycle, AND1 compares the alignment of the delayed local positive square wave (the delay buffer for the SQ. AMP (+) output as it feeds into AND1 is not shown) and the remote positive square wave as conveyed by the high-state detector output of the receiver. If the local and remote waves are aligned for over 3 ms, the integrator or comparer output picks up and tripping is initiated. Similarly, AND2 compares the alignment of the delayed local negative half-cycle square wave and the remote negative half-cycle wave as conveyed by the low-state detector output of the receiver.

The local transmitter sends a continuous guard signal on the center frequency for channel monitoring during non-fault times, and is keyed to high or low frequencies by the squaring amplifier outputs only if the low-set fault detector FDL picks up. As with the other logic schemes, the local FDL should be set to always pick up for any internal or external fault that picks up the remote FDH. However, note the security bias of this tripping logic: the remote terminal cannot trip if the local FDL fails to pick up and the channel is not keyed. Gate AND3 ensures that the transmitter is never asked to send high and low frequencies at the same time; it cannot do this. The negative square wave takes priority and causes a low shift in the event, such that both are momentarily present.

3. Channel Requirements & Limitations

Depending on speed requirements and logic selection, 87PC is most often used with ON-OFF or frequency shift (FSK) carrier channels. Phase Comparison is desirable because it yields all its benefits, explained throughout this paper, using such ubiquitous, utility-owned, economical channels. 87PC also performs well on other channels, ones suited to binary state transmission: audio tone sets on leased analog telephone circuits or analog microwave, and digital data transfer sets operating on the same audio circuits or on dedicated fibers.

87PC can work with contact transfer cards in T1/E1, SONET, digital microwave, or other multiplexed data communications WAN facilities in use at a growing number of utilities, as long as the channel can be configured such that the propagation delay is constant or within tight constraints (under 1 ms variation) in the face of switching or rerouting events. This communications flexibility, along with outstanding protection abilities, makes Phase Comparison a natural choice for a standard pilot scheme, useable across the entire power system. The ability of Phase Comparison to work on a carrier channel is its major trump card over current differential protection, although it has other protection performance advantages that are explained throughout this paper.

Accordingly, the logic and processing algorithms are carefully arranged to handle the idiosyncrasies of carrier channels, along with those of other channel types. These logic and algorithm adaptations are explained in previous and following sections.

To begin, the Phase Comparison user (or any carrier-based pilot relay user) should begin with proper application analysis of the carrier channel itself. See references [1], [2], and [3] for important details. The application process comprises:

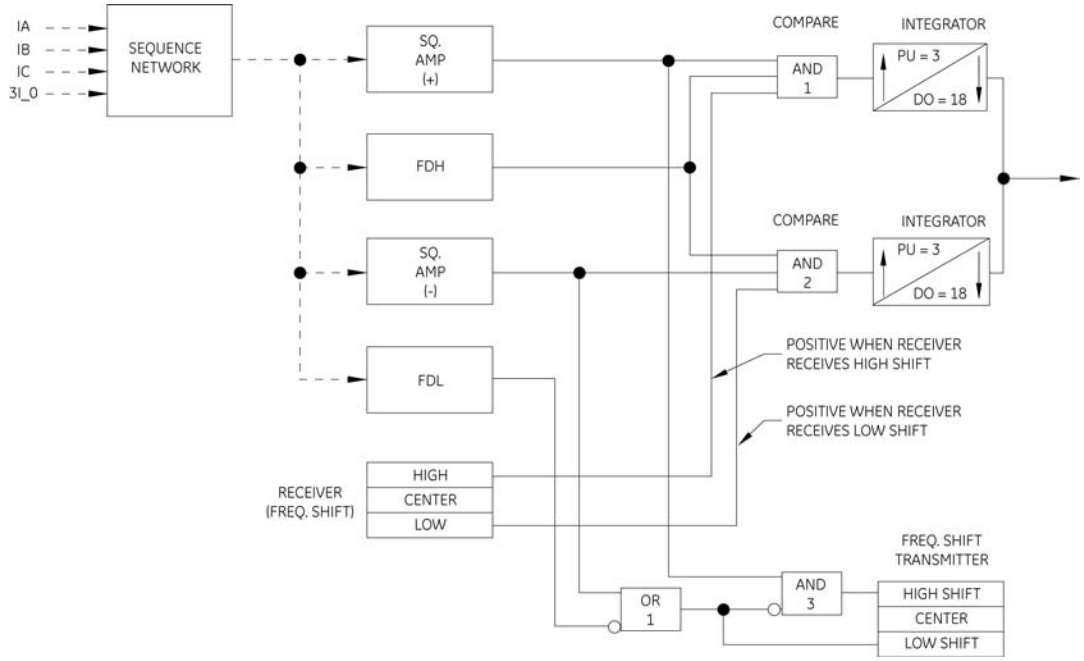


Fig 2-4.
Dual-Phase Comparison Tripping PC Logic.

1. Channel loss calculations from transmitter power level (typical +30 dbm or 10 watts) to received signal level.

    a. Hybrid losses, as the transmitter is combined with other transmitters and receivers sharing the same tuning interface to the line. Add to this hybrid losses in db, at the remote (receiving) end.
    b. Outbound local coupling losses based on tuner, CVT, and modal analysis of the coupling to the line (often on the center phase or an outer phase). Add to this the inbound coupling losses in db at the other end of the line.
    c. Loss in db per unit length of line, based on line voltage and construction, and on the chosen frequency of operation.
    d. Losses due to mode conversion at each transposition point.
    e. Losses due to imperfect blocking of modes by line traps.

2. Channel noise calculations at the receiver.

    a. Corona noise data in dbm based on line voltage and construction, as well as the chosen frequency of operation.
    b. Corona noise during foul weather and icing conditions, as opposed to fair weather levels.
    c. Noise power correction for the bandwidth of the receiver, as compared to the bandwidth of the instruments used to collect either the reference data, or actual measurements from a line in operation before applying the carrier.
    d. Corona noise power is often in milliwatts and swamps any electronic circuit or thermal noise, which are ignored.

3. Calculation of signal to noise ratio (SNR) at the receiver detector

    a. Ensure SNR of at least 10 db to 20 db for the worst noise conditions.
    b. Ensure that transmitter power is adequate to yield this SNR. Increase power (use an amplifier), improve hybrid connection architecture, or upgrade line-coupling equipment to raise signal level. If signal is very high, receiver must have gain attenuation control and signal level metering.

4. Other application considerations

    a. Select modern transmitter-receiver sets with frequency synthesis, selectable bandwidths, 3-frequency or 4-frequency operation to combine transfer trip with pilot protection, and serial or Ethernet data communications ports for integration of the carrier set with substation control systems and remote monitoring.

    b. Check the bandwidth of the carrier channel for its effect on channel delay and its impact on tripping speed. It is also important to have an initial delay estimate within ½ cycle of the exact value to avoid aliasing errors when adjusting the relay logic channel delay using the load testing methods explained in the following section.
    c. Check that the channel logic bundled in the receiver by the manufacturer, does not conflict with duplicate or alternate logic in the relay. Turn it off, or order equipment without unneeded logic.
    d. Use channel monitoring including guard loss (FSK), automatic checkback testing (ON-OFF or ASK), reduced-power margin testing, and out-of-band noise detection (correction of noise alarm setting for noise monitor bandwidth, versus bandwidth of reference or field data).
    e. Ensure that there is a maintenance program for line coupling equipment, especially outdoor equipment such as coax cable, line tuners, drain coils at the base of the CVT, and protective gaps on CVT and line tuners, that often collect spiders' webs (the contaminated gap flashes for mild voltage transients and shorts the carrier signal, producing carrier holes).
    f. Avoid the frequencies of licensed radio services operating near the line, that use a carrier band of 30 kHz to 535 kHz.
    g. Integrate with spectrum management with respect to the interconnected network; frequency use typically not repeated for at least two line sections away, or mitigate with better line trap configuration.
    h. Check for compatibility of telemetry or voice facilities operating on carrier channels during quiescent times.
    i. Ensure there is a program for reviewing analog carrier channel input oscillograms (remotely retrievable COMTRADE files) provided by the latest microprocessor relays (explained in the next section), to check for holes in, or deterioration of, received carrier signals, and for dispatching maintenance before experiencing relaying problems.
    j. When employing ON-OFF carriers at three-line terminals all sharing the same frequency for 3-terminal single comparison blocking, ensure that the transmit frequencies are offset slightly (about ± 100 Hz) to avoid the risk of zero-beat cancellation during any external fault seen by two or three terminals.

Note that in Section 4.4 below, the text explains to the user how the logic and timing of the Phase Comparison can be adjusted to minimize exposure to tripping problems due to intense positive corona discharges.

While applying these methods can only help add to the security margin for any installation, the authors emphasize that it is critical to design the carrier system with an adequate signal-to-noise ratio under the worst conditions, as explained both above and in the referenced carrier application guides.

If this is done right, the corona noise concerns of Section 4.3 won't matter. The advice in 4.4 below has been helpful for ensuring tripping dependability in overseas applications where carrier channel performance was marginal.

4. Application of Phase Comparison

4.1. General principles

Setting a phase comparison relay is simple. In general, only a handful of settings is required:

Scheme type
(blocking/tripping, single/dual comparison).

This selection is typically driven by system conditions such as weak infeed, channel availability and characteristics, and historical experience within a given utility. Typically the design group makes this selection "once and for all" for a given utility, voltage level, etc.

Operating current
(phase segregated, zero- or negative-sequence, K-value, coincidence timer/angle) and fault detectors (FDL, FDH)

This requires simple short-circuit calculations, and following simple setting rules, lessening the work requirements for the project group. These settings have plenty of margin and are robust in the face of system evolution, so fewer coordination studies are needed over time. Some of these can be standardized for the entire range of system applications at a utility.

Channel settings
(delay, pulse asymmetry).

This is done on a per installation basis using channel measurements and experimentation, and is thus part of commissioning. Modern digital relays simplify this task greatly by providing excellent channel monitoring tools.

Application of Phase Comparison not be concerned with many obstacles applicable to distance or digital current differential relays, but needs to focus on the following basics, and advanced protection concepts, as applicable:

- Settings fault detectors (Section 4.2).
- Setting of the coincidence timer (Section 4.3)
- Selecting phase reference (Section 4.4)
- Channel delay setting (Section 4.5)
- Weak-infeed conditions (Section 4.6)
- Three-terminal lines (Section 4.7)
- Two-breaker terminals (Section 4.8)
- Long lines and cables (Section 4.9)
- Single-pole tripping (Section 4.10)
- Series-compensated lines (Section 4.11)

4.2. Coordinating fault detector settings

The fault detectors must satisfy the following setting rules:

a. FDH must pick up at all line terminals for all types of faults and locations and target fault resistance for SLG faults.
b. The phase difference in the operating current between any two terminals during all internal fault situations must be less than the tripping threshold of 90 degrees theoretically, and about 115 degrees in practice.
c. For blocking schemes, the FDL at the local relay must be set low enough to pick up on all reverse faults that activate the FDH level at the remote terminal.
d. Neither FDL nor FDH should be picked up under load conditions.

The above rules are straightforward for phase-segregated applications.

Consider next the negative-sequence operating mode. Here typical setting rules are:

$$FDL_{PKP} = 1.1 \cdot K \cdot I_{LOAD} \quad \text{(4-1a)}$$

$$FDH_{PKP} = \frac{3}{8} \cdot I_{CHARGE} + \frac{4}{3} \cdot FDL_{PKP} \quad \text{(4-1b)}$$

The 10% margin in equation (4-1a) with respect to load requirement (D) is acceptable, as sporadic pickup of the scheme is allowed on load, swing or switching events. The charging current requirement in equation (4-1b) can be eliminated if a given relay compensates for it (see Section 4.6).

On long heavily loaded lines, the FDH value of equation (4-1) may have difficulty meeting the dependability condition (A). If this is the case, advanced starting such as impedance or disturbance detection (delta I) can be used in parallel with regular overcurrent starting. This inconvenience can be easily overcome compared with coordination problems encountered for distance functions on long, three-terminal or heavily loaded lines.

4.3. Coincidence timer setting

For the ideal fault cases of Figure 2-1, the "square waves" are either in perfect alignment or in perfect opposition, suggesting a coincidence timer setting of 8.33 ms for a 60 Hz power system. However, real faults are never so perfect , and the "square waves" do not have ideal zero degree or 180 degree relationships. Among the factors that change the phase relationship are:

1. Through-load currents flowing during the fault.

2. Load combined with nonzero fault resistance.

3. CT saturation, which narrows the positive and/or negative current wave pulses and shifts the phase position of zero crossings.

4. Line capacitance charging current, which produces a net inflow from the two or more terminals.

5. Faulty adjustment of the local delay timer, or unnoticed changes in channel delay.

6. For a solid internal fault at a time of load flow, the source angle differences between the buses will lead to phase angle difference between the currents each end contributes to the fault (this will not happen during external faults, and does not impact security).

7. Asymmetrical pickup and dropout times for the carrier receiver (pulse asymmetry).

Exhaustive analysis of real-world fault cases has shown that a coincidence timer setting of 3 to 4 ms for a 60 Hz system provides good security against false tripping in the face of all the influences we just listed, while tripping reliably for all internal faults. 3 ms corresponds to a minimum blocking angle zone of about 65 degrees. See Section 6.8 below for an explanation of how to implement the coincidence timer function.

4.4 *Corona Effect* – Selecting reference and shifting the operating current

Power lines generate high-frequency noise due to the corona effect. If the carrier installation has been properly designed and maintained as explained in Section 3, the receiver signal-to-noise ratio will be adequate for reliable tripping in the face of the worst corona noise. If the carrier channel is quite marginal, there is a danger that the corona noise may be received by the carrier equipment as a valid signal. This in turn may result in worsened dependability when using blocking schemes. For users who cannot correct the basic carrier system shortfall, it is beneficial to shift the "space" periods away from the corona-induced noise. This can be done when using single-comparison schemes because of the asymmetry of the corona effect. The following setting methods can only help improve the margin in any installation, but can be ignored without risk if the channel SNR is as robust as it should be.

The power conductor (round) and ground (flat plane) creates an asymmetrical capacitor, making the positive corona (potential of the conductor is positive with respect to ground) much worse than the negative corona. As a result the "space" periods should be shifted away from the positive peaks of the voltage towards the negative peaks and small voltage values, at least for faults that do not involve the conductor on which the carrier is installed. In the latter case, we trust that the fault will depress the voltage, alleviate the corona effect, and reduce the danger of creating a ghost mark period within the actual space interval.

Figure 4-1 presents a case BC and BG faults for the case of phase-A being used as a reference for calculating symmetrical components. Note that the transmission will have to be shifted in the leading direction by approximately the line characteristic angle, in order to move the space periods away from the positive corona, and toward voltage zero crossings or the negative corona.

Optimization of transmission with respect to the positive corona requires the following:

a. Calculating symmetrical components with respect to the phase used by the carrier (setting on the relay or external connections).
b. Advancing the phase angle of the composite current by approximately 90 degrees to effectively postpone the periods of coincidence for all faults involving the carrier conductor (setting).
c. Compensating for the relay/carrier delay between the negative polarities of the operating current and the moment the actual space period is put on the high voltage conductor by fine tuning the ideal value of 90 degrees (item b above). The goal is to place the coincidence periods in optimum slots given the delay between changes in polarity of the current and the frequency shifts (setting).

Modern relays provide for all these requirements by allowing shifting of the angle of the operating current freely with respect to the reference phase (see Section 6 for details).

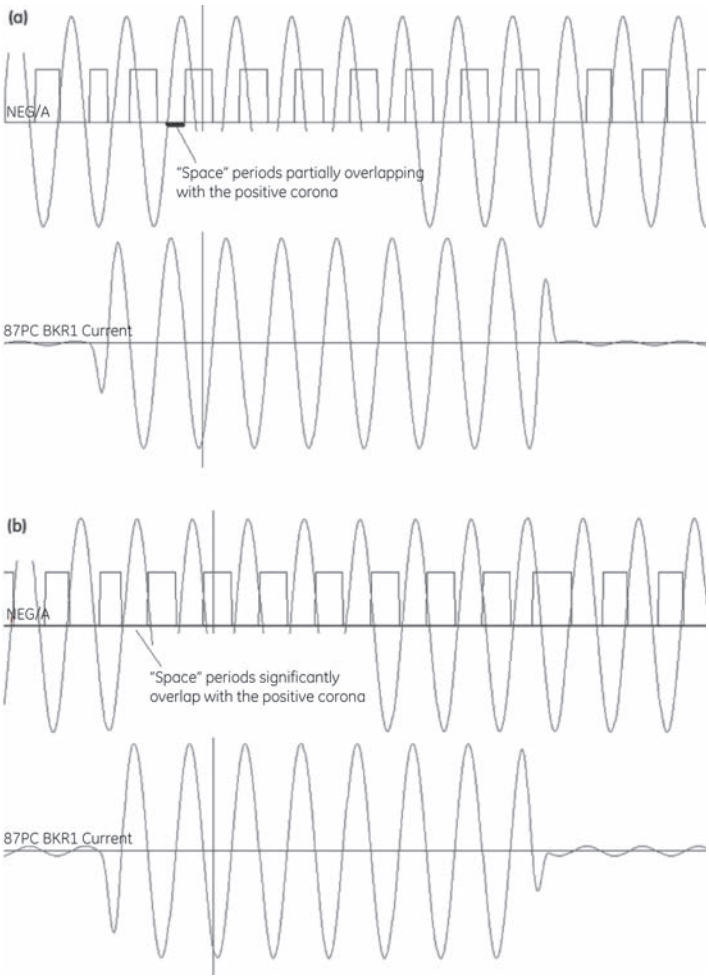


Fig 4-1.
Internal BC (a) and BG (b) faults. The A-phase is used by the carrier, and as a reference for calculating symmetrical components. The transmit signal (blue) needs to be advanced by approximately 0.25 of a cycle to reduce the impact of the positive corona (carrier voltage in red).

4.5. Channel settings

It takes a finite time to transport the phase pulses between terminals on the line. Each receiving relay must delay its local pulses, and potentially remote pulses from a faster channel, in order to align the information before measuring the coincidence time for the trip/no-trip decision. Channel delay is therefore one of the crucial relay settings. Practical values of channel delay could reach or exceed an equivalent of 90 degrees making it necessary to measure and compensate for it.

Modern relays allow explicit measurement of the channel delay during controlled conditions such as commissioning. The most accurate way is to measure the delay using either GPS-synchronized current injection, or by observing relaying square wave coincidence alignment for a through load condition for natural synchronization. The latter requires forcing the relays into keying by temporarily lowering the FDL settings, or by overriding the actual key condition from other more convenient flags. Care must be taken when tuning the delay setting based on the natural load on long lines; charging current will play a role there. A choice can be made, however, to align the two terminals taking into account the typical load and the actual line-charging current.

Figure 4-2 presents an example based on a relay oscillograph triggered during commissioning. Assuming the two currents were perfectly out-of-phase (GPS-synchronized test, or load current), one can measure the total relay-carrier-relay delay and adjust for it when setting the relay. To cross-check, or for extra accuracy, the delay should be measured in both directions. In general the A-to-B and B-to-A delays may differ slightly. The process of measuring and entering new values of delay setting may be iterated until a perfect alignment is achieved, resulting in no signal passed to the integrators under through-current conditions.

When using load or reference currents for alignment, some a priori knowledge of the approximate channel delay is required because of the risk of aliasing pulses – mistakenly choosing a pulse that is one cycle earlier or later than the correct target alignment pulse. When keying permanently one can measure the delay with an accuracy of multiples of half a cycle.

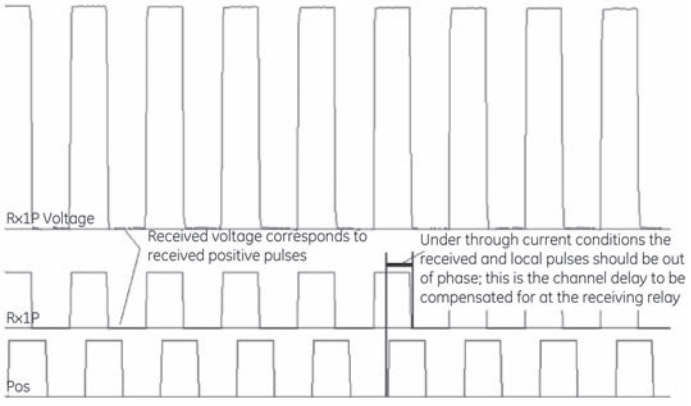


Fig 4-2.
Using advanced relay monitoring means to measure channel delay settings.

Pulse asymmetry is another setting that may be needed. This measurement is even easier and does not require synchronization. Upon forcing transmission one triggers oscillography at both ends of the line and measures the duration of "marks" and "spaces" directly from the Comtrade files. The amount a "mark" is extended constitutes a positive pulse asymmetry setting; a shortened "mark" calls for a negative setting.

4.6. Weak-infeed conditions

Blocking schemes work naturally under weak infeed conditions. The weak terminal would not establish blocking action for a forward fault, thus allowing the strong terminal to operate. This assumes that the charging current out-feed does not lead to a spurious reverse-direction indication. Setting the FDL threshold accordingly prevents this undesired response.

Permissive schemes do not handle weak-infeed conditions naturally, and they therefore need an explicit condition that would substitute the permissive pulses sent in normal situations. This is handled by weak-infeed logic combining well-known elements such as voltage unbalance with no reverse fault indication, undervoltage with no reverse fault indication, echo supervised with no reverse fault indication, echo controlled from the breaker position, etc. Those conditions could be established using known practices while using the voltage, current and impedance functions of the relay.

One of the simplest solutions is to use an overcurrent condition of the FDL. If set properly, the FDL detector would pick up on all reverse faults. Therefore, if dropped out, the FDL could be used to trigger permissive echo to the strong terminal. If FDL is operated, it means that the terminal produces enough current to key permission on its own, and the echo function should be inhibited.

Tripping the weak terminal after the strong terminal clears the fault, is a universal problem for both PC and DC schemes. This could be accomplished via DTT or from a loss-of-load / undervoltage logic.

4.7. Three-terminal lines

Phase Comparison schemes are typically easier to set than Directional Comparison on three-terminal lines . The FDL and FDH conditions can almost always be set to satisfy the security / dependability criteria, unlike impedance reach settings that often create coordination problems.

Permissive schemes call for individual frequencies for each of the remote terminals.

Blocking schemes work with a single frequency. The terminal, which sees a reverse fault condition, sends the block that is received by all relays, including the blocking relay. Note that two of the three carrier transmitters should be detuned from the nominal carrier frequency by about 100 Hz (one up, one down). This avoids the possibility of an external fault causing

two or more transmitters to zero-beat out-of-phase and cancel the blocking signal at some receivers.

4.8. Two-breaker terminals – through currents and CT saturation

Past practice with respect to protecting two-breaker line terminals (breaker-and-a-half or ring-bus) is to sum up the two currents externally, and feed a single-breaker line relay with the total current flowing into the protected line.

Security under reverse fault conditions at the two-breaker terminal is a concern in such applications. With reference to Figure 4-3 the fault current flowing through the two breakers is limited by the short circuit capacity of the local bus, and could reach significant levels. On the other hand, the actual line current supplied through the line toward the fault is limited by the short circuit capacity of the remote equivalent and the line itself. This current can be much lower compared with the through fault current. The ratio could reach 40:1 [4].

The sum of the two currents at the two-breaker terminal correctly reflects the actual line current if both the CTs perform with no, or minimum, errors (Figure 4-3a). When one of the CTs saturates, the "missing" current will appear as a spurious component in the relay input current. In particular, when the CT carrying the reverse current saturates, a spurious forward component is added to the relay input currents. With enough missing current due to CT saturation, the spurious forward current would override the actual reverse line current, and the relay input currents would appear in the forward direction (Figure 4-3b). This leads to misoperation of the single-input line relay.

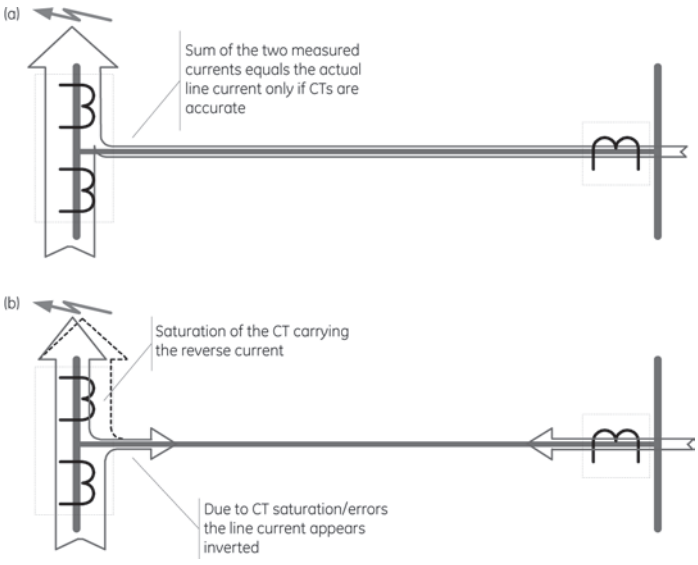


Fig 4-3.
Impact of CT saturation on two-breaker line applications. Accurate CTs preserve the reverse line current direction under weak remote feed (a). Saturation of the CT that carries the reverse current may invert the line current as measured from the externally summated CTs (b).

The scenario shown in Figure 4-3 applies to individual phase currents, and would take place where CT errors are large enough to override the actual line currents. When considering symmetrical components of the currents (zero- and negative-sequence), there will be cases when the real line current is zero, yielding no margin for any CT error. Under such conditions any CT errors could yield spurious operating signals resulting in misoperation, if the relay is set too sensitively.

Consider a line-to-line external fault in the system shown in Figure 4-4. The neutral (zero-sequence) current through the line is zero regardless of the short circuit capacity of the remote equivalent. If any of the 4 CTs carrying the current through the two breakers saturates, a spurious zero-sequence current is created, potentially in the tripping direction.

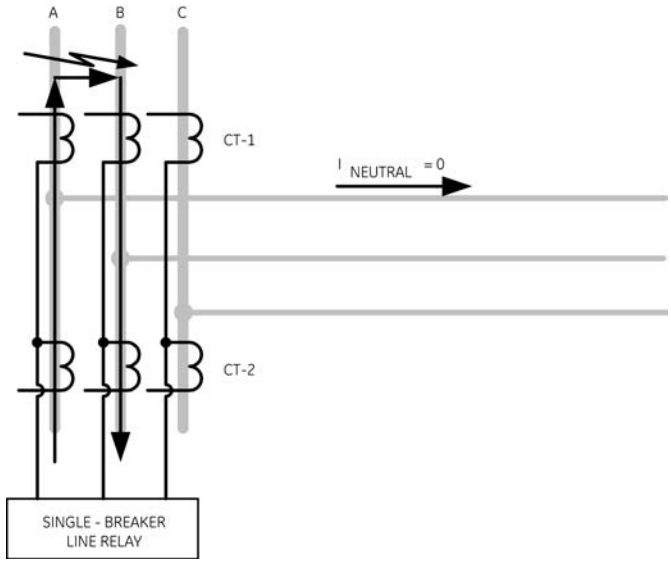


Fig 4-4.
Symmetrical currents are particularly exposed to through-fault conditions.

Similarly, consider a three-phase symmetrical fault in the system shown in Figure 4-4. Saturation of any of the 6 CTs carrying the currents may create spurious negative- and/or zero-sequence currents. These are practical scenarios for the application of Phase Comparison relays responding to the composite (mixed-mode) signals.

All line protection principles, if set to be highly sensitive, are prone to this problem (current differential, distance, ground directional overcurrent, Phase Comparison). This results from feeding a single-breaker relay with grossly inaccurate current signals.

In recent years dual-breaker distance and line-current differential microprocessor-based relays have emerged.

Although primarily driven by the ability to achieve integrated P&C designs by providing breaker fail, synchrocheck and auto-reclose functions, these multi-function IEDs also address this security problem, because they are capable of individually measuring the two currents, responding to their magnitudes and directions before creating the summed signal for the main line protection function [5].

One of the chief advantages of the Phase Comparison principle is its natural immunity to CT saturation. Current waveforms distorted by heavy CT saturation preserve their correct "phase" information in the time domain. However, when fed with externally summed currents, a single-breaker Phase Comparison relay loses this ability and is exposed to misoperation with respect to reverse faults. This is particularly true for Phase Comparison relays working with composite currents (mixed-mode): zero- or negative-sequence, as explained above.

In order to address this issue, modern Phase Comparison relays are developed as two-breaker IEDs and apply appropriate measures to cope with through-fault conditions.

These schemes do not communicate the phase information separately for each of the individual currents; this would impose impractical requirements on the communication channel. Instead, the local currents are "consolidated" locally ensuring both security and dependability, and the remote terminals are presented with the "phase" information as in single-breaker applications. Section 6 provides more details.

4.9. Cables and long lines – capacitive charging currents

Capacitive currents "leak" from the unit protection zone causing an unbalance for the line current differential principle, and a phase-shift for the Phase Comparison principle. Charging currents are present both in the balanced pre-fault state (positive-sequence charging current) and during internal and external faults (unbalanced charging currents).

Most conservative protection philosophies exclude applications of Phase Comparison relays, or call for a Charging Current Compensation option on lines longer than about 150 km. In practice the problem becomes significant for lines in excess of 300-400 km. Assuming about 1A of charging current primary per km of line length, a 300 km line would generate about 300A of charging current – a value potentially comparable with through fault / load currents.

Consider a negative-sequence equivalent network for an external fault as shown in Figure 4-5a. The phase shift caused by the capacitive current depends on the X/R ratio of the line and system equivalents.

For large X/R values the capacitive current affects mostly magnitudes of the terminal currents. This is a concern for the line current differential, but less of a problem for the Phase Comparison relays (Figure 4-5b).

For smaller X/R values (highly resistive impedances), the capacitive current affects the phase relationship more, creating larger problems for Phase Comparison relays (Figure 4-5c).

Where highly resistive currents are concerned, such as when applying phase-segregated relays under heavy load / remote external fault conditions, the effect on phase is dramatic (Figure 4-5d).

A different problem occurs when a very weak system feeds an external fault through the protected line. The actual inductive current generated by the weak source may be smaller compared to the charging current, and the latter could invert the current measured at the weak terminal (Figure 4-5e). Effectively, the capacitance of the line would change the equivalent impedance at the strong terminal, from inductive to capacitive. This problem affects most sensitive directional functions that are designed / set with the assumption of inductive fault loop characteristics, including distance protection elements. Applying blocking vs. tripping (permissive) schemes solves this problem.

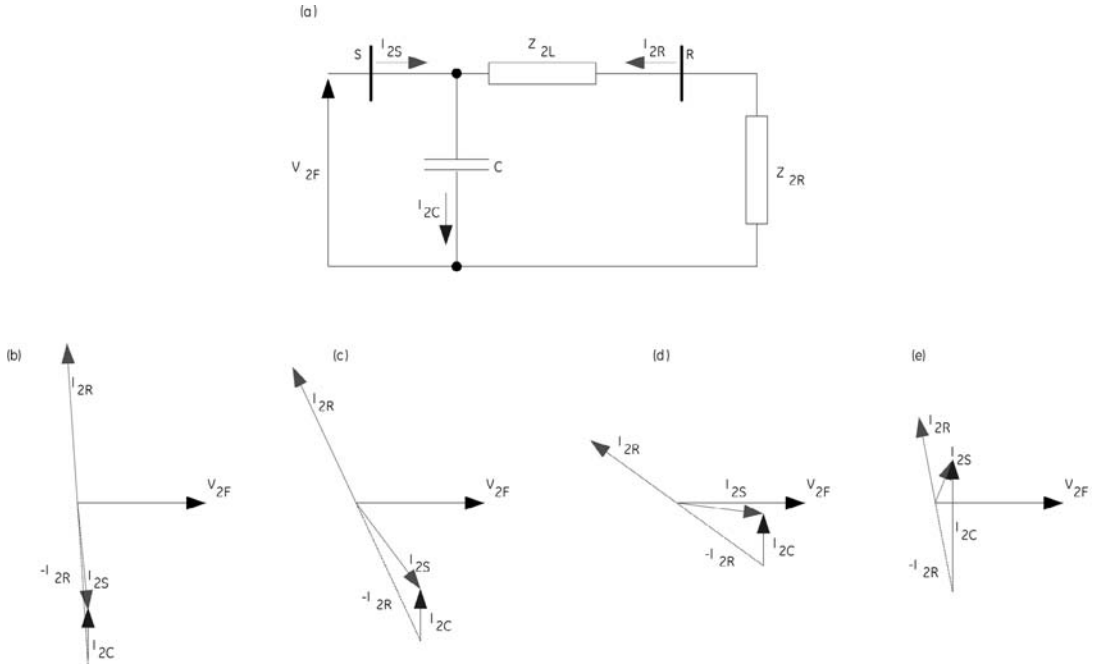


Fig 4-5.
Negative-sequence equivalent network for an external fault (a). Impact of the charging current under large (b) and small (c) X/R ratios; in highly resistive networks (d); and under weak infeed (e).

Large amounts of capacitive current call for increasing the coincidence timer/angle setting of the Phase Comparison element in order to maintain security (de-sensitizing the relay).

Impact of charging current on dependability when applying Phase Comparison relays, is difficult to quantify, and could vary. With reference to Figure 4-6a with respect to negative-sequence networks the line capacitances reduce the inductive character of both of the equivalent impedances into the S and R systems. With identical X/R ratios of such equivalent impedances, the two negative-sequence currents would be perfectly in phase. When the ratios differ, a phase-shift will occur. The capacitance can reduce or increase the difference in the X/R ratios, resulting in either a positive or negative effect on sensitivity (Figure 4-6bc).

Modern Phase Comparison relays compensate for the line charging current (see Section 6 for details). When applying such compensation it is important to consider shunt reactors, if installed. In this respect, it must be kept in mind that the inductance (of the reactor) and capacitance (of the line) cancel each other for the fundamental frequency only. When considering transients, an inductor is not a "negative capacitor". It is therefore prudent to exclude the reactors from the measuring zone, as shown in Figure 4-7, and configure the charging current compensation for the entire amount of the line capacitive current (not for the net between the line and installed reactors). This approach is not only technically correct, but also simplifies the application eliminating the need for monitoring the status (ON/OFF) of the reactors.

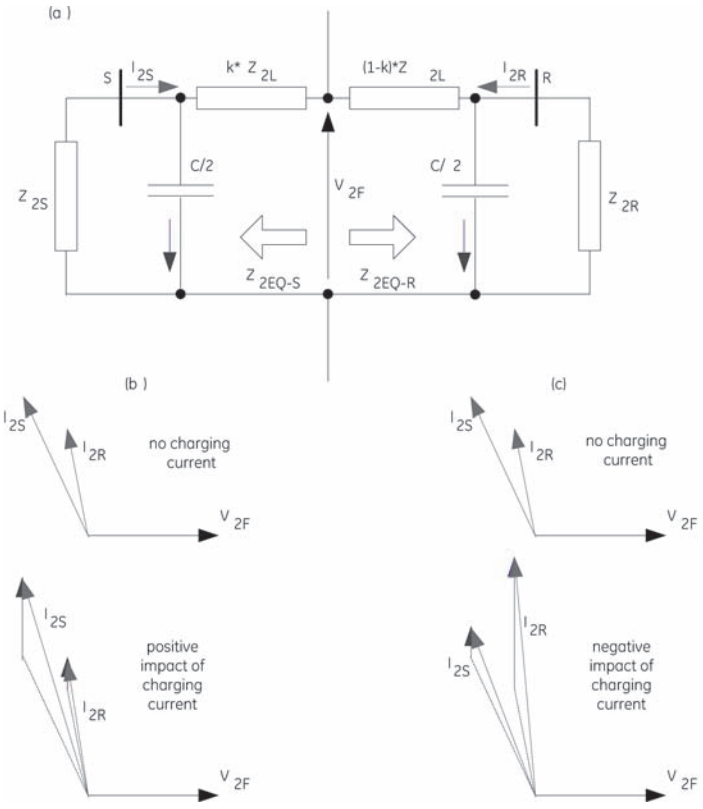


Fig 4-6.
Negative-sequence equivalent network for an internal fault (a). Positive (b) and negative (c) impact of the charging current on dependability.

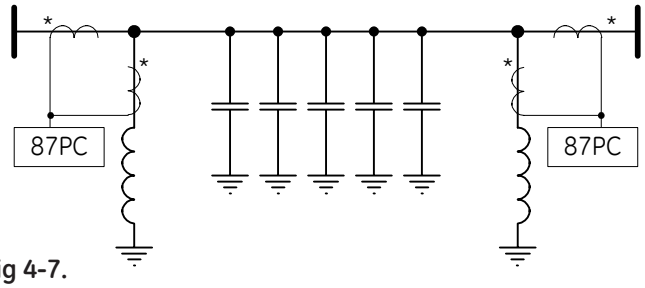


Fig 4-7.
Shunt reactors should be excluded from the measurement when applying charging current compensation in phase comparison relays.

4.10. Single-pole tripping

Single-pole tripping (SPT) applications:

- require fast phase selection logic in order to decide which phase to trip depending on the fault type
- call for the main protection function to remain dependable and selective for faults during the single-pole auto-reclose interval with one phase opened.

Unit protection schemes such as Line Current Differential and phase comparison – if phase segregated – could act as their own phase selectors. Modern line current differential relays often follow this principle. These relays employ digital channels for communication and could use SPT with either individual phase currents or composite (mixed-mode) currents.

In case of phase comparison relays, however, each operating signal calls for a dedicated analog channel, and, typical applications are therefore based on a single composite signal (typically negative-sequence augmented with a selectable amount of positive-sequence). Even if more communication channels are available, it is better to use them for dual comparison (faster operation) than to facilitate the explicit phase selection based on the main tripping function (perhaps with the exception of series-compensated lines).

Enhanced sensitivity of mixed-mode phase comparison, compared with phase-segregated phase comparison, is yet another reason to follow the mixed signal approach. This "phase-blind" principle, however, calls for dedicated phase-selection logic. This is similar to initiating single-pole tripping from "phase-blind" ground directional overcurrent elements in currently-used directional comparison schemes.

Being voltage-independent is one of important advantages of Phase Comparison. This benefit should be retained, if possible, when facilitating phase selection for single-pole tripping. Current-only phase selection methods are known and used in many practical implementations [6,7]. These methods use angular relationships between fault components of symmetrical currents: negative-, zero-, and positive-sequence (Figure 4-8). Being unaffected by load currents, these signals allow high sensitivity and fast operation, particularly when angle information is used exclusively, neglecting the magnitudes (more prone to transients and slower). One particular method uses voltages – optionally if available – to enhance performance under weak infeed conditions [7].

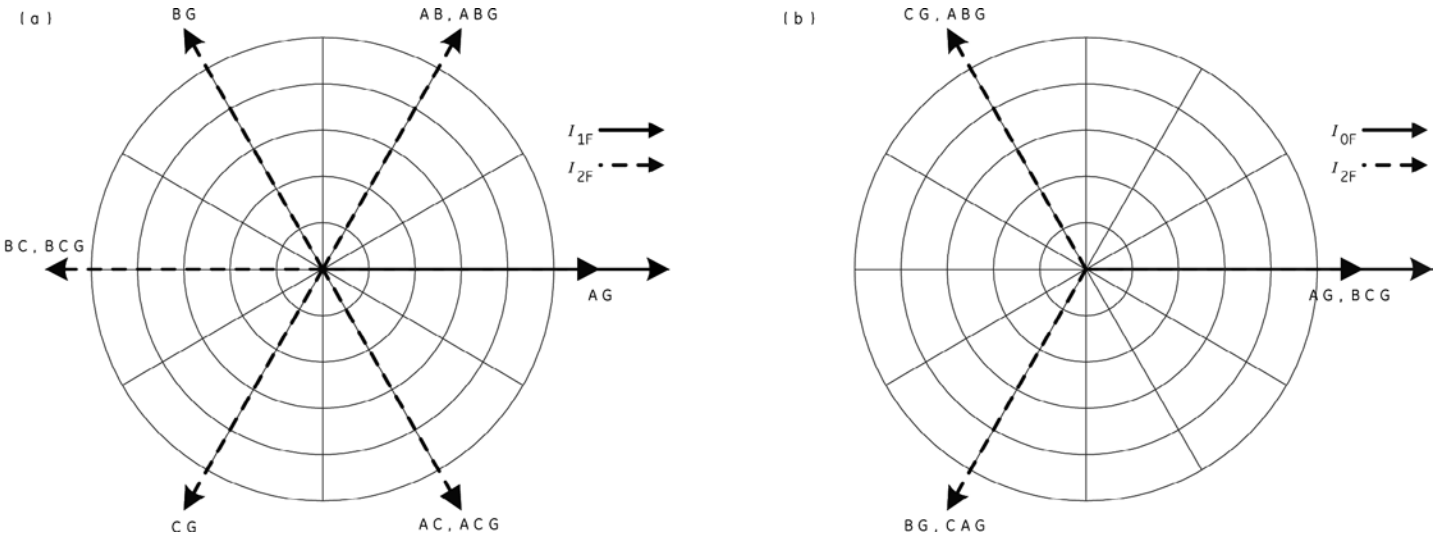


Fig 4-8.
Operating principle for the current-only phase selector based on angular relationships between symmetrical currents. Negative- and positive-sequence check (a). Auxiliary negative- and zero-sequence check for ground faults (b).

We discourage the use of overreaching distance elements for phase selection, even though they may be available on Phase Comparison relays for back-up protection. These elements have limited sensitivity to resistive ground faults, and might misidentify close-in ground faults [7].

Retaining the high sensitivity of mixed-mode Phase Comparison schemes is equally important. The phase selection logic must therefore be not only as fast (or faster) but as sensitive (or more sensitive) as the trip initiating Phase Comparison function. Current-based phase selection logic is proven to work satisfactorily in EHV networks, for ground faults with 300-ohm fault resistance [7]. Quite often such faults are cleared sequentially requiring only the strong terminal to detect, identify and clear the fault. Once the infeed effect is removed by clearing the strong terminal, the weak terminal operates.

The ability to detect evolving internal-to-internal faults during 2-phase operation in the dead time between a single-pole trip and reclose is another important requirement of single-pole tripping. Typically, sensitivity expectations for the second fault are lowered, while the selectivity requirements are sustained.

The Phase Comparison principle remains stable during two-phase operation. Typical schemes key continuously but remain balanced during load and external fault conditions (Figure 4-9). Quite often current reversal logic may activate to secure the scheme against external faults in the opposite direction compared with the unbalance current during the single-pole open condition.

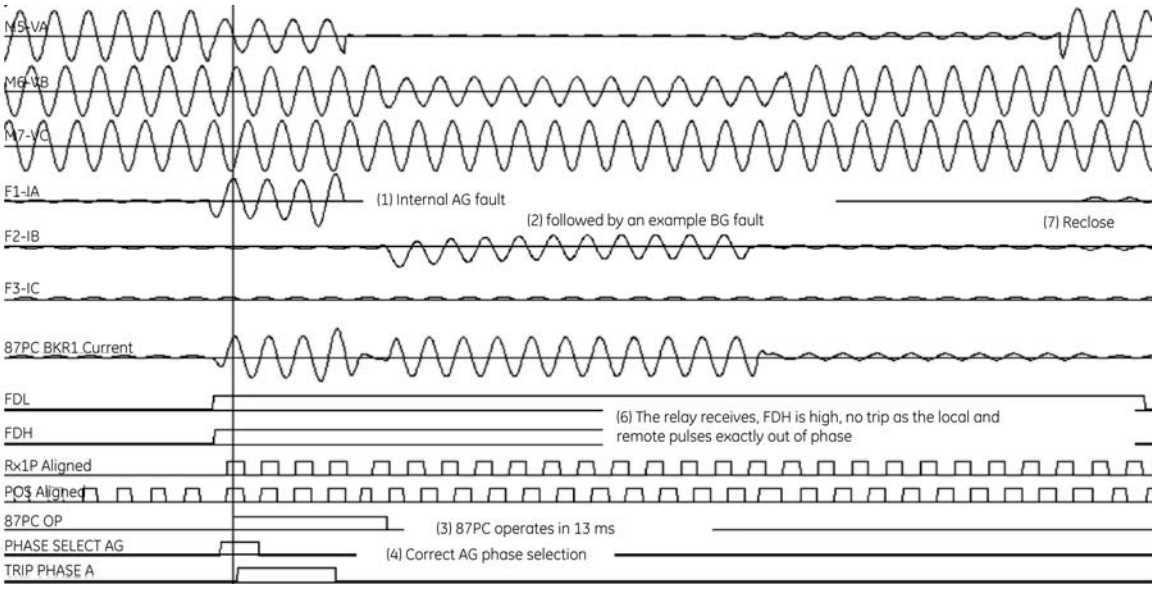


Fig 4-9.
Operation of a single-comparison tripping scheme during open-pole condition (evolving internal-to-external fault).

The scheme retains the ability to detect the second internal fault, but existence of the zero- and negative-sequence through current caused by the open single-pole, results in less sensitive, and possibly slightly delayed (due to current reversal logic), operation. See Figure 4-10 for an illustration.

Application of the Phase Comparison principle to single-pole tripping is relatively straightforward. Distance backup, and ground directional overcurrent functions require more attention when applying an integrated Phase Comparison relay for single-pole tripping.

4.11. Series-compensated lines

The Phase Comparison principle, as with the current differential principle, faces dependability issues when applied to series-compensated lines. Currents supplied to an internal fault from different terminals of a series-compensated line can be significantly shifted in phase, to the extent of jeopardizing reliable tripping.

This phenomenon, often labeled as "current-inversion", is much less dramatic than a literal inversion of 180 degrees, but is significant enough to cause dependability problems, particularly on high resistance ground faults. The problem is caused by different arguments of equivalent impedances from the fault location into equivalent systems. Some of these impedances will remain inductive, while some may see enough capacitive reactance added by series capacitors to depart from inductive toward resistive or even capacitive characteristics. If the difference in argument of these impedances is greater than the stability angle setting of the Phase Comparison element, one may run into tripping dependability problems.

High-resistance faults magnify the problem; low fault currents do not cause the overvoltage protection of the capacitors to conduct and partially by-pass the capacitors (typically Metal Oxide Varistors, MOVs). As a result, full physical capacitance is present in an equivalent circuit making it more likely to alter the character of the fault loop from highly inductive to resistive or even capacitive.

The amount of current inversion during internal faults depends on fault type and location, fault resistance, and system equivalents. The relationship is highly non-linear and its quantitative analysis is beyond everyday engineering [8].

In addition the phase currents, zero- and negative-sequence currents, may get affected to different degrees. With the MOVs in the faulted phases conducting significant currents, the effective capacitance in these phases is significantly reduced making operating conditions much more favorable. With one or two MOVs not conducting in the healthy phase(s) some capacitance exists in these phases, affecting symmetrical components of the currents. The effect is not significant, however, as the large currents in the faulted phases are inductive and would bias the zero- or negative-sequence currents toward an inducting character despite capacitances in the healthy phases.

Historically, it has been claimed that the mixed-mode approach faces security problems when applied to series compensated lines, while the phase-segregated relays would perform adequately. This statement should be revisited in the light of the newest digital implementations. During through fault conditions the phase currents at all terminals on the line match. i.e. assuming two terminals, the two currents are perfectly out-of-phase (neglecting line charging currents).

This remains true for any external fault causing asymmetry at the series capacitor (some MOVs conducting or bypassed). The two currents will remain out-of-phase as instantaneous values, even if they are rich in subsynchronous oscillation components. The positive and negative pulses of the Phase Comparison algorithm at both ends would miss each other perfectly. Duration and alignment of these pulses would appear chaotic due to the subsynchronous oscillations, but the phase relation will be perfectly retained.

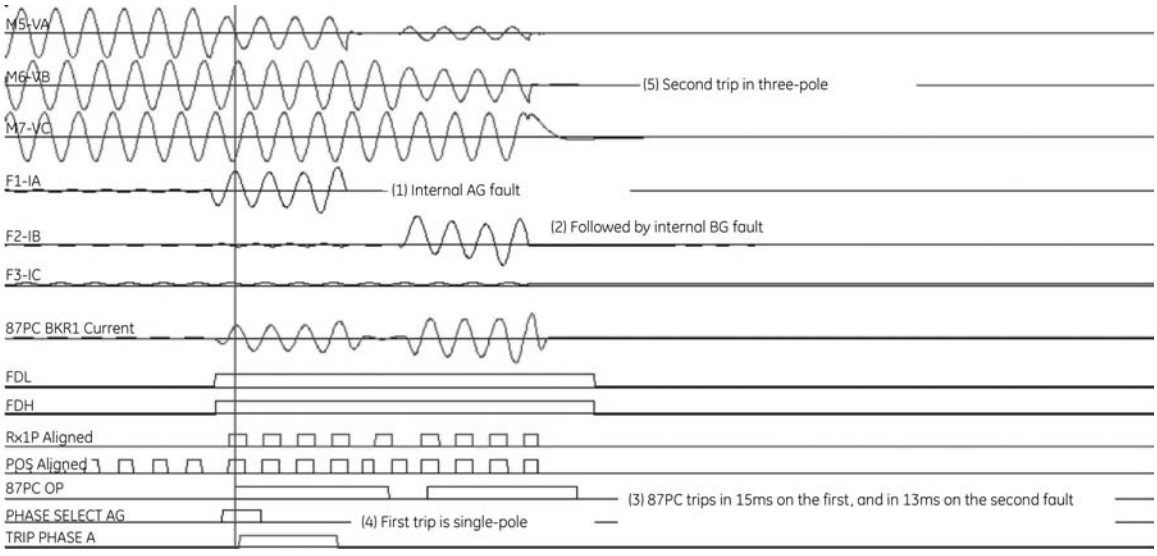


Fig 4-10.
Operation of a single-comparison tripping scheme during open-pole condition (evolving internal-to-internal fault).

Mathematically this could be written as:

$$i_{SA} + i_{RA} = 0 \quad (4\text{-}2a)$$

$$i_{SB} + i_{RB} = 0 \quad (4\text{-}2b)$$

$$i_{SC} + i_{RC} = 0 \quad (4\text{-}2c)$$

Let us add the three equations:

$$i_{SA} + i_{RA} + i_{SB} + i_{RB} + i_{SC} + i_{RC} = 0 \quad (4\text{-}3a)$$

The above can be re-grouped as:

$$(i_{SA} + i_{SB} + i_{SC}) + (i_{RA} + i_{RB} + i_{RC}) = 0 \quad (4\text{-}3b)$$

meaning:

$$3 \cdot i_{S0} + 3 \cdot i_{R0} = 0 \quad (4\text{-}4)$$

If the phase currents are balanced at both terminals, the zero-sequence currents are balanced as well - i.e. perfectly out of phase during external faults regardless of the series capacitors, MOVs, and positions of bypass breakers. A zero-sequence mixed-mode relay (differential or Phase Comparison) will therefore perform adequately during external faults on series-compensated lines. The zero-sequence calculation as a concept is valid in both time and frequency domains. The above analysis was done in the time domain and automatically applies to the frequency domain.

Analysis of the negative-sequence balance must be done in the frequency (phasor) domain, but it yields the same result: the negative-sequence currents are balanced on series compensated lines, assuming identical relays at both ends, neglecting the charging currents. The above analysis proves the key point that series-compensated lines can be properly protected by relays using the mixed-mode Phase Comparison principle, as long as the mixing logic uses linear operations allowing both terminals to exhibit the same, mutually-compensating, errors. To illustrate, Figure 4-11 shows an external AG fault causing large subsynchronous oscillations. The figure shows an "instantaneous negative sequence current" (operating signal I_2 - KI_1) at both terminals. The composite currents oscillate; but nevertheless, remain out-of-phase for this external fault.

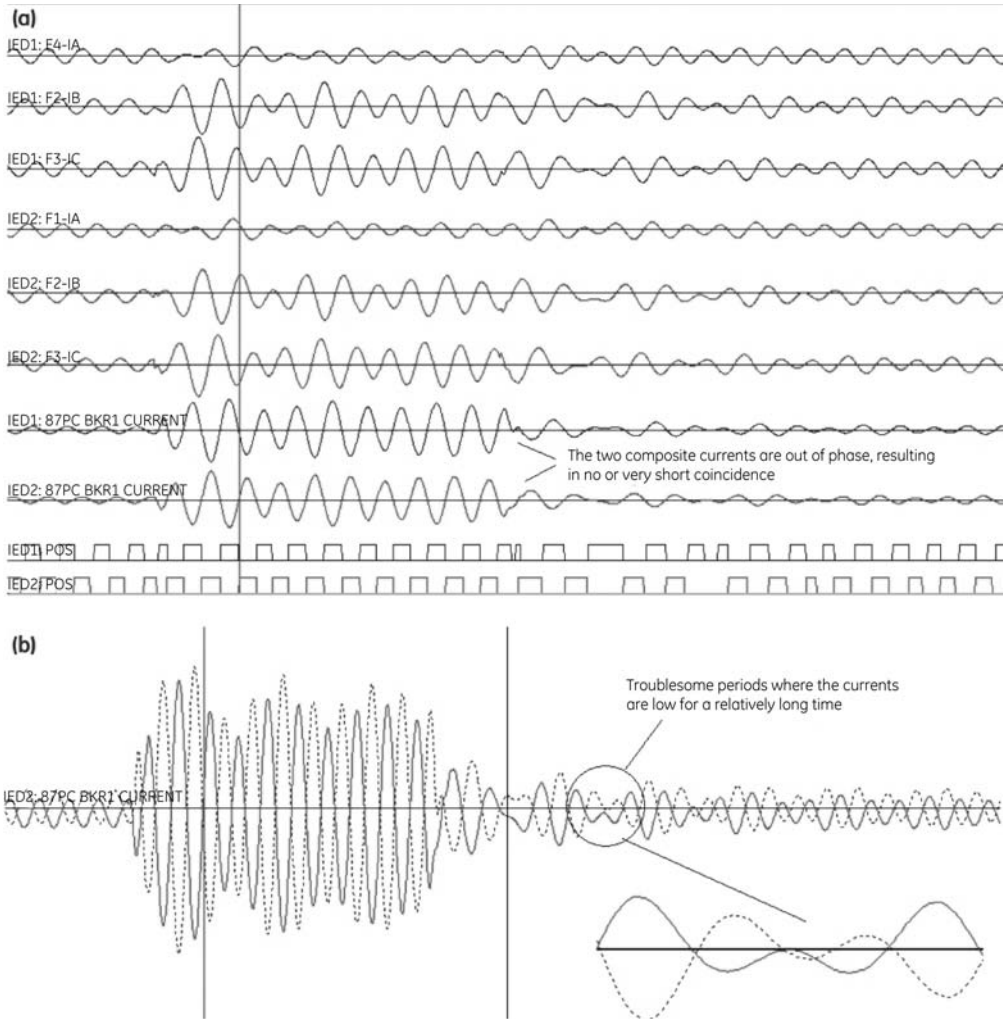


Fig 4-11.
Operating current of a mixed-mode phase comparison relay during an external BC fault on a series compensated line.

The phase pulses at both ends do not overlap, yielding no coincidence and making the scheme secure. Note, however, that the pulses are irregular in duration reflecting the subsynchronous oscillations. This may be a problem for older generation relays, but not for modern digital solutions as explained in Section 6.

As illustrated in Figure 4-11b there are periods of time, particularly when the current is low, such as after clearing the external fault, where the waveforms linger at relatively small values for a relatively long period of time (quarter of a cycle or so). During these periods the phase information can easily be altered by relatively minor factors such as charging current, CT errors, or finite relay accuracy. However, looking at Figure 4-11 one observes that the phase currents are subject to the same phenomenon. This casts doubt on the superiority of phase-segregated approaches in this situation. Older generations of analog Phase Comparison relays, limited by the available analog signal processing technology, performed filtering of the symmetrical currents imperfectly.

Inaccuracies of the symmetrical filters under subsynchronous oscillations were sometimes pointed out as the reason to move from the mixed-mode to the phase-segregated approach [4,6]. This is, however, a limitation of a certain relay technology, and not a constraint coming from the behavior of series compensated lines for internal or external faults. Extensive simulations on transient simulators prove that modern solutions such as [9] can be safely applied on series-compensated lines in a mixed-sequence component operating mode on a single channel. Considering single-pole tripping on series-compensated lines, single-ended current-only phase selection methods may be affected by the subsynchronous oscillations and/or current inversion (some symmetrical currents may be shifted while others will be less affected [8]). In this situation, the phase-segregated approach for both tripping and phase-selection functions is beneficial.

5. Drawbacks of Analog Implementations

The phase comparison principle, although analog in nature, requires several advanced operations on the input and intermediate signals.

1. Decaying-exponential dc-offset components need to be removed from input currents. Under ideal CT operation dc removal is not necessary, but in order to cope with saturated CTs the dc offsets should be removed as explained in section 6. "Transactors" – RL circuits mimicking the X/R ratio of the line - were once used for this purpose. Under elevated fault current situations, reactors in the mimic circuit would respond with slight differences at both ends of the line, yielding potentially significant differences in the current zero-crossing times, thus jeopardizing performance. Paradoxically, when fed with distorted waveforms of saturated CTs, these filters would magnify the high frequency components due to the large di/dt ratios encountered in saturated waveforms. Transactors were used in distance relays as well, but the distance principle is based on both phase and magnitude information, and is therefore less sensitive to these problems compared with Phase Comparison, where all information is compressed into the relative phase associated with current zero-crossings

2. The mixed-mode Phase Comparison uses filters to develop symmetrical component signals. These filters used to be realized by combining phase currents with their derivatives shifted by 90 degrees. This could be implemented by employing magnetic, electric, or electronic circuits. In any case, the operation has limited accuracy. Small differences in transient or steady-state response could yield significant differences in the zero-crossing times. The sequence filters showed a particular weakness on series-compensated lines; relay designers became convinced it was better to eliminate the problem by removing the sequence filters rather than improving them. This resulted in the widely-accepted, but theoretically unfounded biased solution of using segregated 87PC relays on series-compensated lines (see Section 4 above).

3. Each Phase Comparison relay needs to delay its local signals in order to align them with the naturally delayed remote signals. This operation seems relatively straightforward because the signals to be delayed are binary (on/off). In general, however, the pattern to be delayed is not regular, i.e. is not a textbook "square wave", and delaying is not therefore a trivial operation. It requires the equivalent of a delay line / buffer. Older relays used timers for delays. Timers would work correctly for well-behaved square waves, but could lead to very significant errors when the pulses did not follow the expected textbook pattern such as during current reversals on series-compensated lines, or under CT saturation while working with composite signals.

4. Older line carriers used to receive pulses with limited accuracy, typically extending the "marks" or "spaces". Accurate correction of this impairment requires receiving the original pulse, explicit detection of the impaired edge, and moving this edge back or forth appropriately. This is well beyond the capability of analog circuits. The pulse asymmetry correction was done using timers by forcing the received pulses to a "correct" length. This was nothing but arbitrary alternation of the dynamic signal, and was accurate only if the sent signal was guaranteed to be of the "correct" length. Transients, such as those on series-compensated lines, would cause sent pulses of an irregular pattern, and the arbitrary repair, upon reception, could lead to misoperations. Dealing with channel impairments was one of the weakest points of analog designs.

5. The natural stability of Phase Comparison relies on integrating the coincidence time. This again used to be implemented via timers, which is not an optimum way. Solid-state analog relays could mimic the integrators much better, but their capabilities to control the positive or negative integration during short gaps in the coincidence, and reset, were limited.

These older Phase Comparison relays were designed without extensive simulations, particularly transient simulations. They were conceived assuming the textbook square wave picture. As a result their designs often forced the relay response into such ideal patterns. Steady state bench-testing with no signal distortions or channel impairments was employed to verify such designs. Misoperations in the field with very limited analysis information such as high-speed recordings of power and communication signals, were the only practical means of fine-tuning the designs. This fine-tuning in turn was very limited as all the intelligence was cast in magnetic / electric / electronic circuitries with complex interactions and no convenient means of adjustment. Despite their limitations, early Phase Comparison relays performed very well after fine-tuning to a particular line and carrier. The need for fine-tuning in the field, however, limited acceptance of the principle. Also, because there were virtually no monitoring capabilities for the power and communication signals, some misoperations were difficult to analyze and explain. These challenges can be eliminated when applying the latest generation of microprocessor-based technology. Accurate signal processing, monitoring and recording capabilities, buffering and delaying are key advantages. Early designs of Phase Comparison on digital platforms were less than optimum. Quite often the principle was implemented in the frequency domain, i.e. the waveforms were transformed into phasors, and later transformed back into the time domain of the transmit and receive analog pulses.

The textbook picture of square waves led to some designs using interrupts, i.e. edge detectors to receive the incoming phase information. This made the relay extremely susceptible to noise in the channel. The solution of forcing the response into the textbook pattern led to arbitrary alternation of the true incoming information, with potentially dramatic consequences. The latest designs adhering to the core of the Phase Comparison principle, such as one described in the next section, provide for very accurate implementation with no arbitrary manipulations of any of the processed signals. This purity of approach, combined with high processing accuracy, ensuring similar responses at all terminals on the line, yields fast, dependable and secure protection. Because of exceptional monitoring capabilities these solutions are easy to apply and maintain. Being parts of integrated multi-functional platforms, they become an attractive alternative to directional- comparison and line-differential schemes.

6. Modern Implementations of Phase Comparison

Phase Comparison as a protection method, is naturally a time-domain principle. It can be logically explained and analyzed if implemented as a set of operations on instantaneous signals starting at the local ac currents and received dc voltages encoding the phase information for the remote currents, and culminating at the trip integrators to measure the coincidence time between the operating currents. Early, and still prevailing, implementations of microprocessor-based relays in general, are based on frequency domain processing. This means that instantaneous currents and voltages are first filtered and represented by phasors, i.e. magnitudes and angles, and trip/no-trip decisions are based upon phasors or similar aggregated values. Successful implementations of the Phase Comparison principle on microprocessor-based relays should be based on instantaneous values, not phasors. There are several reasons for this as illustrated in this section, the chief one being about the analog nature of the remote information. The transmitted/received analog signal is an on/off binary signal that encodes the information not on the signal magnitude, but rather on timing with respect to actual continuous time. In addition, this signal is subject to impairments that cannot be alleviated by means of filtering, but rather by manipulations of its shape. It is therefore logical to process the communication signals in the Phase Comparison relay in the time domain, and adjust the reminder of the algorithms to follow the instantaneous approach, not vice versa. The time domain approach follows the approach of the last generation of analog Phase Comparison relays, allowing the possibility of equally good performance. Several improvements to, and other benefits of, this approach, follow naturally as explained below.

6.1. Overall organization of calculations

With reference to Figure 6-1 the core of the phase comparison algorithm is about

- deriving operating currents (block 1),
- mixing the currents into the composite signal (block 2),
- establishing the overcurrent supervision conditions (block 3),
- producing local phase information pulses (block 4),
- solving the two breaker logic, if applicable (block 5),
- converting this local information into transmit pulses (block 6),
- receiving the analog phase information (block 7),

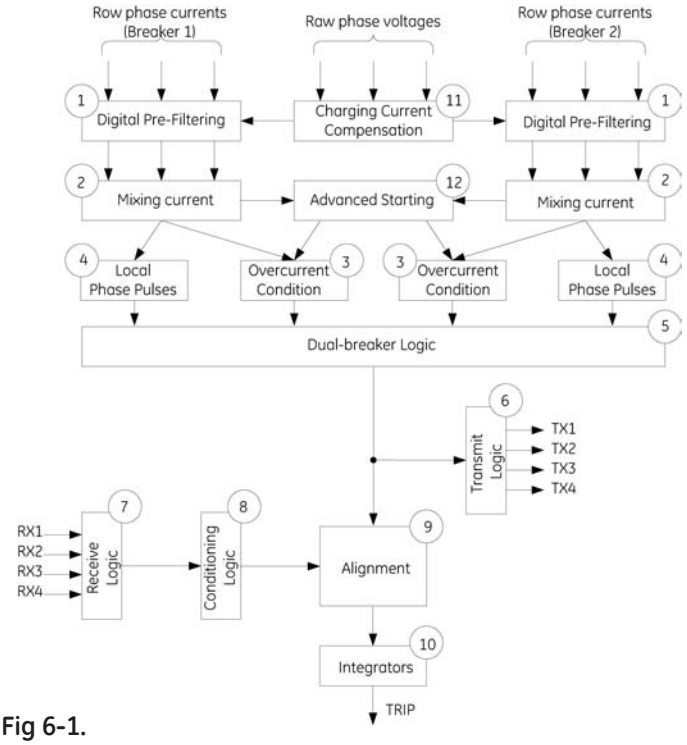


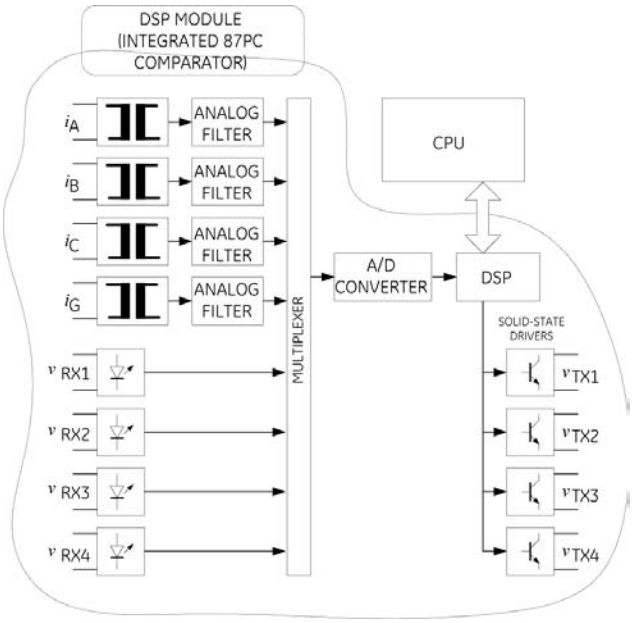
Fig 6-1.
Overall organization of the phase comparison algorithm.

- conditioning the analog phase information for channel impairments (block 8),
- aligning the local and naturally delayed remote phase information (block 9)
- measuring the coincidence time for the trip/no-trip decision (block 10).

Extra operations can be added such as charging current compensation (block 11) or sensitive starting algorithms (block 12).

The above stream of signal treatments naturally lands on the Digital Signal Processor (DSP) of a modern relay. In order to do that it needs access to instantaneous values of the operating quantities. These include local ac currents, and the dc-voltage-coded phase information for the remote line end(s). Both of these signal classes are sampled via the A/D converter and worked with as samples (Figure 6-2).

With sampling rates of 64 or 128 samples per cycle, one could achieve time resolution in the order of 120-250 microseconds or 2-5 electrical degrees. This is sufficient in practical cases, particularly given the other benefits of a digital time-domain implementation. Following the approach of Figures 6-1 and 6-2, the DSP acts as an integrated "87PC comparator". The auxiliary functions such as keying from an open pole condition, current reversal logic, etc. are coded on the main processor of the relay allowing easy integration with other functions and resources of the multi-function relay.



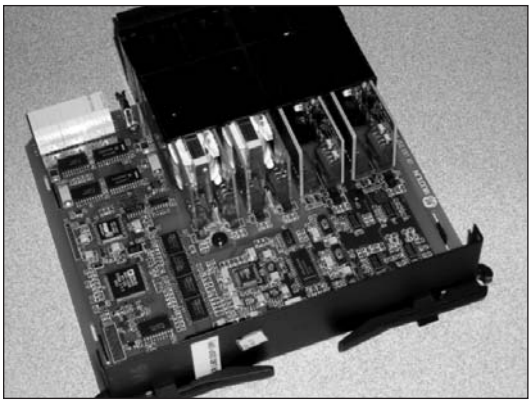


Fig 6-2.
Hardware architecture of a digital phase comparison comparator.

This section focuses on selected aspects of the 87PC comparator residing on a DSP.

6.2. Operating currents

The Phase Comparison principle is naturally immune to transients; – as long as the phase information is preserved, magnitude distortions do not affect the operation even if relatively high. However, under external faults there may be some differences in high frequency noise at various terminals on the line. In addition, severe saturation of a high dc offset component could alter the current polarity information, and thus require the dc component to be filtered out. The saturated CT would effectively "remove" the dc offset from its secondary current, while the accurate CT would preserve it. As a result, saturation can alter polarity information by up to quarter of a cycle, jeopardizing security (Figure 6-3). It is therefore prudent to apply some bandpass filtering to the input currents. The filtering should not be excessive in order to avoid penalizing the speed of relay operation. A Finite Response Filter (FIR) - a weighted average of signal samples in a selected data window - is used for pre-filtering. One particular implementation uses a data window of 1/3 of a cycle, resulting in an extra signal (phase) delay of about 1ms [9].

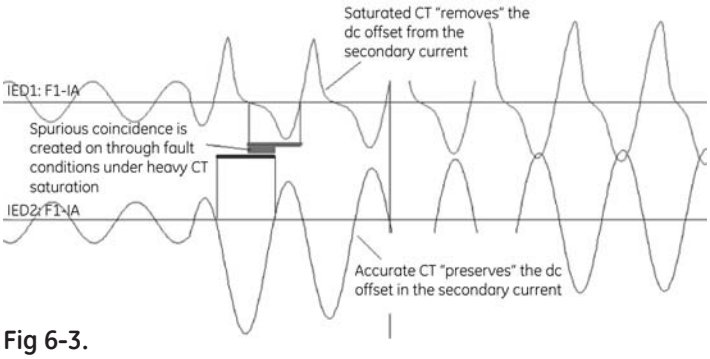


Fig 6-3.
CT saturation under dc offset calls for low-pass filtering of the operating currents.

The pre-filtered instantaneous currents can be used directly in phase-segregated implementations.

In mixed-mode applications they need to be converted into a single composite current. This operation uses symmetrical components and may seem at odds with the time-domain approach. It must be kept in mind, however, that the two mixed mode signals typically used ($3*I_0$ or $I_2 - K*I_1$) are nothing but an aggregating mechanism to shrink the three-phase information into a single analog channel, while preserving sensitivity to all types of faults. As long as this original goal is met, and the steady-state value of the instantaneous operating current matches its phasor expectation, the algorithm is acceptable, transparent to the user, and will work as expected. The neutral current as a composite signal requires nothing but plain addition of the three phase currents. The negative-sequence mode, however, calls for shifting the currents before producing the sequence

components, and ultimately the composite signal. This could be done, without introducing unnecessary delay, by applying a pair of orthogonal filters. Orthogonal filters are two filters that yield phase responses shifted by 90 degrees, and preferably have similar magnitude responses, i.e. filtering capabilities. The two filters are often labeled as direct (D) and quadrature (Q). Their outputs are instantaneous values, but could be treated in a way similar to the real and imaginary parts of a phasor in the frequency domain. One particular implementation of a Phase Comparison relay uses a pair of short-window FIR filters to derive the D-Q components while providing extra transient filtering. Once the D-Q components are obtained, the instantaneous negative-sequence based composite signal ($I_2 - K*I_1$) is created as follows.

ABC phase rotation, phase A as a reference:

$$i_{MIX} = \frac{1}{3}\left(i_{D\_A} \cdot (1-K) + \frac{1}{2} \cdot (K-1) \cdot (i_{D\_B} + i_{D\_C}) + \frac{\sqrt{3}}{2} \cdot (K+1) \cdot (i_{Q\_B} - i_{Q\_C}) \right) \quad (6\text{-}1a)$$

ACB phase rotation, phase A as a reference:

$$i_{MIX} = \frac{1}{3}\left(i_{D\_A} \cdot (1-K) + \frac{1}{2} \cdot (K-1) \cdot (i_{D\_B} + i_{D\_C}) + \frac{\sqrt{3}}{2} \cdot (K+1) \cdot (i_{Q\_C} - i_{Q\_B}) \right) \quad (6\text{-}1b)$$

Technically, the mixed signal is created as a linear combination of the D-Q components of the phase currents (ABC) as illustrated in Figure 6-4.

As explained in section 4 there is a need to shift the reference phase for the calculations taking into account a particular conductor on which the carrier equipment is installed. This shapes the instantaneous value of the operating signal in a way that boosts its immunity to noise expected at the crest values of the voltage in the phase used by the carrier.

Equations (1) are still valid when shifting the reference. The indices must be rotated accordingly ABC® BCA ® CAB. For example, the mixed signal referenced to the B-phase is calculated as:

$$i_{MIX} = \frac{1}{3}\left(i_{D\_B} \cdot (1-K) + \frac{1}{2} \cdot (K-1) \cdot (i_{D\_C} + i_{D\_A}) + \frac{\sqrt{3}}{2} \cdot (K+1) \cdot (i_{Q\_C} - i_{Q\_A}) \right) \quad (6\text{-}2)$$

Note that equations (6-1 and 6-2) are linear combinations of current samples, as long as the operations of pre-filtering and deriving the orthogonal components are linear, as they should be. This guarantees security on external faults regardless of any transients, as long as the hardware/algorithms are the same at all line terminals, as they should be. With both terminals applying the same linear processing, the two mixed currents will always be out-of-phase as waveforms, regardless of their possible distortions and transients.

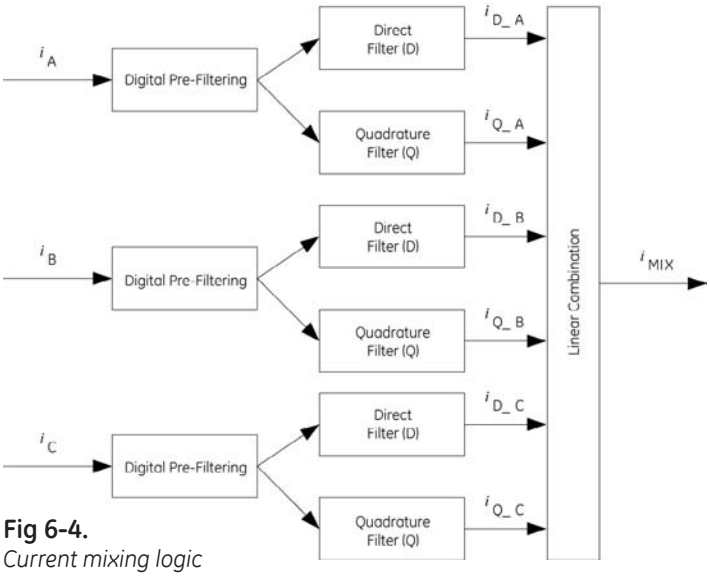


Fig 6-4.
Current mixing logic

Other approaches to creating mixed mode instantaneous signals are possible; the primary goal is to "compress" three signals into a single value while preserving sensitivity to all types of faults. For example, one may use a combination of Clarke components. The (I_2 – K*I_1) signal is used here both for historical and user familiarity reasons.

Figure 6-5 presents a sample plot of the three phase currents (raw) and the mixed-mode negative-sequence current (filtered, thus delayed slightly).

6.3. Overcurrent supervision conditions

Two levels of fast overcurrent supervision are required: fault detection low (FDL) for keying, and high (FDH) for tripping. These conditions are supervisory, and do not therefore have to be very accurate. Instead, they should be fast enough not to slow down the remainder of the 87PC algorithm.

Calculating the quadrature component of the instantaneous operating signal is a natural way produce a fast estimator of the magnitude. The quadrature component to the signal (6-1) is:

$$i_{MIX\_Q} = \frac{1}{3}\left(i_{Q\_A} \cdot (1-K) + \frac{1}{2} \cdot (K-1) \cdot \left(i_{Q\_B} + i_{Q\_C}\right) + \frac{\sqrt{3}}{2} \cdot (K+1) \cdot \left(i_{D\_C} - i_{D\_B}\right) \right) \quad (6\text{-}3)$$

And the fast magnitude is now calculated as:

$$I_{FAST} = \sqrt{\left(i_{MIX}\right)^2 + \left(i_{MIX\_Q}\right)^2} \quad (6\text{-}4)$$

Response of the overcurrent condition to switch-off transients, including current reversal on parallel lines, and heavily saturated CTs, is important. The key design requirement is to keep the FDL and FDH picked up and resetting in a way that ensures both dependability and security in both tripping and blocking arrangements.

From this perspective, in order to boost the magnitude on heavily saturated CTs, the RMS component is calculated as follows (on a sample-by-sample basis):

$$I_{RMS(k)} = \sqrt{\frac{2}{N_1} \cdot \sum_{p=0}^{N_1-1} \left(i_{MIX(k-p)}\right)^2} \quad (6\text{-}5)$$

Where N_1 is the number of samples per cycle (64).

The magnitude estimator combines the fast estimator (6-4) for accuracy, the RMS value (6-5) for dependability on CT saturation or other severe transients, and the waveform peak for speed:

$$I_{AUX} = \max\left(I_{RMS}, I_{FAST}, 0.85 \cdot abs\left(i_{MIX}\right)\right) \quad (6\text{-}6)$$

The final estimator tracks the maximum value of the auxiliary signal (6-6) in a window of the last half-cycle, for extra security. When checking the FDH flag (tripping supervision) the algorithm

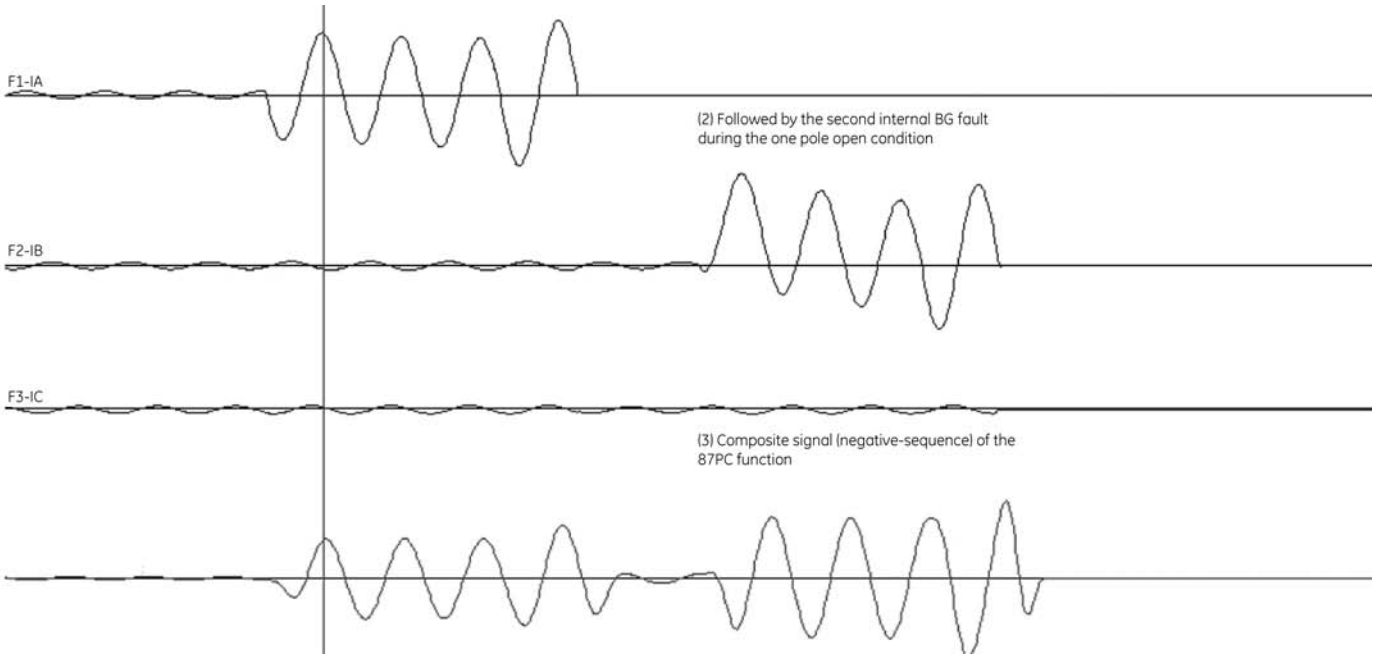


Fig 6-5.
Example of mixing current operation (relay COMTRADE record).

applies an overcurrent condition using the operating quantity (6-6) with the user-defined threshold and a fixed hysteresis. When checking the FHL flag (keying) the algorithm is built in a way that makes sure a "phase" pulse, once started, will get finished regardless of the magnitude measurements within the duration of the pulse. This is done for security of blocking schemes, where it is desirable to maintain the full duration of the last blocking pulse before ceasing transmission. This response is achieved by virtually sealing the FDL flag with the positive or negative pulse upon drop-out of the raw magnitude condition.

Figure 6-6 shows an example of the response of the magnitude estimator for the case of Figure 6-5. The FDL and FDH flags pick up in about 2.8ms.

6.4. Local phase pulses

The local operating current is converted into "phase" pulses. It is important to realize that the operation is nonlinear, erasing almost all information contained in the magnitude of the signal, and presenting exclusively the phase information by encoding it in the on/off pulses signifying polarity of the operating signal.

This polarity is preserved with respect to the universal "analog" time. This is one of the key advantages of the Phase Comparison principle even when implemented digitally: no synchronization is required between the individual relays of the 87PC scheme. The raw LOC-al pulses (Positive and Negative polarity) are produced while disregarding the FDL and FDH flags. The fault detector flags are used in the dual-breaker, key and trip logic. The raw pulses are calculated as follows:

$$LOC_{P\_RAW} = i_{MIX} > \alpha \cdot \sqrt{2} \cdot C\,T_{pu} \quad \text{(6-7a)}$$

$$LOC_{N\_RAW} = i_{MIX} < -\alpha \cdot \sqrt{2} \cdot C\,T_{pu} \quad \text{(6-7b)}$$

Where α is a factory constant (a small fraction of the CT rated current, 2-5%).

The "phase" pulses represent the signal polarity with the accuracy of one sampling period. For example, 250 microseconds or 5.2deg when sampling at 64s/c.

The two pulses are marked here as "raw" as they need more conditioning before they can be used for keying or tripping.

6.5. Dual breaker logic

As explained in section 4, the Phase Comparison principle would face security problems when fed from externally summated currents in two-breaker applications. In order to maintain the excellent immunity to CT saturation of the "original, single-breaker" Phase Comparison principle, one must process the two currents individually and use both the phase and magnitude information to detect the through fault condition. The dual breaker logic consolidates two pieces of information: fault detector flags signaling the rough current levels, and "phase" pulses signaling current direction.

The fault detector flags are OR-ed between the two breakers (breakers 1 and 2):

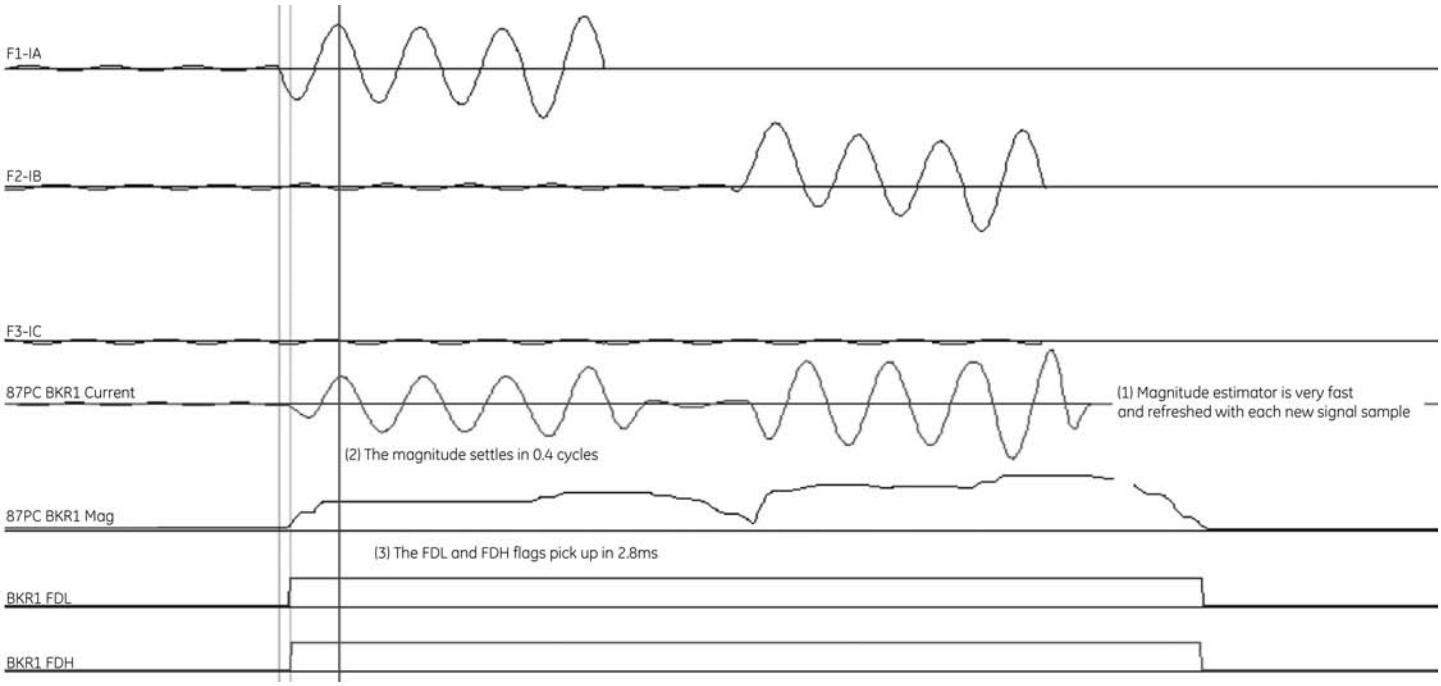


Fig 6-6.
Sample response of the overcurrent supervision algorithm (relay COMTRADE record).

$$FDL = FDL_1 \ \ OR \ \ FDL_2 \ , FDH = FDH_1 \ \ OR \ \ FDH_2 \qquad (6\text{-}8)$$

The rationale behind this is that regardless of which breaker (or breakers), carry a current; the elevated current condition (FDL) should be declared to signal either permission or blocking as per the scheme type and fault location. Similarly, with the trip supervision condition (FDH).

It is the "pulse" combination logic that ensures security and dependability. In this respect a distinction must be made between tripping and blocking schemes.

For tripping (permissive) schemes, a positive polarity is declared for the terminal if one breaker displays positive polarity when its FDL flag is set, while the other breaker either does not show the negative polarity or its FDL flag is dropped out (Figure 6-7a). This is similar to a Hybrid POTT scheme when a given terminal sends a permissive signal unless it is restrained locally by a reverse fault condition. Note that this logic displays the following desirable features:

- Under through fault conditions, when both currents are elevated and out of phase, the positive pulses in one breaker get "erased" by the negative pulses in the other breaker.
- Under reverse or forward fault conditions, with one breaker opened or its current below the lower fault detector, the logic behaves as for a single breaker. The elevated current in the closed breaker drives the response of the scheme. In this way a small out-feed can be tolerated and will not impair the dependability of the scheme.
- Under forward fault conditions, with both breakers closed and both currents above the fault detection level, the two-breaker logic effectively creates a coincidence pulse out of the two individual pulses (logical AND). This corresponds to a multi-terminal Phase Comparison where all individual current pulses are AND-ed before feeding the trip integrators.

The above logic is used for keying in permissive schemes, and regardless of the scheme type for derivation of local pulses, sent to the trip integrators.

Transmission logic for the blocking logic follows a different reasoning (Figure 6-7b). Here, a blocking action must be established if any of the two breakers sees a reverse direction. It must be kept in mind that as the positive and negative pulses do not necessarily complement each other, one must not substitute not(positive polarity) = negative polarity.

Figure 6-8 shows a sample response of permissive logic to a through fault condition at a two-breaker terminal. The terminal does not produce permissive pulses and inhibits as expected.

Figure 6-9 shows the case of an internal fault with strong feed from both breakers.

6.6. Transmit logic

The local phase pulses as developed in the previous section, drive the transmit output of the relay. The speeds of the outputs are controlled via solid-state electronics, and can be wetted individually from different battery systems, if required.

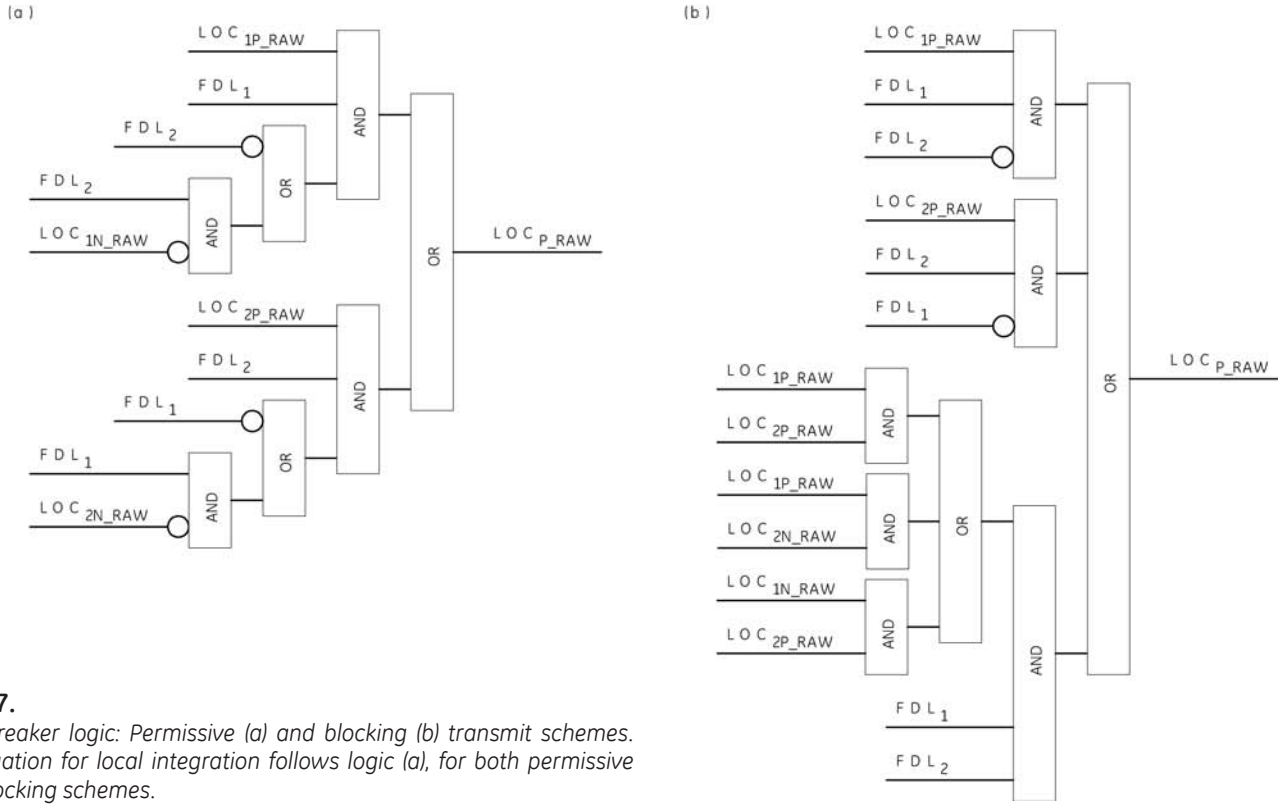


Fig 6-7.
Dual-breaker logic: Permissive (a) and blocking (b) transmit schemes. Aggregation for local integration follows logic (a), for both permissive and blocking schemes.

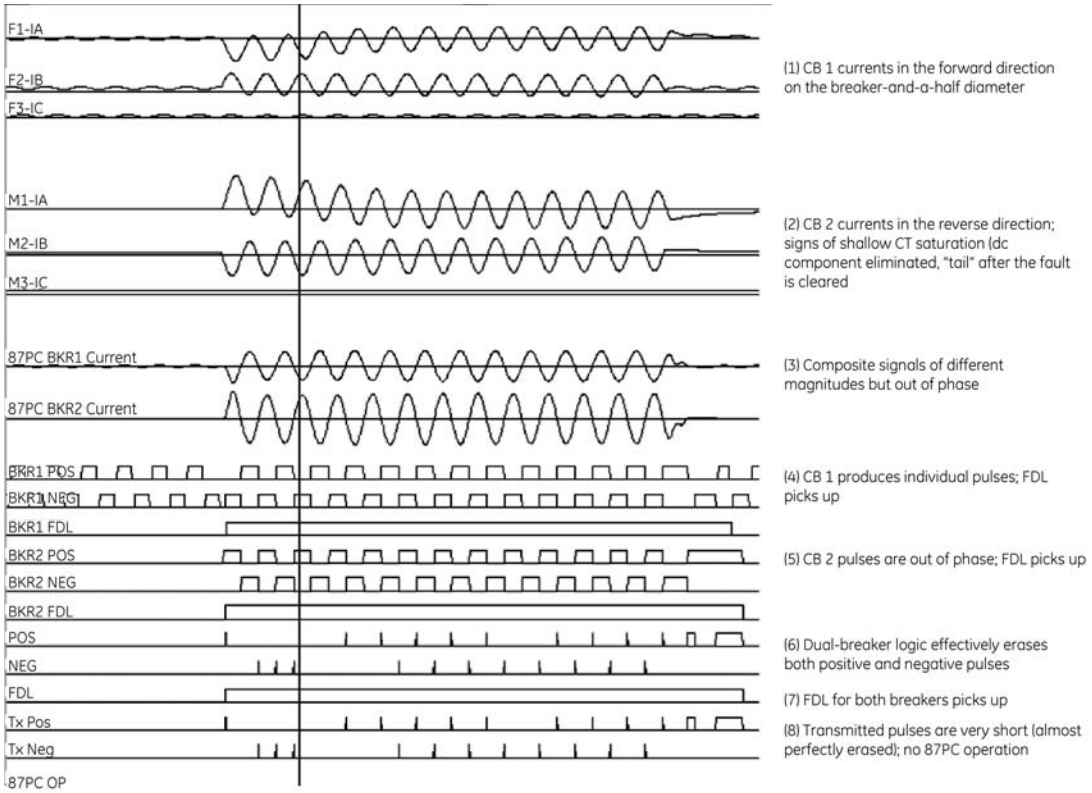


Fig 6-8.
Illustration of the dual-breaker logic: permissive, dual-comparison scheme, through fault condition (relay COMTRADE record).

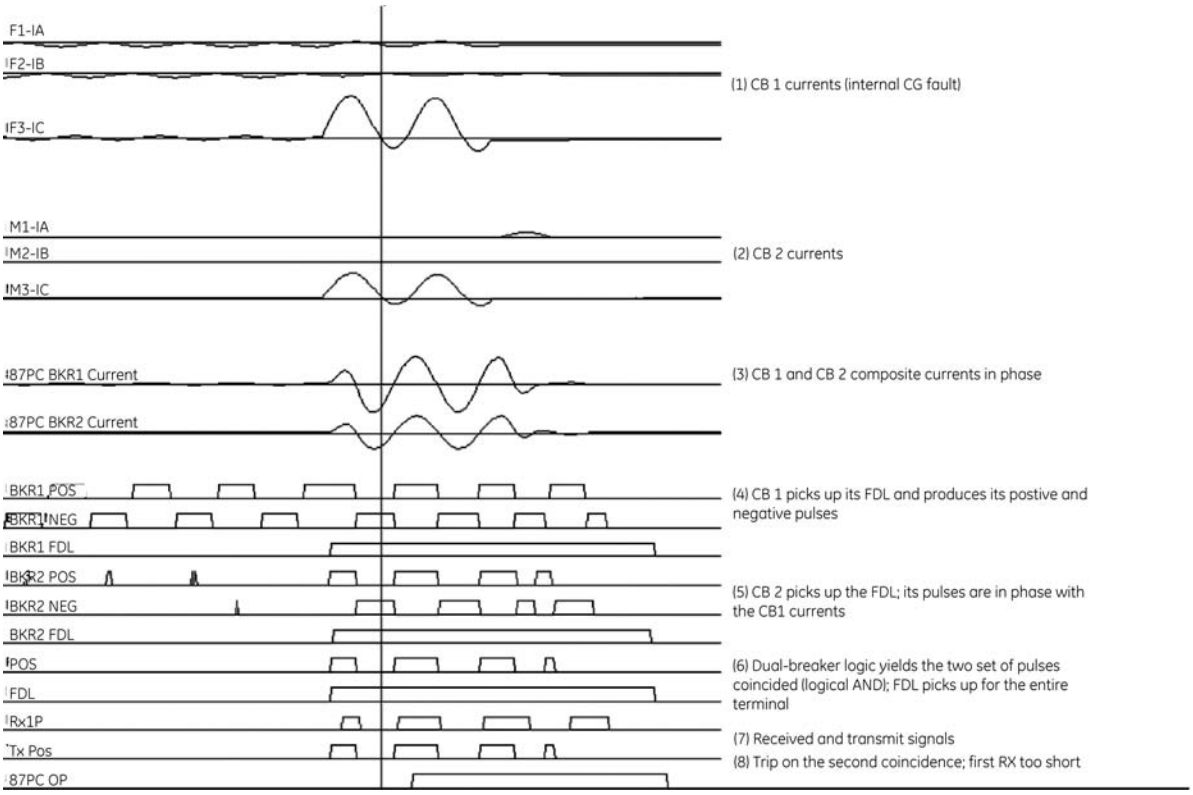


Fig 6-9.
Illustration of the dual-breaker logic: permissive single-comparison scheme, internal fault condition (relay COMTRADE record).

Up to four transmit channels are available to support the following schemes and combinations thereof:

a. Single/dual comparison.
b. Two/three terminal.
c. Mixed-mode/phase-segregated.

A provision is necessary to force a continuous key under certain conditions such as open pole, weak feed, Breaker Fail trip, to force the remote relay to trip assuming it sees the fault, etc.

It is a simple fact resulting from the basic principle of operation, that the transmit pulses (marks and spaces) are of different lengths under transients. The algorithm should not artificially alter such patterns to force them into a textbook case of regular half-cycle pulses.

For example, during current reversal (fault direction opposite to the pre-fault load), the current may get reversed generating a short first pulse. A dc offset component will make pulses of certain polarity longer compared with those of the opposite polarity. It is safe to preserve these natural patterns, comparing what actually happens to the polarity at each terminal, and let the very core of the principle work towards security and dependability.

The communication equipment is expected to transport such signals unaltered, other than the unavoidable delay, to the remote terminals. Channel impairments will happen and need to be dealt with at the receiving relay as described below.

6.7. Receive logic

The received pulses may be distorted in a number of ways. Some of those distortions must be filtered out, and some of them should be left as received (their rectification is neither necessary nor safe).

The received information is delivered from the carrier or other receiver as a dc voltage. In prior generations of relays, the input for this signal was a binary or status circuit that reported only a debounced or filtered true or false indication to the following circuits or microprocessor.

In the newest design, this signal is sampled synchronously with the local ac signals through the same A/D converter controlled from the same S&H signal (Figure 6-2), and at the same high sampling rate. In this way both pieces of information (local ac currents, and remote phase signals) are automatically aligned in time, and the analog value of the receiver output status signal can be used to achieve the closest approach to the core Phase Comparison operating principles.

The analog voltage signals are processed on an instantaneous basis, the first step being applying a threshold to derive a Boolean on/off flag.

The first and most obvious distortion in the received signal is a time delay added by the communication channel. This must be corrected by buffering all the pulses to be aligned, for time differentials with respect to the slowest remote channel. Assume for example a 3-terminal application with the two remote terminals delayed by 3ms and 5ms, respectively. The local pulses must be buffered and delayed by 5ms, pulses from terminal 1 must be buffered and delayed by 2ms, and pulses from terminal 2 must be passed with no delay.

Using digital technology such delays can be accomplished in a precise and straightforward way - buffering the signal sample values in a delay queue. Analog technologies may have difficulty delaying these signals in a precise way, particularly if the signals are of variable length and have other impairments.

The second possible distortion is high frequency noise embedded on the mark or space pulses. which should be left unaltered. The receiving relay has no reliable information as to the real value of the received information, and will not therefore alter it based on any assumptions.

The Phase Comparison algorithm has a well-understood security margin due to the averaging action of the trip integrators. The integrators deal with this kind of noise, yielding a predictable response that is transparent and easy to grasp by the user.

Figure 6-10 shows a possible case of such distortion influences. With respect to the time alignment operation, the digital implementations buffer and reproduce the pulses as received. In the analog world this operation corrupts the information, given the fact that the individual on and off states are of variable length. Channel impairments are not the only reason for accurate buffering and alignment. Figure 6-11 shows an

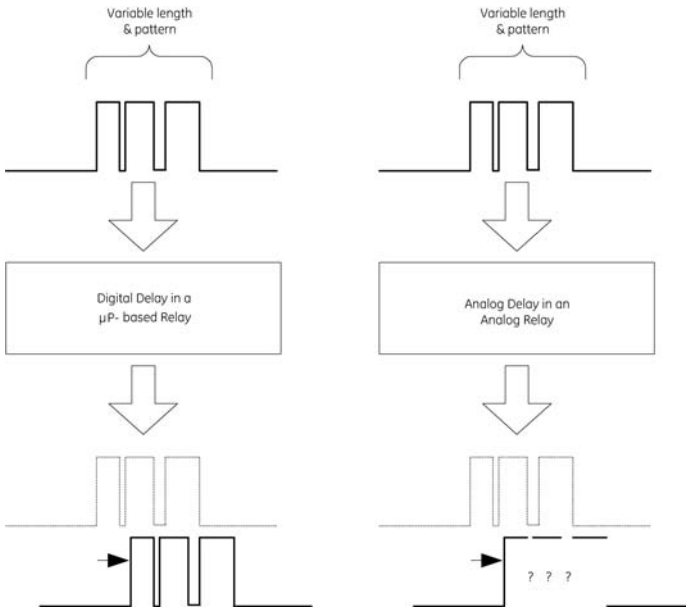


Fig 6-10.
Illustration of time delay of a chattering pulse: digital vs. analog. Quality of reproduction of an impaired "mark" may be affected when delaying for alignment in the older analog schemes.

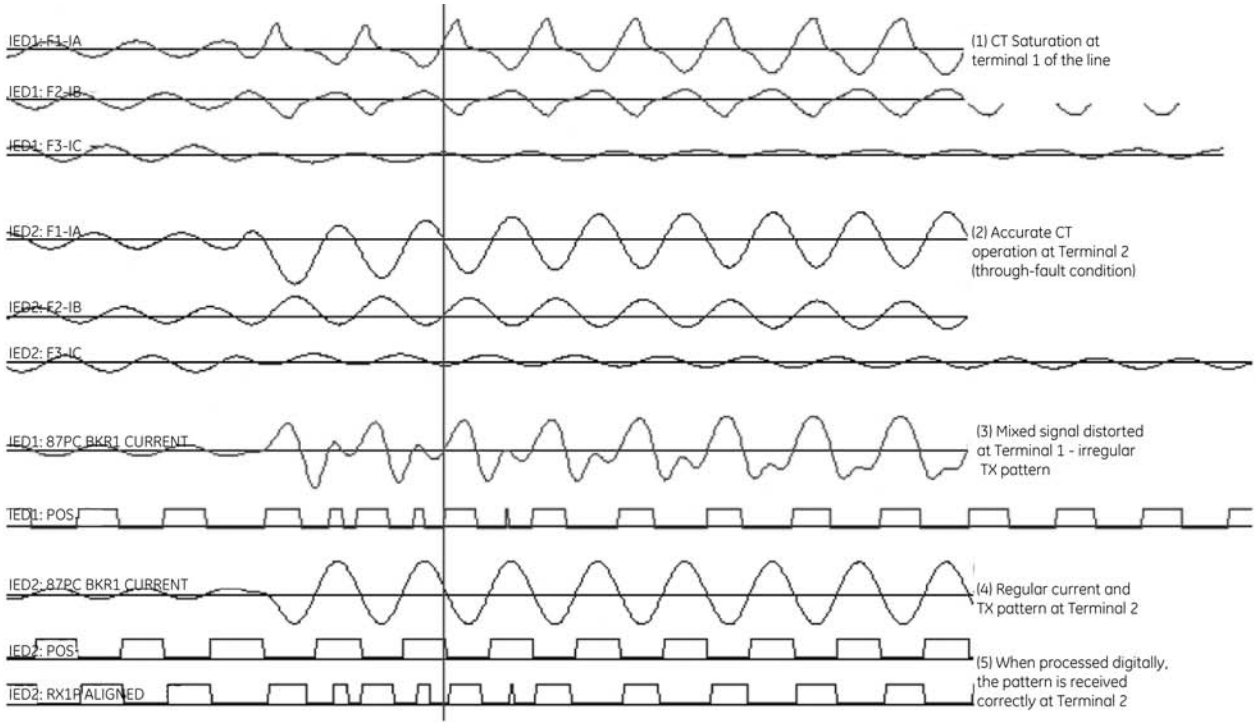


Fig 6-11.
Transmit pulses could be irregular due to CT saturation. Exact reproduction of the transmitted information at the receiving relay when delaying for alignment is critical for performance of the scheme.

example of a mixed-mode 87PC operation under severe CT saturation. The operating signals become distorted due to CT errors, and may produce short irregular pulses.

These pulses are not a problem as long as they last less than the coincidence timer. However, if "repaired" or distorted by the delay and alignment logic, they may exhibit unpredictable behavior. Digital delay introduces no errors, producing solid scheme performance.

The third type of distortion is pulse asymmetry. Modern carrier sets claim to be free of this problem, but historically it has been observed that either the mark or the space signals have been extended at the receiving end, compared with the originally sent signal. Distinction between the delay and asymmetry is relatively straightforward; if the rising edges and the falling edges of the transmit and receive signals are spaced by the same period of time, one deals with a straight delay.

If the spacing is different between the rising and falling edges, pulse asymmetry takes place on top of the delay. In this case, one of the numbers is labeled as a delay, and the difference with respect to the other number is labeled a pulse asymmetry. Both need to be entered as settings in order to deal with this distortion.

Figure 6-12 shows two cases of this channel distortion. In the case of an extended mark, the falling edge must be shifted forward in time (accelerated). In the case of an extended space, the rising edge must be advanced. If not corrected, pulse asymmetry renders the system unusable for distortions longer than quarter of a power cycle.

This particular problem shows the advantage of modern DSP technology. Assuming that the signal may be impaired by short-term noise, it is very difficult to perform this correction accurately in the analog world. Digitally, the compensation works as follows:

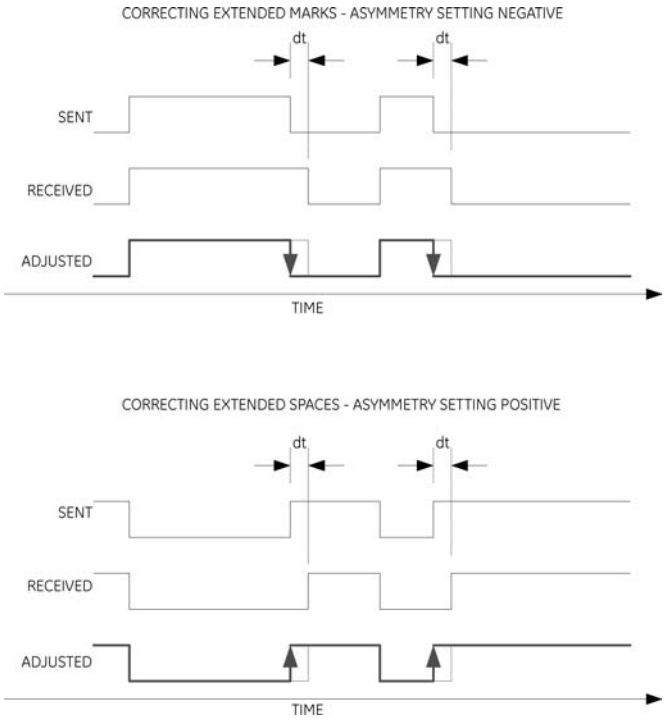


Fig 6-12.
Pulse asymmetry: phenomenon and correction (channel delay not shown for simplicity).

The entire algorithm of the Phase Comparison is delayed by the pulse asymmetry setting (a few milliseconds). This requires our ability to "go back in time" and adjust the received information after seeing the impaired edge. First, it is confirmed that the edge was actually subjected to pulse asymmetry.. Secondly, the algorithm shifts this edge by the amount of the pulse asymmetry setting. In this way the original pulse is passed unaltered with the exception of exact and explicit adjustment of the edge in question.

Digitally this operation is a series of simple manipulations on data buffers. In the analog world, when accomplished with timers, this operation may alter the original information and lead to problems. In practice the extra delay in processing the data is shorter, unless it is the slowest remote channel that is affected by the pulse asymmetry.

Otherwise, the already introduced delay to "wait" for the slowest channel works towards facilitating this feature. Figure 6-13 illustrates the alignment algorithm. The figure shows local current, received RX voltage, and the remote pulse aligned with the local pulses accounting for the channel delay setting.

Being communication-dependent, a Phase Comparison relay should treat information delivered from the remote terminals with the same criticality as the local ac currents. This includes monitoring for troubleshooting purposes, accountability, and continuous improvement capability for products and installations. Modern microprocessor-based Phase Comparison relays that sample their binary dc input voltages for analog level at the same high sampling rate as they do for analog signal inputs provide great analysis tools - they include all the measured and derived instantaneous signals in their oscillographic records (COMTRADE files).
These include flags driving transmission, received dc voltage, local ac currents, and all relevant instantaneous signals leading towards the trip/no-trip condition. Having four receive channels, it is even possible to loop back the transmit voltages to monitor both the signal connected to local carrier equipment, and that received at the remote location (see Figure 6-14).

Figure 6-15 shows an example of the monitoring capabilities by depicting the received voltage as an analog signal sampled by the relay and zooming-in on minor distortions in this signal.

6.8. Integration and coincidence timing

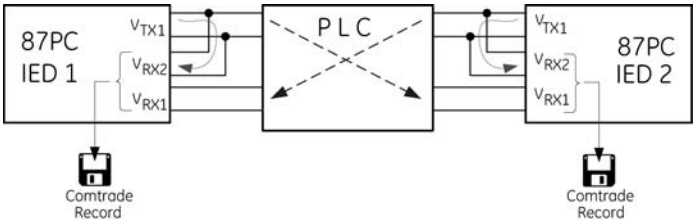


Fig 6-14.
Using spare RX channels (RX2) for complete high-resolution carrier/relay monitoring..

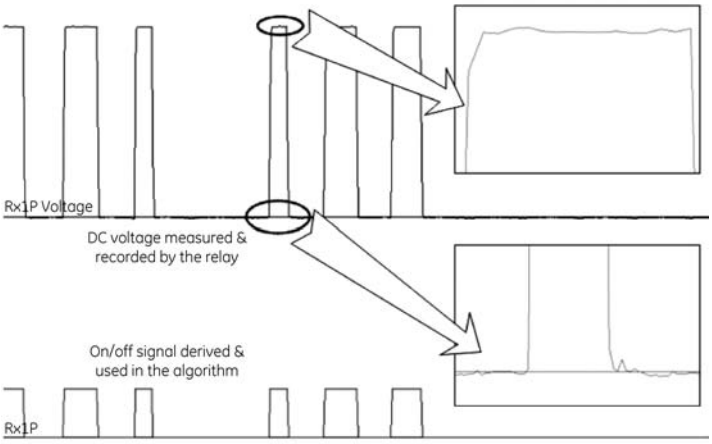


Fig 6-15.
Example of high-resolution carrier/relay monitoring.

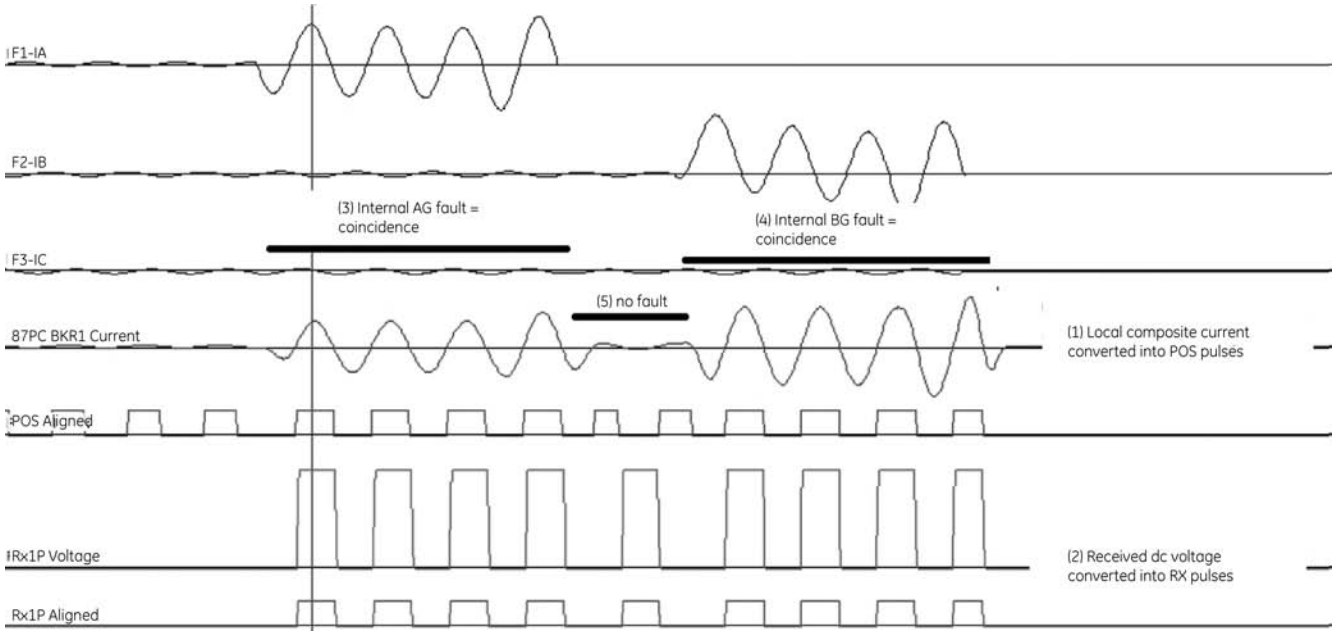


Fig 6-13.
Illustration of the alignment logic (relay COMTRADE record).

Section 4.3 above explained coincidence timing at the top application level. Here we explain exactly how to achieve this timing in the most effective way.

After all the local and remote pulses are aligned and conditioned, a coincidence condition is established as per the number of terminals and type of the scheme (tripping vs. blocking). For example, for a 3-terminal permissive scheme the condition becomes:

$$X = FDH \ AND \ LOC \ AND \ REM_1 \ AND \ REM_2 \qquad (6\text{-}9)$$

The above is executed for positive polarity in single-comparison schemes, and independently for positive and negative polarities in dual-comparison schemes.

The coincidence condition drives an explicitly implemented integrator (summator). In one particular application the integrator counts down by 10 units if the coincidence input is in logic 1; counts down by 5 counts if the coincidence input is in logic 0 momentarily; and counts down by 20 if the input is in logic 0 for longer periods of time. This brings extra security under chattering inputs, allows an eventual trip in a clear situation, and provides full re-set of the integrator before the next coincidence period.

The output of the integrator (or two integrators in dual-comparison schemes) is compared with the coincidence timer setting yielding the final trip/no-trip flag.

Figure 6-16 shows an example of the coincidence integration for an internal fault as recorded in a Comtrade file by the relay under test.

6.9. Charging current compensation

As explained in section 4, charging current leaking from a long line during through fault conditions shifts the terminal currents toward each other, jeopardizing security and/or calling for increased coincidence timer setting, thus hurting the sensitivity/dependability of the scheme.

This obstacle can be alleviated by applying charging current compensation. Based on the zero- and positive-sequence capacitive shunt impedances of the line, the relay calculates the line charging current based on the voltage signals, and uses it to compensate the measured currents.

The following aspects make this approach a good approximation rather than an exact calculation:

1. It is not known at a given terminal how much capacitive current is supplied through this terminal versus other terminals. Typically schemes assume an equal split between all line terminals. This is of secondary value; in most cases good correction takes place as long as the total current subtracted is close to the actual value, regardless of the split between or among the terminals.

2. The voltage profile along the line is not flat, and capacitance is distributed along the line. The relays use lump capacitance models and terminal voltages. This approximation is relatively close as during external faults the voltage profile is approximately linear along the line length.

3. The capacitive current contains high frequency noise. The relays measure the frequency spectrum up to a designed upper frequency limit.

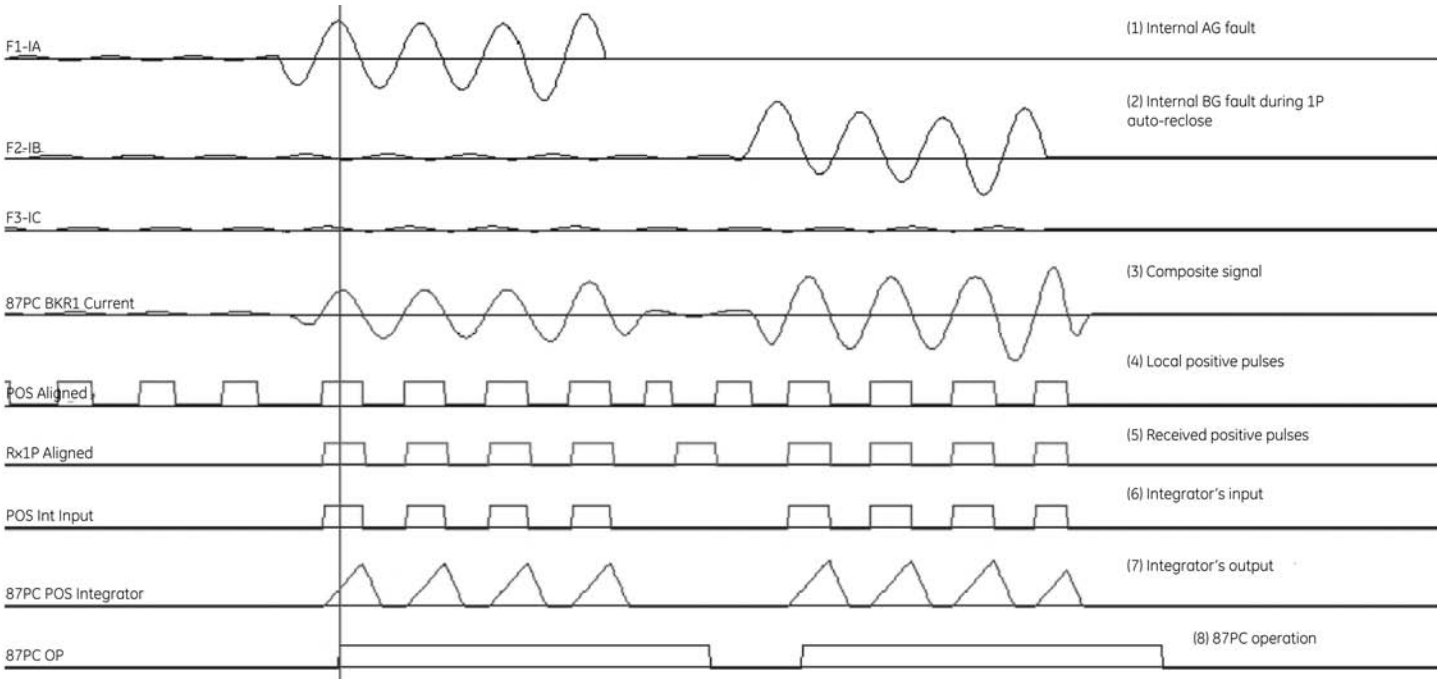


Fig 6-16.
Illustration of the trip integration logic (relay COMTRADE record).

One particular approach calculates the charging current on a per phase basis, as an instantaneous signal, and subtracts it from the measured currents before any other operation geared toward Phase Comparison protection. This approach was first introduced on line-current differential relays [10] and was proved to reduce the impact of the charging current approximately five- to tenfold in field installations.

The operation is straightforward and is based on a numerical derivative of voltages (Dv_A, Dv_B and Dv_C). The instantaneous charging current is calculated as:

$$\begin{bmatrix} i_{qA} \\ i_{qB} \\ i_{qC} \end{bmatrix} = \begin{bmatrix} \alpha & \beta & \beta \\ \beta & \alpha & \beta \\ \beta & \beta & \alpha \end{bmatrix} \begin{bmatrix} Dv_A \\ Dv_B \\ Dv_C \end{bmatrix} \quad (6\text{-}10)$$

where:

$$\alpha = \frac{1}{3}\left(\frac{2}{X_1} + \frac{1}{X_0}\right) \quad \text{and} \quad \beta = \frac{1}{3}\left(\frac{1}{X_0} - \frac{1}{X_1}\right) \quad (6\text{-}11)$$

Calculating the charging current as an instantaneous value is a prudent approach given the fact that the described phase comparison relay works in the time domain as well. In addition to removing the leaking current, charging current compensation implemented in the time domain equalizes the high frequency components among the line terminals, making the application more secure on cables and long overhead lines.

Again, as explained in section 4, inductance of the compensating shunt reactor is not a negative capacitance. The relay should be set to compensate for the total charging current, while the reactors should be excluded from the relay measurements by external paralleling of the line and reactor CTs.

6.10. Advanced starting algorithms

Some lines may exhibit persistent content of the negative-sequence current and/or voltage during normal operation. Untransposed EHV lines, or lines supplying traction circuits are good examples. It is not desirable to continuously key Phase Comparison systems. In such cases advanced starting methods are required. Different methods could be used, one of the most popular being based on the increase in negative sequence voltage augmented with a small amount of negative-sequence current:

$$START = \Delta\left|V_2 + Z_{offset} \cdot I_2\right| \quad (6\text{-}12)$$

This approach is similar to concept of an offset impedance for the negative-sequence ground directional overcurrent elements [11]. Operating principle (6-12) can be easily implemented in the time domain as illustrated by equations (6-1) through (6-4).

Other advanced approaches include changes in sequence currents and/or voltages, impedance, or combinations.

6.11. Other advanced phase comparison features

Other advanced functions can be implemented taking advantage of digital technology. Practically considered examples are:

Automated measurement of the channel delay.
It is possible to initiate a loop-back test under normal system conditions. By measuring the difference between the sent and received pulses, each relay in the scheme can estimate the actual channel delay. For short lines with negligible charging current, the channel delay can be calculated from the misalignment between the local current pulses and the received pulses, assuming that the remote relay keys test messages.

Automated check-back.
Under normal system conditions, a relay could initiate transmission and modulate the analog signal to exchange small amounts of information. Ability to abort in cases of system faults, is a key to successful deployment. This feature could replace the guard signal when this is not available. Furthermore, it provides a more comprehensive communications check from one center of relaying intelligence in the microprocessor at one end, to its companion at the other line terminal. This covers all the links in the chain of communication, not just the carrier part of the system.

Automated measurement of the positive-sequence charging current.
By measuring the misalignment between the local and remote pulses under through load conditions, the relays could estimate the amount of positive-sequence charging current.

6.12. Modern multi-function platforms

While focusing on the performance and application benefits of a modern pure Phase Comparison implementation as described above, users should be aware of the synergistic benefits of the many other functions that are integrated in the latest generation of microprocessor relays.

It is interesting to see how multifunctional relay evolution has enabled the new Phase Comparison approach. Consider the earlier-generation microprocessor line relays of either the directional comparison/distance or the current differential type. The affordable digital hardware elements available at that time, limited the number of analog input channels that could be sampled, as well as the sampling rate. Accordingly, there were three or four current input channels for measuring line currents only, and three inputs for line voltage.

Many of these early multifunctional products included breaker failure protection and automatic reclosing with line protection. However, these could only be used if a single breaker fed the line. More common breaker-and-a-half and ring-bus connections had two breakers feeding the line; each breaker had its own CTs and the CT circuits were paralleled external to the line relay. The internal breaker failure and reclosing functions could not be used, and the user had to install separate breaker failure and reclosing relays on a separate breaker panel.

In the latest relay generation, the drive is to increase the functions in each relay package in order to reduce cost, panel and floor space, and wiring. A major breakthrough has been the addition of voltage and current input channels, and the requisite internal processing horsepower, to handle substation current differential relaying (bus and transformer protection with a separate input for each differential zone CT set), or to separately connect the currents from the CTs of each breaker feeding a line to be protected. The line current is developed by mathematical summation or processing of the individual breaker current inputs internal to the line relay.

Separating the CT inputs, adding bus voltage inputs, and upgrading the accuracy and bandwidth (sampling rate) of each input, brings the following functions to benefit the user:

1. The breaker failure function is provided as a separate and independently operating function for each breaker, using the appropriate currents for that breaker. Each relay thus has two or more instances of the breaker failure logic. These can be used in the breaker-and-a-half or ring-bus configurations that are ubiquitous in transmission substations, eliminating the separate breaker panels and relays.

2. Two redundant line protection systems are installed on bulk transmission lines to meet reliability design requirement of no single point of failure that can completely disable an important protective function. In the new generation of relays, the breaker failure protection for two breakers now resides in the box with the line protection and might be disabled by the same single failure that disables the line protection in that box. However, these breaker failure functions are all duplicated in the redundant line relay, so the single-failure risk is eliminated. Furthermore, the adjacent-zone redundant relays (line, bus, or transformer) may also have additional instances of failure protection for the breaker that separates the zones. So there is more redundancy than was ever available in the past – from two to four breaker failure instances – even as the count of relay boxes is reduced.

3. Automatic reclosing is also included as an independently operating function for each of the breakers, and the relay can develop closing supervision signals of dead line/live bus, live line/dead bus, and synchronism from the connected line and bus voltages for each breaker. Redundant line relays can exchange status reports to enable only one reclosing function at a time for a given breaker.

4. If the relay is integrated with a substation automation system using an Ethernet or serial LAN, it is able to provide accurate and timely metering measurements of individual breaker currents, bus and line voltages, as well as line Watt and VAr flows, to the substation communications concentrator. It can replace conventional informational meters, RTUs and transducers, and can also display these independent metered values on its panel.

5. As the measurements for the individual breakers are separated, the control outputs are separated as well. Thus, the relay can serve as the breaker or switch control conduit for SCADA, or for local operators at a substation console, all via the LAN. The relay panel controls can be used for backup, eliminating separate panel switches. It is critically important to recognize the value of performing these control operations through the relay; doing so verifies that the relay is able to trip the breaker for faults without performing a local maintenance-style tripping test.

6. With individual current inputs captured with high sampling rates, and with greater fault record memory capacity, the relay can capture oscillographic data as good as or better than that captured by a free-standing oscillograph. Again, there are redundant sources of individual measurements that were not available in the past. The oscillographic data is also available over the substation integration LAN for local or remote access by operators, or non-operational users (engineering or maintenance).

Taking advantage of these functional capabilities in the relays, new substation control house design can eliminate more than half of the relay unit count and panel or floor space required, along with masses of redundant or daisy-chained wiring. Information and control interfaces from the relays via LAN integration can serve the full range of utility business enterprise users and needs.

With these individual high-bandwidth signal inputs designed into the relay for all of these integration–oriented reasons, the relay now also has the platform of information to carry out Phase Comparison relaying with more pure and secure calculations than were ever possible before. Critically important to the effectiveness of the new 87PC methods are as follows:

1. Separated CT inputs from multiple breakers feeding the line, enabling proper handling of bus through faults at a line terminal as explained in Section 4.8.
2. Developing comparison signals from each breaker separately, and combining with the logic explained in Section 6.5, thus eliminating security risks caused by combining the breaker currents before calculating the comparison signals.
3. Treating channel receiver inputs as analog signals and sampling the waveform at high speed, enabling processing of the receiver outputs that overcomes misbehaviors of the channel that fooled earlier Phase Comparison implementations, as explained in Section 6.7.

7. Conclusions

Today's thinning ranks of protective relay engineers are seeking designs that cut workload by simplifying the engineering and maintenance of system protection. They are driven by management to reduce costs while at the same time meeting more stringent system security requirements. The task is easiest if:

1. there is a standard solution that works well for most or all protection needs, from critical bulk transmission lines (including series compensated lines) to multiterminal subtransmission applications

2. the economics allow the user to make a business case for standardizing on this design, which makes it easy to engineer new projects and maintain the consistent installed base of relays

3. the protection standard is as easy to apply in dense urban networks as for lines operating over long distances

4. the scheme is easy to set, with settings not critically dependent on evolution of the power network as new lines or cogenerators are installed, or as the system is switched to unusual operating states. This minimizes the labor required to run coordination studies and update relay settings in the field

5. it is not vulnerable to false tripping during stressed system conditions or recoverable swings, which could contribute to a major blackout

6. the selected standard system provides the suite of information reporting and control facilities to support modern LAN-based substation and enterprise integration of relays

The authors have explained in detail how a new, pure implementation of the long-standing phase comparison protective relaying scheme meets all of these criteria. It is the ideal choice as a standard pilot protection scheme for most utilities.

Table 1 summarizes the salient evaluation points among phase comparison (87PC), line current differential (87L), and directional comparison pilot relaying schemes (DC).

8. References

[1] IEEE Standard 643 - 2005, Power Line Carrier Application Guide.

[2] Sanders, M.P. and Ray, R.E., Power Line Carrier Channel & Application Considerations For Transmission Line Relaying, 50th Protective Relay Conference, Georgia Tech, May 1996 (also available at http://www.pulsartech.com/pulsartech/docs/C045-P0597.pdf).

[3] IEEE Power System Relaying Committee Special Paper of Working Group H9, Considerations In Applying Power Line Carrier For Protective Relaying, available at http://www.pes-psrc.org/h/H9/h09.html, final paper link.

[4] Wilkinson S., "Series Compensated Line Protection Issues", GE Publication GER-3972 (www.multilin.com).

[5] Kasztenny B., Voloh I., "Application of Distance and Line Current Differential Relays in Breaker-and-a-Half Configurations", 2005/6 IEEE T&D Conference and Expo, Dallas, TX, May 2006.

[6] Elmore W., Pilot Protective Relaying, Marcel Dekker, 2000.

[7] Kasztenny B., Campbell B., Mazereeuw B., "Phase Selection for Single-Pole Tripping – Weak Infeed Conditions and Cross Country Faults", Proceedings of the 27th Annual Western Protective Relay Conference, Spokane, WA, October 24-26, 2000.

[8] Kasztenny B., "Distance Protection of Series Compensated Lines – Problems and Solutions", Proceedings of the 28th Annual Western Protective Relay Conference, Spokane, WA, October 22-25, 2001.

[9] L60 Phase Comparison Relay (Instruction Manual), GE Publication GEK-106412, 2005 (www.GEMultilin.com/manuals).

[10] L90 Current Differential Relay (Instruction Manual), GE Publication GEK-113210, 2005 (www.GEMultilin.com/manuals).

[11] Kasztenny B., Sharples D., Campbell B., Pozzuoli M., "Fast Ground Directional Overcurrent Protection–Limitations and Solutions", Proceedings of the 27th Annual Western Protective Relay Conference, Spokane, WA, October 24-26, 2000.

	87PC	87L	DC
Measurement quantities	Current comparison only	Current comparison only	Current and voltage; susceptible to misoperation due to voltage loss or poor CVT transient response.
Line loading response	None	None	May trip on load – need load encroachment measurement and setting
Disturbance, swing or OOS response	Immune	Immune	May trip for stable or unstable swings – need OOS detection and trip blocking measurements and settings.
Synchronization of comparison values (microprocessor-based relays)	Not required	Required	Not required
Channel availability	Good – widely installed power-line carrier or other binary channels	Expensive – data stream transmission via multiplexed or direct fiber, digital microwave	Good – widely installed power-line carrier or other binary channels
Handling of channel impairments	Digital processing improves performance	Varying, depends on design	Poor
Operating time	0.75 to 1 cycle SPC,0.5 to 0.75 cycle DPC	0.75 to 1.5 cycles for high fault current, slower for low current faults	1-1.5 cycles for tripping schemes, 1.5-2 cycles for blocking schemes
Complexity of application and settings	Relaying: simple; Communication: simple	Relaying: simple; Communication: relatively involved	Relaying: relatively involved to complex; Communication: simple
Sensitivity of application to power system topology and evolution	Low	Low	Higher – need coordination studies and setting changes.
Resistive fault coverage	Good; additional starting functions might be needed	Good with charging current compensation	Good with 67N or 67Q
Applications on long lines	Economical from the channel perspective; charging current compensation beneficial	Signal retransmittal is needed every »100km; charging current compensation beneficial	Economical from the channel prospective; charging current must be factored into the 67N/Q settings
Applications on short lines	Straightforward	Straightforward	Reach behavior of distance or overcurrent elements under varying system conditions requires study
Applications on tapped lines	Possible with distance supervision stopping short of LV transformer sides; may encounter channel problems: reflection losses and signal resonance	Possible with distance supervision stopping short of LV transformer sides	Possible with distance stopping short of LV transformer sides; 67N/Q cannot be used; may encounter channel problems: reflection losses and signal resonance
Measurement quantities	Current comparison only	Current comparison only	Current and voltage; susceptible to misoperation due to voltage loss or poor CVT transient response.
Applications on 3-terminal lines	Straightforward	Straightforward	Difficult coordination due to outfeed/infeed
Application on series-compensated lines	Straightforward; good performance	Straightforward; good performance	Involved engineering; varying performance
CT saturation	Naturally secure principle	Naturally secure principle	Subject to misoperation
Single-pole tripping	Easy engineering; good performance	Easy engineering; good performance	Involved engineering; varying performance
Ring-bus and breaker-and-a-half applications	Secure with the two breaker currents measured and processed individually, combined with two-breaker logic	Secure if restrained using individual breaker currents (as opposed to summed line current)	Subject to misoperation; requires special logic with poor CTs
Weak-infeed conditions	Good performance; may need explicit weak infeed logic	Naturally secure and dependable	Needs explicit weak infeed logic
Current reversal	Naturally secure	Naturally secure	Requires explicit logic

Table 1
Summary of Schemes

33RD Annual
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The Western Protective Relay Conference (WPRC) is an educational forum for the presentation and discussion of broad and detailed technical aspects of protective relaying and related subjects. Approximately 450 attend, mostly from the western United States.

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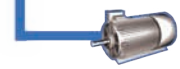

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Fundamentals of a Motor Thermal Model and its Applications in Motor Protection

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1. Abstract

This paper discusses the fundamentals of a motor thermal model and its mathematical interpretation and physics for the different stages of motor operation. (overload, locked rotor, too frequent or prolonged acceleration, duty cycling applications). It explains Thermal Model Time Constants and other technical parameters that cause the biasing of the thermal model algorithm. Other topics covered in this paper show that (a) detailed motor data sheet information, and (b) coordination between the protection engineer and the motor supplier, can lead to proper selection of motor thermal protection parameters. This paper presents a closer look at motor stall, acceleration and running thermal limit curves. It also explains the concept of thermal capacity and elaborates on how thermal capacity is evaluated in motor protection devices. The following points are also covered in this paper:

- Discusses some additional methods, such as voltage-dependant and slip-dependant motor overload curves, employed to evaluate thermal capacity in nonstandard motor applications,
- Presents the concept of matching thermal time constants for motor cyclic loads cases. In addition, the response of a thermal model algorithm in practical applications is demonstrated.
- Describes a real case example showing how to apply and fine-tune the thermal model in high-inertia load application.
- Explores in this context, some of the key topics that will ensure safe operation of the motor while promoting satisfactory motor design characteristics.

2. Introduction

Induction motors are the workhorses of any industrial plant. Typical motor applications include pumps, fans, compressors, mills, shredders, extruders, de-barkers, refiners, cranes, conveyors, chillers, crushers, and blowers. Statistics have shown that despite their reliability and simplicity of construction, annual motor failure rate is conservatively estimated at 3-5% per year, and in extreme cases, up to 12%, as in the Pulp and Paper industry. Downtime in a factory can be very expensive and, in some instances, may exceed the cost of motor replacement. Proper machine protection is required to minimize the motor failure rate, prevent damage to associated equipment and to ensure both personnel safety and production targets.

The document "Report of Large Motor Reliability Survey of Industrial and Commercial Installations", published by the IEEE Motor Reliability Working Group [3] contains the results of IEEE and EPRI surveys on motor reliability and major causes of motor failure. The summary of these results is shown in Table I.

In spite of different approaches and criteria (IEEE failure groups are formed according to "cause of failure" and EPRI according to "failed component") both studies indicate a very similar failure percentage associated with mechanical- and electrical-related machine problems.

Analyzing the data from this table we can conclude that many failures are directly or indirectly related to, or caused

IEEE Study		EPRI Study		Average
Failure Contributor	%	Failed Component	%	%
Persistent Overload	4.2%	Stator Ground Insulation	23.00	Electrical Related Failures
Normal Deterioration	26.40%	Turn Insulation	4.00	
		Bracing	3.00	
		Core	1.00	
		Cage	5.00	33%
Electrical Related Total	30.60%	Electrical Related Total	36.00%	
High Vibration	15.50%	Sleeve Bearings	16.00	Mechanical Related Failures
Poor Lubrication	15.20%	Antifriction Bearings	8.00	
		Trust Bearings	5.00	
		Rotar Shaft	2.00	
		Rotor Core	1.00	31%
Mechanical Related Total	30.70%	Mechanical Related Total	32.00%	
High Ambient Temp.	3	Bearing Seals	6.00	Environmental Maintenance & Other Reasons Related Failures
Abnormal Moisture	5.8	Oil Leakege	3.00	
Abnormal Voltage	1.5	Frame	1.00	
Abnormal Frequency	0.6	Wedges	1.00	
Abrasive Chemicals	4.2			
Poor Ventilation Cooling	3.9			
Other Reasons	19.7	Other Components	21.00	
Environmental Reasons & Other Reasons Total	38.70%	Maintenance Related & Other Parts Total	32.00%	35%

Table 1.
Summary of IEEE and EPRI Motor Reliability Surveys.

by, extensive heating of the different motor parts involved in machine operation. That is why we find accurate tracking of motor thermal status and adequate response of the motor control system to abnormal situations to be very important.

Modern trends in motor design and construction are moving in the direction of making motors more compact and efficient. The use of inorganic insulation materials such as fiberglass and silicon resins provides improved dielectric motor insulation properties compared to legacy materials such as cotton and varnish. But at the same time some new materials are more vulnerable to excessive heating. Another important consideration that should be consdered in tracking the thermal state of the motor, is heating overestimation, which can also cause undesirable motor stoppage and hence potentially costly interruption of processes. The statements above clearly explain the importance of an accurate thermal estimate of a motor in service.

Currently this task (precise motor thermal protection) is strongly supported by modern technology. The developed algorithms can be implemented in microprocessor devices, which are capable of providing a desirable level of accuracy and flexibility.

The thermal algorithm operates as per the following sequence:

- Real-time motor data is supplied to microprocessor device.
- This data is processed according to the firmware thermal algorithm program and compared with expected values, stored in memory.
- The protection device computes the analog value, which is compared with the programmed threshold.
- The protection device triggers the digital outputs if the compared analog value exceeds this threshold.

The ideal analog method for modeling the thermal image in the Motor Protection Device (MPD) would be to embed non-inertial temperature sensors into the stationary (stator) and rotating (rotor) parts of the motor structure. However, it is not feasible to install temperature sensors in the rotors for technical reasons, reliability and cost. An additional reason to reject such temperature sensors as the main basis for thermal protection, is the fact that the traditional Resistance Temperature Detector (RTD) has a relatively slow reaction time and can't respond adequately to the high speed of the heating process during motor acceleration.

Stator RTDs actually provide realistic results in monitoring the temperature under balanced motor conditions, but again they are not suitable for monitoring the fast thermal transients.

Alternatively, a main real-time input thermal model could use 3-phase motor current. The electrical energy applied to the motor is partially transformed into heat which is stored in the motor. Thus this heat is a function of current and time. This fact, plus some other factors and assumptions that will be covered further in this paper, are employed to develop and implement the current-based thermal model. 3-phase current values measured in real-time are also used in special algorithms applied to detect different stages of motor operation: stopped, start, run, overload.

In high-inertia load applications voltage monitoring can be used in the thermal model algorithm to dynamically match the thermal limit to different starting conditions. In some applications speed sensors are employed to detect slow rotor rotation or motor stall.

Another important part of thermal model implementation is "Expected values stored in MPD". This term implies that information is available from the motor designer and motor manufacturer, that is related to the thermal reserve, allowed performance and thermodynamics of the motor in question.

The motor is not a homogeneous body and even one component can be presented as a combination of nodes connected via thermal resistance to each other and external ambient conditions. For example, the stator has slot copper, end-head copper, teeth and a core. Each node is characterized by its own rate of temperature change. [6]

That is why in order to do the full analysis and detect a boundary for normal operation, motor designers always target the development of the most detailed model including electrical, mechanical, thermal, and chemical components. But once a motor is properly designed and constructed to its intended specifications, a less detailed model is adequate to provide thermal protection by evaluating thermal risk with reference to motor data sheets and thermal damage curves.

Common sense dictates reliance on a complete motor analyses to determine the correspondence of the MPD algorithm variables to the data typically available from the motor manufacturer. MPD also incorporates simplified algorithms modeling physical motor states and processes. This approach allows us to attain an adequate level of thermal protection in modern MPD, for any application, by handling the available motor information. In trying to keep the algorithm simple we face another challenge. It is rather difficult to relate the thermodynamic behavior of the motor under steady-state conditions, with the rapid stator and rotor heating that occurs during thermal motor transients such as acceleration, stall and cyclic load change. The algorithm must also account for heat transfer from the motor's winding to the housing and from the housing to the free (ambient) air. To resolve this issue the "time before trip" parameter was selected as the common criterion for thermal condition evaluation. Actually, for motor acceleration and stall conditions, the safe stall time specified by motor designers, is the only objective estimate of the maximum allowable motor temperature, because of the real difficulty of directly measuring the rotor temperature. [6]

Based on the discussion in this section of the paper, the main motor thermal algorithm requirements can be summarized as follows:

- **Accuracy.** A precise estimate of the thermal motor image. Consideration of different motor applications, such as variable frequency, voltage unbalance, long acceleration, cyclic loads. Reference to data specified by motor designers.
- **Simplicity.** The algorithm is easy to understand. A simple way to calculate the thermal estimate of the motor for the operational sequence in question.
- **Dependability.** The capability of monitoring the thermal

capacity at any moment of motor operation. The thermal estimate is maintained and responds adequately to MPD power failure events.

- **Compliance to industry standards.** The algorithm must meet the requirements, and should follow the recommendations listed in, IEEE Guide for AC Motor Protection (Std C37.96-2000) [9] and IEEE Guide For the Presentation of Thermal Limit Curves for Squirrel Cage Induction Machines (Std 620-1996) [10].
- **Easy Setup.** The parameters required to set up the thermal model are obtained from the standard set of motor data readily available from motor manufacturers.
- **Reliability.** The model is supported by alternative motor temperature evaluation methods, based on RTD's monitoring. This backup method is extremely useful in cases where the thermal process significantly deviates from what was expected because of abnormal ambient temperatures or motor cooling impairment.
- **Flexibility.** The possibility of apply the model even in very unusual cases.

In addition to the accurate thermal model the state of the art Motor Protection Device should be equipped with the enhancements and additional functionality listed below.

- RTD Inputs for absolute temperature monitoring, alarming and tripping of the motor at high temperatures.
- Temperature-based stator thermal estimate, capable to correct main thermal model in the abnormal operational conditions
- A temperature-based stator thermal estimate, capable of correcting the main thermal model under abnormal operating conditions
- Wide selection of thermal overload curves; standard for typical applications, user defined for unusual applications and voltage dependant for special applications, featured long starts of high inertia loads.
- A Motor Start Lockout feature inhibiting the start of the machine in the case of non-availability of sufficient thermal reserve to complete the acceleration. The lockout time is calculated based on the available thermal capacity, the maximum learned value of Thermal Capacity Used (TCU) during one of the last 5 successful starts and the rate of temperature change for the motor at standstill.
- A wide selection of thermal overload curves; standard for typical applications, user-defined for unusual applications and voltage-dependant for special applications, featuring long starts of high inertia loads.
- Thermal model biasing in response to the current unbalance that causes an extensive heating effect.
- The option to select separate cooling constants for the motor in the stopped and running states.
- A current unbalance element capable of issuing a warning about a potentially dangerous level of unbalance and of tripping the motor off line on single–phasing.
- A Start Supervision Element preventing an excessive number of motor starting sequences.
- A mechanical Jam Detector.
- An acceleration limit timer.
- Phase Short Circuit and Ground Fault Protection Functions.
- Voltage and Frequency elements ensuring motor operation within specified limits. Phase Reversal Detection.
- Power Elements to monitor and respond to abnormal motor loading conditions.
- MPD failure detection.
- Communication capability to host computers to allow easy integration into existing DCS and SCADA systems.
- Cost justifiable.
- Can be adapted (retrofitted) to multi-vendor MCC's and motor starters.
- Industrially hardened by means of a conforming coating, to work in mill environment.
- Highly accurate predictions of mechanical and insulation failure, as well as the broken rotor bar condition, without removing the motor from service and without the need for resident experts.
- The capability of reading/capturing motor currents and voltages during electrical system faults.
- The capability of recording and storing in the device's nonvolatile memory, time-stamped events related to abnormal motor situations.

Additional protection functions can be provided using expensive equipment such as vibration sensors and/or instruments to display the current spectrum of the motor, to predict incipient failures. These are not covered in this document.

3. Thermal Protection Theory

There are two main types of thermal risks for an overheated motor: stator insulation may degrade and/or rotor conductors may decrease their capability to resist bending (deformation) forces or even melt. Deterioration of stator insulation presents the chemical process that is governed by an Arrhenius equation [6[, [7]. NEMA Motor Insulation Class defines the maximum allowable temperature rise above the

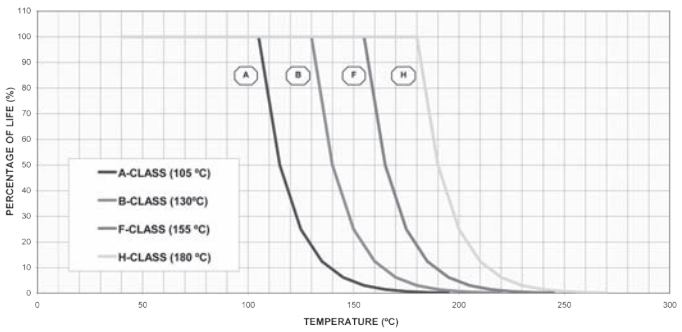

Fig 1.
Aging Factor of Motor Insulation.

ambient or thermal limit, if temperature exceeds this limit it doesn't cause immediate insulation failure but decreases the insulation's expected lifetime. A fairly accurate approximation of Arrhenius equation states that an operating temperature increase of 10°C in excess of the thermal limit cuts the life of stator insulation by half. The percent of life vs temperature characteristics for different classes of insulation are shown at Figure 1.

The thermal risk for a squirrel cage rotor is that the rotor conductors may deform or melt. Since there is no insulation, the rotor conductors can be operated at a much higher temperature than the stator conductors. It is difficult and impractical to provide a numerical temperature value defining the rotor thermal limit. Motor designers address the maximum allowable rotor temperature under stall, acceleration or any other fast transient conditions by stating the stall time thermal limits for a hot or cold motor. These values must correspond to the system voltage level during the stall event. For the majority of applications, the safe stall time defines the rotor thermal limit, but in some special cases motor capability during stall and acceleration is dictated by the stator thermal limit. A rule of thumb to define a stator-limited motor says: "When the voltage rating of the motor is equal to or greater than 10 times the horsepower rating, the motor is stator limited." For example: 500 HP, 6900 V. [8]

Steady-state operations such as running overloads are usually not an issue for the rotor. Under running conditions the stator is subject to extensive heating. Thus a stator overload protection element ensures an overall sufficient level of thermal protection for a rotor rotating at near synchronous speed.

The steady state and transient thermal behavior of the stator and rotor conductors of a motor depends on the details of the motor thermal circuit. The motor designer typically uses a rather detailed thermal circuit, including separate representations of stator iron, rotor iron, stator conductors, rotor conductors, internal air, external air, motor shell and end shields. Details of the thermal circuit depend on the ventilation construction of the motor, including "drip proof", "totally enclosed fan cooled", and "totally enclosed non-ventilated". For example, heat storage in each circuit element as well as convective or conductive heat transfer between various pairs of circuit elements is included in the model. A typical motor thermal circuit used by a motor designer may have on the order of 20 nodes and 20 branches, resulting in a dynamic response characterized by several time constants.

Motor designers are typically interested in a few standard thermal scenarios including steady state loading, cold, hot and successive starting. The designer checks the computed steady-state temperature of the stator winding to make sure it is within the capability of the selected insulation system, designers also define the time limits to withstand overloads. It is also very important to determine running and stopped motor cooling rates especially for "totally enclosed non-ventilated" motor designs and in some applications with intermittent use ratings. The motor designer is also interested in allowable cold and hot stalled times. Stalled thermal calculations are usually performed assuming adiabatic conditions. The designer often concedes the fact that the peak temperature of the stator winding may temporarily exceed the steady state capability of the insulation system, taking into account the expected application of the motor and how many times it is expected to be stalled cold or hot in a lifetime, in making a design compromise. After a design is complete, a summary of the thermal model becomes available. Basic information includes the steady state thermal rating of the motor, hot and cold stall times, and the cooling time constants of the motor. For medium and large motor designs complete thermal damage curves of allowable time versus current are provided as a standard.

Once the motor has been designed, and the basic operational parameters have been established for steady state load and cold and hot stall times, the responsibility shifts to thermal protection for the motor. For majority of service conditions the operating profile of the motor matches the assumptions made by the motor designer, so that the main job of thermal protection is to stay out of the way and let the motor run. However, if motor is abused by mechanical breakage or human error then protection steps in to assure there is no risk of thermal damage.

The question is, what model should be used to protect the motor when it is running? What is a reasonable compromise between accuracy and complexity? What physics should be included? What should be used as an estimate of operation limit?

As we mentioned before the ideal method would be to have the direct accurate temperature measurement and use aging factor to estimate the consumed motor thermal capacity. But temperature sensors (RTD) have a delayed response to thermal transients such as stall and acceleration and can't serve as a basic criterion for a thermal model.

How detailed should the model be?

We should certainly provide a model with enough flexibility to protect motors that have a dynamic thermal response represented by several time-constants. A single time-constant is not always adequate [6]. Physics shows that there are at least 4 distinct thermal time-constants: 2 for the stator conductors, and 2 for the rotor conductors. For example, when heat is generated in the stator conductors, the first effect is to raise the temperature of the conductors. The stator winding in the stator slots are surrounded by a steel magnetic core. Therefore, as the windings get hot, heat begins to flow from the windings into the steel core. The combination of the thermal capacity of the winding and the thermal conductivity/impedance between the winding and the steel core establishes a short time-constant. Heat that continues to flow from the winding into the surrounding core is stored in the core, causing its temperature to rise, but more gradually than the initial rate of rise of the windings, because of the greater thermal capacity of the core. Eventually, the temperature of the core (and the motor frame, etc.) also rises, causing heat transfer by convection to the surrounding air. The combination of the thermal capacity of the core and the frame and the thermal impedance between them and the cooling air establishes a time-constant that is much

longer than that of the winding-core interaction.

So, the next question is, what is the best way to go beyond a single time-constant model?

The most reasonable way to model the thermal state of the motor is to measure motor current and to correlate it in real time to motor thermal damage curves. The manufacturer's thermal damage curves represent the results of simulations of a complete motor model, including a multi-node thermal model. The curves capture the multi-time-constant parameters and thermal damage times for running, stall and sometimes acceleration conditions of the motor. Typical curves are shown at Figure 3. Any point on the motor thermal damage curve represents a thermal time limit at a specific level of current, or in other words: "The thermal limit defines how long a motor can withstand the corresponding level of stator current without exceeding the thermal boundary specified by the motor manufacturer." Details of the thermal model implementation, based on overload curves are given in the next section.

In this section we answer two important theoretical questions concerning a thermal model based on motor thermal damage curves (overload curves):

1. What is the relationship between standard overload curves and a single time-constant thermal model?

2. Does an overload curve based thermal model behave correctly when it is used in applications in which the load is not constant?

We turn to mathematical analyses of the physics to answer theses two questions, starting with an analysis of a single time-constant model. The thermodynamic behavior of homogeneous body at rest (motor) heated by electrical current can be described by a single time-constant thermal equation:

$$C \cdot \frac{dT'(t)}{dt} = I'^2(t) \cdot R - H \cdot T'(t)$$
$$T'(t) = \text{motor temperature rise above ambient} \quad (1)$$
$$I'(t) = \text{motor current}$$
$$C = \text{specific heat capacity of the motor}$$
$$H = \text{running heat dissipation factor}$$
$$R = \text{electrical resistance}$$

It is convenient to rewrite equation (1) in terms of per unit temperature rise and per unit current:

$$T(t) = T'(t)/T_{\max} = \text{per unit temperature rise}$$
$$I(t) = I'(t)/I_{rated} = \text{per unit current} \quad (2)$$
$$I_{rated} = \text{rated current}$$
$$T_{\max} = \text{motor temperature at thermal limit trip condition}$$

In that case, equation (1) can be rewritten as:

$$\tau \cdot \frac{dT(t)}{dt} = I^2(t) \cdot \frac{I_{rated}^2 \cdot R}{H \cdot T_{\max}} - T(t) \quad (3)$$
$$\tau = \frac{C}{H}$$

The maximum temperature is related to the rated current such that $\frac{I_{rated}^2 \cdot R}{H \cdot T_{\max}} = 1$. In that case, equation (3) can be rewritten as:

$$\tau \cdot \frac{dT(t)}{dt} = I^2(t) - T(t) \quad (4)$$

Equation (4) can be used to analyze the thermal response of a single time-constant model to a steady overload. It can be shown that the solution of equation (4) for a steady overload, starting from a cold initial condition, is given by:

$$T(t) = I^2 \cdot \left(1 - e^{-t/\tau}\right)$$
$$I = \text{per unit motor current (a constant)} \quad (5)$$
$$T(t) = \text{per unit motor temperature rise}$$

Equation (5) can be solved for the amount of time needed for the temperature rise to reach the thermal limit of the motor, i.e. T(t)=1:

$$t_{\max}(I) = \tau \cdot \ln\left(\frac{I^2}{I^2 - 1}\right)$$
$$t_{\max}(I) = \text{time estimated by a simple thermal model for the motor temperature to reach thermal limit} \quad (6)$$

To develop a comparison between a single time constant thermal model and overload curves, we now turn our attention to standard overload curves, which are given by:

$$t_{\max}(I) = \frac{87.4 \cdot CM}{I^2 - 1} \quad (7)$$
$$t_{\max}(I) = \text{trip time, seconds}$$
$$CM = \text{curve multiplier}$$

To compare standard overload curves with the behavior of a single time constant model, it is useful to start by recognizing that the numerator of the right hand side of equation (7) corresponds to a time constant:

$$t_{\max}(I) = \frac{\tau_{CM}}{I^2 - 1} \quad (8)$$
$$\tau_{CM} = 87.4 \cdot CM$$

Equation (6) and equation (8) are plotted in Figure 2. In order to make the curves align for large values of current, it is necessary to satisfy the following constraint:

$$\tau = \frac{C}{H} = \tau_{CM} = 87.4 \cdot CM \quad (9)$$

In other words, in order for an overload curve to match a single time-constant thermal model during a simple step overload, the

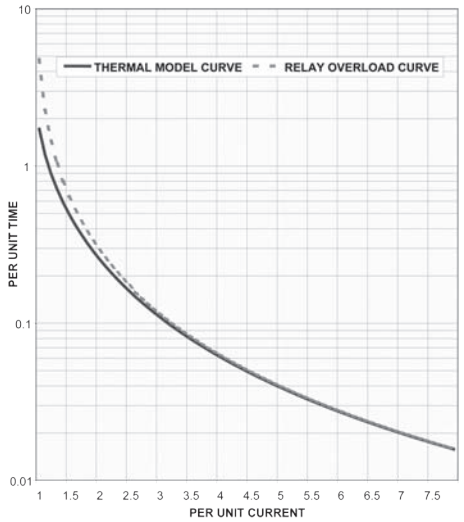

Fig 2.
Single Constant Thermal Model vs Relay Overload Curve Comparison

time-constant implied by the curve multiplier of the overload curve must be set equal to the time-constant of the single time-constant model. In Figure 2, the ratio of the time divided by the time-constant is plotted against per unit current. It can be seen that although equation (6) is not exactly the same as equation (8), the approximation is very close, particularly for large values of current. For lower values of current, the standard overload curves are a better approximation to typical motor overload curves than a single time-constant model. That is because there are at least two time-constants in the thermal response of a motor. Over short time intervals, the thermal response of a motor is dominated by heat transfer from the stator and rotor conductors to iron. Over longer time intervals, the thermal response is dominated by heat transfer from the iron to cooling air. A single time-constant model cannot be accurate over the full range of operation and tends to overprotect a motor when it is operated near its rated load. A standard overload curve provides protection that is a closer match to a motor's thermal limit. The close proximity of the two curves for large values of current is not a coincidence because both models are equivalent to an adiabatic model for large values of current. This can be shown mathematically by finding the asymptotic behavior of the two curves. First, equation (8) is given approximately by:

$$t_{\max}(I) = \frac{\tau_{CM}}{I^2 - 1}$$
$$t_{\max}(I) \approx \frac{\tau_{CM}}{I^2} \qquad I^2 >> 1 \tag{10}$$

A similar approximation can be shown to hold for equation (6) by rewriting and taking a Taylor's expansion in terms of the reciprocal of the square of the current. First, we rewrite to explicitly show the dependence on the reciprocal of the square of the per unit current:

$$t_{\max}(I) = \tau \cdot \ln\left(\frac{I^2}{I^2 - 1}\right)$$
$$t_{\max}(I) = \tau \cdot \ln\left(\frac{1}{1 - 1/I^2}\right) = -\tau \cdot \ln\left(1 - 1/I^2\right) \tag{11}$$
$$t_{\max}(I) = -\tau \cdot \ln(1 - x)$$
$$x = 1/I^2$$

We then take the first two terms in a Taylor's expansion of $\ln(1-x)$ with respect to x around the point $x = 0$:

$$\ln(1-x) \approx \ln(1) - x \approx -x \qquad x << 1$$
$$\therefore t_{\max}(I) \approx \frac{\tau}{I^2} \qquad I^2 >> 1 \tag{12}$$

Equation (8) describes how long it will take a standard overload curve to reach thermal limit for a constant overload. We now turn our attention to how a standard overload curve behaves during cycling loads. We start with the differential equation that is used to implement standard overload curves:

$$\frac{dT(t)}{dt} = \frac{I^2(t) - 1}{\tau_{CM}} \tag{13}$$

To gain insights into what the response is to a cycling load, we will consider a simple cycling load in which the current alternates between no load and an overload value:

$$I_{low} = 0 \approx \text{current during the low cycle}$$
$$I_{high} = \text{current during the high cycle}$$
$$t_{low} = \text{time interval for the low cycle} \tag{14}$$
$$t_{high} = \text{time interval for the high cycle}$$

Motor heating is proportional to the square of the current, so the effective current for heating over the cycle is:

$$H_{effective} = I_{effective}{}^2 = \frac{t_{high} \cdot I_{high}{}^2 + t_{low} \cdot I_{low}{}^2}{t_{low} + t_{high}} \tag{15}$$
$$I_{effective} = \text{effective value of the load current}$$
$$H_{effective} = \text{effective heating value of the load}$$

Equation (15) can also be expressed in terms of a duty cycle ratio:

$$H_{effective} = D \cdot I_{high}{}^2 + (1 - D) \cdot I_{low}{}^2$$
$$D = \text{duty cycle ratio} = \frac{t_{high}}{t_{low} + t_{high}} \tag{16}$$

If the current and heating are expressed in per unit and the low cycle current is approximately equal to zero, the steady state boundary condition for tripping the motor becomes:

$$1 = D \cdot I_{high}{}^2 \tag{17}$$

Equation (17) defines the appropriate response to a duty cycle. It can be shown that a single time-constant model provides approximately this response. The next question is what is the response of a standard overload curve to a duty cycle? Analysis of a standard curve under load cycling conditions will show that the response is correct, and will reveal how to properly set an overload curve model to match the behavior specified by equation (17). We must consider values of current below pickup, during which our motor thermal model is defined by the following differential equation:

$$\frac{dT(t)}{dt} = \frac{1}{\tau_{cool}} \cdot \left(I \cdot \left(1 - \frac{hot}{cold} \right) - T(t) \right) \quad (18)$$

τ_{cool} = cooling time constant

hot = hot stall time

$cold$ = cold stall time

The factor $\left(1 - \frac{hot}{cold}\right)$ is included to match the hot and cold stall times specified by the motor manufacturer. By including the factor in the cooling computation, the hot overload curve is effectively shifted down by the correct amount relative to the cold overload curve to account for the difference in "time to trip" of hot and cold motor conditions.

For the load cycle under consideration, the current during the unloaded part of the cycle is approximately equal to zero, so the differential equation given by (18) reduces to:

$$\frac{dT(t)}{dt} = -\frac{T(t)}{\tau_{cool}} \quad (19)$$

Taken together, equations (19) and (13) describe the behavior of our model during the assumed load cycle. The approximate temperature rise during the overload portion of the load cycle estimated by the overload curve is computed by multiplying equation (13) by the overload time:

$$\Delta T_{high} \approx \frac{1}{\tau_{CM}} \cdot \left(I_{high}^2 - 1 \right) \cdot t_{high} \quad (20)$$

The approximate temperature drop estimated by the cooling model during the unloaded portion of the duty cycle is computed by multiplying equation (19) by the appropriate time, with per unit temperature equal to 1, because that is what it will be approximately equal to during a limit cycle that approaches tripping:

$$\Delta T_{low} \approx -\frac{1}{\tau_{cool}} \cdot t_{low} \quad (21)$$

The overload detection boundary is determined by setting the net temperature change equal to zero. This implies that the total of the right hand sides of equations (20) and (21) taken together is equal to zero:

$$\Delta T_{high} + \Delta T_{low} = \frac{1}{\tau_{CM}} \cdot \left(I_{high}^2 - 1 \right) \cdot t_{high} - \frac{1}{\tau_{cool}} \cdot t_{low} = 0 \quad (22)$$

Equation (22) can be rearranged to show that standard overload curves respond correctly to cycling loads. Equation (22) also reveals how to properly select parameters for a load cycling applications:

$$1 = \frac{\tau_{cool}}{\tau_{CM}} \cdot D \cdot I_{high}^2 \quad (23)$$

Equation (23) expresses the actual overload detection boundary of an overload curve model in terms of its settings, the duty cycle, and the amount of overload. Except for the factor of $\frac{\tau_{cool}}{\tau_{CM}}$, equation (23) is exactly the same as the ideal overload detection boundary, specified by equation (17). Equation (23) and equation (17) will be identical, provided that $\frac{\tau_{cool}}{\tau_{CM}}$ is set equal to one resulting in the following consistency constraint:

$$\tau_{cool}(\min) = \frac{87.4 \cdot CM}{60} \quad (24)$$

Equation (24) represents a consistency constraint relating the cooling time-constant and the curve multiplier of a standard overload curve. Figure 9 shows what can happen if it is not satisfied. There are three cases shown for a cycling load with an approximate per unit heating value of one. In the first case, the cooling time-constant is set too long resulting in over-protection and early motor tripping. In the second case, the cooling time-constant is set according to equation (24) to match the implied time-constant of the curve multiplier, and the protection is correct. In the third case, the cooling time-constant is set too short, resulting in under-protection and possible motor overheating.

4. Thermal Model Algorithm

The thermal model algorithm was developed in order to create the thermal image of the motor and closely track the thermal conditions for all states of motor operation. The following states of motor operation are recognized:

- **Motor Stopped:** Current is below zero level threshold and motor switching device indicates the open status.
- **Motor Starting:** State is declared when previous state was "Stopped" and current greater than 2% of the motor full load amps has been detected. The motor current must increase to the level of overload pickup (service factor times full load amps) within 1 second otherwise motor will transfer into the next state: "Running"
- **Motor Running:** State is declared when previous state was "Starting" and motor current drops below overload pickup level.
- **Motor Overloaded:** State is declared when previous state was "Running" and motor current raises above the overload pickup level.

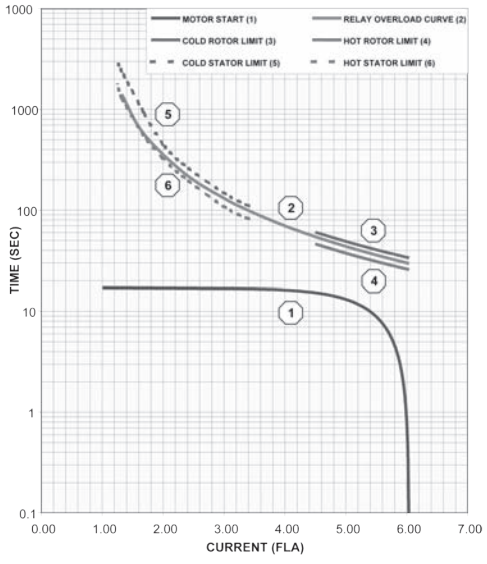

Fig 3.
Motor Thermal Limit Curves

Thermal Capacity Used (TCU) evaluates the thermal condition of the motor. TCU is expressed as percentage of the thermal limit used during motor operation. Per IEEE Std 620-1996 (10) the motor thermal limit is presented in the form of a time-current curve for 3 possible motor overload conditions: locked rotor, acceleration and running overload. Every point on this curve represents the maximum allowable save time at a stator current above normal load.

TCU is incrementally updated every 100 milliseconds and the integrated value of TCU is stored in the thermal memory register of MPD according to the following equation.

$$TCU_{@T} = TCU_{@T-1} + \frac{TIME\ INTERVAL}{TIME-TO-TRIP} \times 100\% \qquad (25)$$

The following example can be a good illustration of TCU accumulation during the cold motor start; initial TCU is equal to 0%. Motor starting pattern (1) and relay overload curve (2) are shown at Figure 3.

For simplicity assume that the time interval for TCU update is 1 second. Every point of motor current on this plot corresponds to the number of seconds that motor can withstand before tripping on overload. The numerical values showing the progress of TCU accumulation during 17 seconds of motor acceleration are presented in table 2. We can observe that by the end of a successful starting the thermal memory of the motor protection device (MPD) accumulates 46.7% of TCU.

ACCEL. TIME (SEC)	ACCEL. CURRENT	TIME-TO-TRIP	TCU@T-1	TCU@T
0	6.04	29.6	-	0
1	5.99	30.1	0.0	0% + (1sec/29.6sec) x 100% = **3.4%**
2	5.94	30.6	3.4	3.4% + (1sec/30.1sec) x 100% = **6.7%**
3	5.89	31.1	6.7	6.7% + (1sec/30.6sec) x 100% = **10.0%**
4	5.84	31.7	10.0	10.0% + (1sec/31.1sec) x 100% = **13.2%**
5	5.78	32.4	13.2	13.2% + (1sec/31.7sec) x 100% = **16.3%**
6	5.71	33.1	16.3	16.3% + (1sec/32.4sec) x 100% = **19.4%**
7	5.65	34.0	19.4	19.4% + (1sec/33.1sec) x 100% = **22.4%**
8	5.57	34.9	22.4	22.4% + (1sec/34.0sec) x 100% = **25.4%**
9	5.49	36.0	25.4	25.4% + (1sec/34.9sec) x 100% = **28.3%**
10	5.40	37.3	28.3	28.3% + (1sec/36.0sec) x 100% = **31.0%**
11	5.29	38.8	31.0	31.0% + (1sec/37.3sec) x 100% = **33.7%**
12	5.17	40.7	33.7	33.7% + (1sec/38.8sec) x 100% = **36.3%**
13	5.03	43.2	36.3	36.3% + (1sec/40.7sec) x 100% = **38.8%**
14	4.85	46.6	38.8	38.8% + (1sec/43.2sec) x 100% = **41.1%**
15	4.60	52.1	41.1	41.1% + (1sec/46.6sec) x 100% = **43.2%**
16	4.18	63.6	43.2	43.2% + (1sec/52.1sec) x 100% = **45.1%**
17	1.03	17221.7	45.1	45.1% + (1sec/63.6sec) x 100% = **46.7%**

Table 2.
Thermal Capacity Used (TCU) calculation.

Typically the motor manufacturer provides locked rotor thermal limit curves or locked rotor safe stall time values for 2 motor conditions: cold motor (motor @ ambient temperature) and hot motor (motor @ ambient + rated rise temperature). In order to distinguish between the 2 aforementioned motor conditions the additional motor parameter, Hot/Cold Stall Time Ratio (HCR) is included in MPD algorithm.

These parameters define the proportional increase of TCU of the motor running fully loaded at a settled temperature compared to the motor resting at ambient temperature. For example let us assume that according to the motor data sheets the Cold Safe Stall Time is 10 seconds and the Hot Safe Stall Time is 8 seconds. Thus HCR is 8 sec / 10 sec = 0.8 and the level of stabilized TCU featuring the hot motor is equal to 20%, or in other words the allowed motor thermal withstand time at overload conditions will effectively decrease by 20%. If the motor load is lower then 100% the TCU level corresponding to the hot motor condition is proportionally lower: 75% load – 15% TCU, 50% load – 10% TCU and so on.

The unbalanced stator phase current will cause additional rotor heating due to the developed negative sequence current and flux rotating in the opposite direction to rotor rotation with approximately double the power system frequency. The skin effect in the rotor bars at this frequency will cause a substantial increase in rotor resistance and hence increased heating, which is not accounted for by the regular thermal model. In order to account for this additional heating factor the **Equivalent Current** concept is introduced. The idea is that the current input into the thermal model is biased to reflect the additional heating caused by the negative sequence component of the load current.

$$I_{EQ} = \sqrt{I_M^2 \times (1 + K \times (I_2/I_1)^2)} \qquad (26)$$

where:

I_{EQ} - equivalent motor heating current

I_M - real motor current

I_1 - positive sequence component of real motor current

I_2 - negative sequence component of real motor current

K - unbalance bias factor

The Unbalance Bias K factor reflects the degree of extra heating caused by the negative sequence component of the load current and can be defined as the ratio of Positive Sequence Rotor Resistance to Negative Sequence Rotor Resistance. It is practical and quite accurate to use the estimate method to define the K factor. Equations for typical and conservative estimates are presented below.

$$K = 175/I_{LRC}^2 \quad (typical)$$
$$K = 230/I_{LRC}^2 \quad (conservative) \qquad (27)$$

where I_{LRC} is the motor locked rotor current.

Of cause, in order to provide a complete thermal model of the motor in service, the cooling process must be taken into account. Cooling is characterized by Cooling Time-constants. These constants define the rate of cooling under stopped and running operating conditions.

When the motor is running at rated load, TCU accumulated during the motor start will decay exponentially and will stabilize at the level of TCU matching hot motor thermal conditions. If the motor load is lower, then obviously the thermal balance point is proportionally reduced.

The stopped motor will also be subjected to the exponential decay of TCU stored in MPD thermal memory during motor operation. Natural cooling of the rotating motor or forced cooling by means of the special fans installed on the machine shaft cause a much higher cooling rate of the running machine compared to the motor at standstill, typically the ratio is 2:1.

Thus 2 separate Cooling Time-Constants are used in the Thermal Model Algorithm. The equations to calculate TCU decay of the cooling motor are as follows:

$$TCU_{START} - TCU_{END}) \times e^{-t/\tau} + TCU_{END} \quad (28)$$

Where:

$TCU_{START}(\%)$	is the initial value of TC accumulated by the moment the cooling starts;
$t(\min)$	is duration of cooling;
$\tau(\min)$	is the Cooling Time Constant;
$TCU_{END}(\%)$	is the steady state level of TC

The steady state thermal condition for the motor at stand still is the ambient temperature, which is corresponding to

$$TCU_{END}(\%) = 0. \quad (29)$$

The steady state thermal condition for the running motor is calculated as:

$$TCU_{END} = \frac{I_{eq}}{SF \times FLA} \times (1 - HCR) \times 100\% \quad (30)$$

Where:

I_{eq}	is the value of the equivalent heating current accumulated by the moment cooling;
SF	is the service factor of the motor;
FLA	is the motor full load current (per unit);
HCR	is the hot to cold safe stall time ratio

In some unforeseen situations, when the motor cooling is blocked or ambient temperature deviates significantly from the industry standard value (40ºC), it becomes difficult to accurately replicate the motor's thermal condition based solely on the measured current. That is why it is practical to apply an independent algorithm, calculating TCU by means of stator RTDs (resistance temperature detectors) and correcting the thermal model upwards if needed.

The RTD-TCU Curve is constructed based on the 3 key points. See Figure 4 for details.

1. RTD bias minimum

Set to 40°C or another value of ambient temperature, if the appropriate RTD is available. TCU is equal to 0%.

2. RTD bias mid point

The mid-point temperature is set according to the motor's hot running temperature and is calculated as follows:

Rated Temperature Rise + Ambient Temperature

For example: The temperature rise for NEMA Class B motors with 1.15 Service Factor, is 90ºC. Thus the temperature value for this point is 130ºC. The TCU quantity for this point is the value of a steady-state running condition @ rated motor load, and can be found as:

$$TCU_{CENTER} = (1 - HCR) \times 100\% \quad (31)$$

3. RTD bias maximum

This point is set to the temperature rise equal to the motor insulation thermal limit.

Typically for NEMA B class motors insulation class is F with temperature rise above ambient of 115ºC. The TCU at maximum temperature point is equal to 100%.

Rate of change of TCU between the adjacent points is approximated as linear.

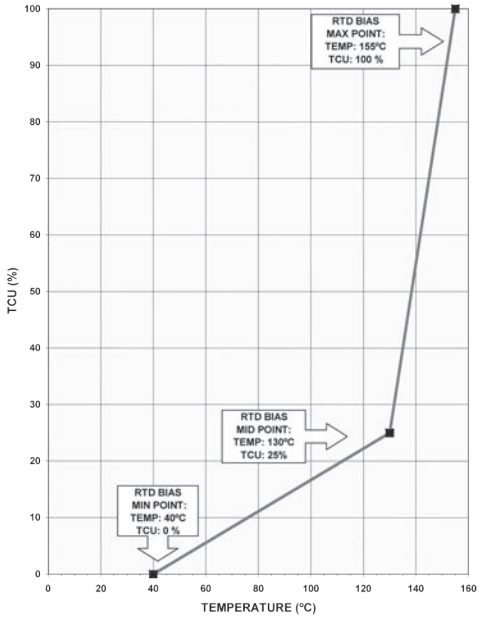

Fig 4.
RTD Bias of Thermal Model

5. Thermal Model Behavior at Different Operational Conditions

In order to illustrate how TCU varies during motor operation let us review the following motor data and operational sequences.

Let us assume that the following motor information is available to us.

- Motor thermal limit curves are as presented at Figure 3.
- Motor Cold and Hot Locked Rotor Times at 100% of the system voltage are 34 and 26 seconds respectively. At 80% of the system voltage Cold and Hot Locked Rotor Times are 50 and 38 seconds respectively.
- Motor Acceleration at 100% of the system voltage is 17 seconds. Maximum locked rotor current is 6 times that of full-load amperes (FLA). The MPD overload curve that we employ as a limit to calculate TCU, is shown in Figure 3. Please note that the location of this curve is between the hot and cold thermal limit curves supplied by the motor manufacturer. The time-current relation in this curve is per following equation:

$$T_{totrip}(\text{sec}) = \frac{87.4 \times 12}{I_{EQ}^2 - 1} \quad (32)$$

- The Running and Stopped Motor Cooling Constants are respectively 20 and 40 minutes. Motor Service Factor = 1.15.
- Current Unbalance Factor: 6

Sequence 1: Combined operation (Figure 5)

State A. Initially the motor is at ambient temperature. TCU = 0%. The motor is ready to start.

Section AB. The motor is successfully started at 100% voltage. Acceleration time = 17.1 seconds, TCU accumulated during start is 46.7% (details are in Table 2)

Section BC. The motor runs for 45 minutes at a steady load of 80% with 10% current unbalance. TCU by the end of the period, exponentially decays to level of 19.5 %. TCU is calculated per equation 25.

Section CD. The Motor runs at 125% balanced overload for 15 minutes. TCU increments to the level of 67.7%.

Section DE. The Motor runs at 125% overload with 10% current unbalance until the thermal capacity reaches 100% and the relay trips the motor offline in 8.5 minutes. It is not well illustrated on the graph, but the addition of current unbalance at the running overload state decreases the trip time by 1.5 minutes or 15% (the calculated balanced overload trip time for the section DE is 10 minutes).

Section EF. The motor is at standstill and cools down to ambient temperature for 150 minutes. TCU decays to approximately 0 level. The rate of cooling is 2 times slower than of the running motor.

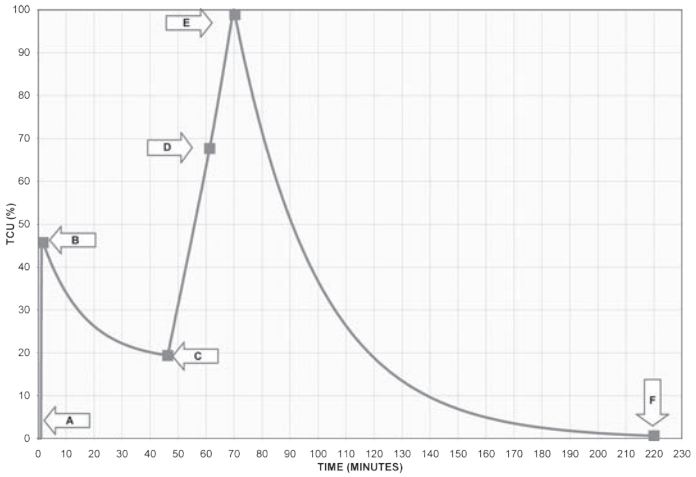

Fig 5.
Thermal capacity used during motor operation.

Sequence 2: Motor stall

The motor can be seriously damaged if a rotor stall occurs during the start attempt. Stall can occur due to a mechanical breakage or a human mistake. The stalled motor draws current equal to locked rotor amps. Locked rotor time (LRT) values provided by the motor manufacturer specify the thermal limit for the motor at ambient and rated conditions. Typically LRT is specified for the motor starts performed at 80% and 100% of the system voltages.

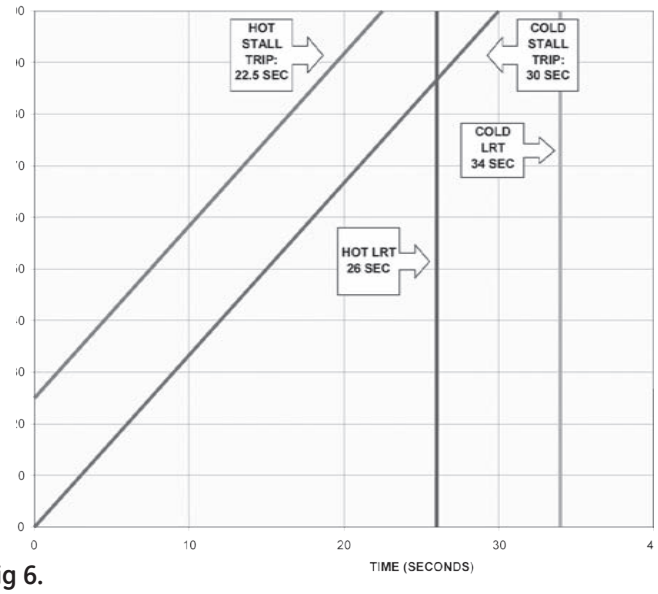

Fig 6.
Stall Trip. 100% Voltage

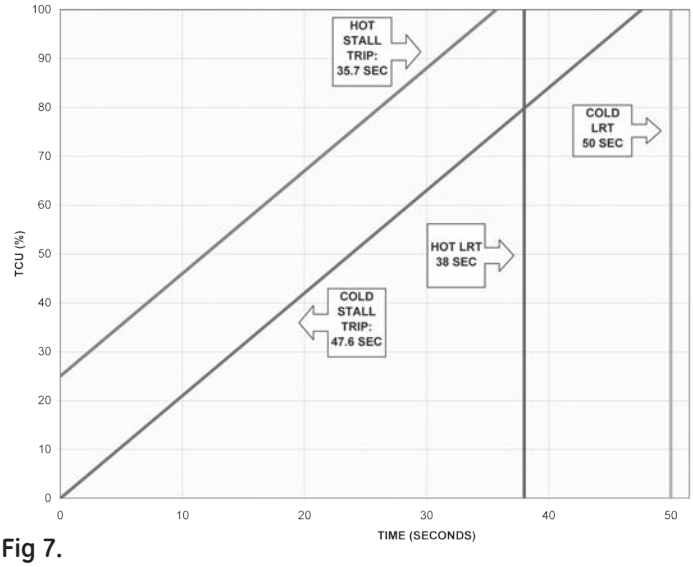

Fig 7.
Stall Trip. 80% Voltage

Figures 6 and 7 demonstrate how the thermal model provides an adequate protection where the motor is taken offline before the thermal limit is reached. This situation has been evaluated for hot and cold motor conditions at both 100% and 80% of the system voltages applied to the motor.

Sequence 3: Running overload

Three different scenarios are considered:

- The motor is overloaded immediately after a cold start.
- An overload is applied to the motor that was started, and, prior to overload, run unloaded for 2 hours.
- An overload is applied to the motor that was started and, prior to overload, run at full load for 2 hours.

The overload that was applied in all three cases was 125% of motor full-load amps.The motor thermal limit time values allow for applying a 125% overload to the cold and hot motor for 50 and 29 minutes respectively (data can be found in

Figure 3). The first case is characterized by severe heat generation in the rotor bars during the startup. Immediately following, the motor startup, the overload heats up the stator windings preventing heat transfer to the environment. This situation presents a serious thermal impact and the motor is taken offline faster in comparison to the other two cases. Trip time in this case is 16.3 minutes.

The second scenario presents an overload of the motor at ambient temperature. Initial TCU is 0%. According to the thermal model algorithm computations, the trip will be implemented 31 minutes after the overload is applied; which is lower than the cold motor limit (50 min). In a real application, the temperature of the unloaded running motor is typically higher than the ambient temperature, because of the associated motor losses. This fact explains why the significant margin between the cold overload trip time (31 min) and the cold thermal limit (50 min) is required.

The third scenario shows the hot overload (i.e. the motor is assumed to be at the rated temperature). The initial TCU in this case, the moment before the overload is applied, is 25%, so the tripping time is proportionally lower, compared to the cold overload. Tripping time in this case is 23 minutes, which is lower than the hot thermal limit (29 minutes).

Sequence 4: Consecutive starting

Per NEMA MG1 standard (11) medium and large induction motors are required to withstand thermally:

- 2 consecutive starts, coasting to rest between starts, with the motor initially at ambient temperature (cold starts)
- One start with the motor initially at rated load operating temperature (hot start)

An illustration of the thermal model response to consecutive starting is shown on Figure 8.

As you can see, the thermal model provides the start sequence required by NEMA.

An important enhancement to the thermal algorithm is the Start Inhibit function, which is employed to prevent excessive motor starting in cases where there is not enough thermal capacity available to perform a successful start. Modern intelligent protection devices are capable to learn and store, in the non-volatile memory, TC value utilized by motor during successful start and use this value in the start inhibit algorithm.

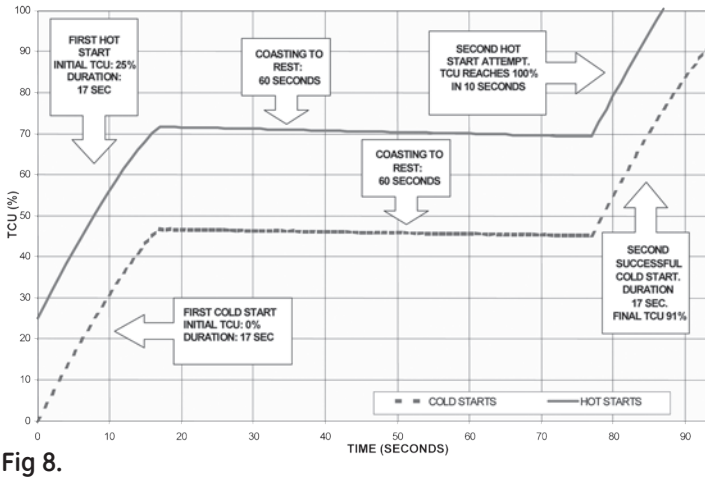

Fig 8.
Hot and Cold Consecutive Starts

Sequence 5: Cyclic load

According to considerations discussed in a previous section of this paper, the main criterion for a thermal model's adequate response to cyclic load is the matching of the implied heating time-constant to the explicit running cooling time-constant (see equation 24). Let us review a balanced cyclic load (i.e. the effective heating) (equation 16) of 1.

After the cold start, the motor varies the load every 30 seconds at between 20% and 160% of the full-load current. Per equation 24, the running cooling constant is calculated as follows

$$\tau_{cool} = \frac{87.4 \times CM}{60} = \frac{87.4 \times 12}{60} = 17.5(\text{min}) \qquad (33)$$

In order to provide a more accurate thermal model response to cyclic load conditions, the cooling time-constant should be adjusted to the calculated value. At the same time this change (from 20 to 17.5 minutes) would cause no significant impact to the other motor operating sequences.

Figure 9 demonstrates the importance of cooling constant value in the thermal model response to cyclic load conditions.

Three cases are shown for a cycling load with an approximate per unit effective heating value of one. In the first case, the cooling time-constant is set long, resulting in over-protection and premature thermal model triggering. In the second case, the cooling time-constant is set to match the implied time-constant of the curve multiplier, and the thermal model adequately responds. In the third case, the cooling time constant is set short, resulting in under-protection and possible motor overheating.

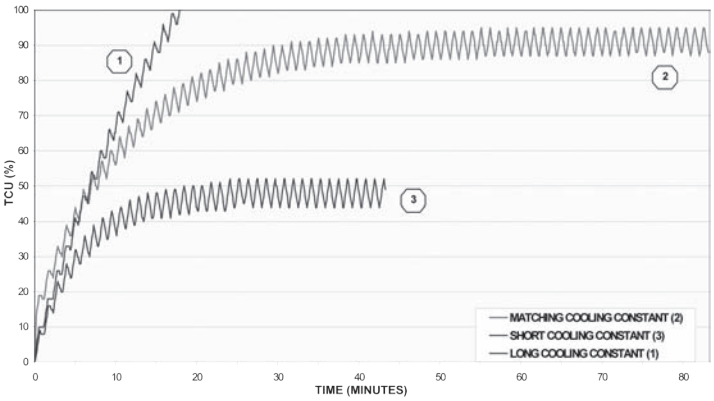

Fig 9.
Thermal model response to cyclic load

Sequence 6: Starting of high inertia loads

The thermal model algorithm has an additional enhancement that allows the coordination of protection with high-inertia long starts, while acceleration time is greater than the safe motor stall time. The voltage-dependant dynamic thermal limit curve is employed to account for varying thermal limits corresponding to the acceleration current levels at the different terminal motor voltages.

Figure 10 shows an example of a 100% voltage high inertia start

lasting 17 seconds (curve 1), and a locked rotor time limit of 8 seconds (curve 4). Actually curve 4 implies the line of the same I^2T. In many short motor start applications it is reasonable to conservatively approximate that the thermal limit remains the same during motor acceleration. In the short start applications an error introduced by this assumption doesn't prevent the motor from successfully starting. The thermal limit curve is thus constructed from sections 2, 3 and 4. If the same approach is applied to the case shown on Figure 10, it will result in the TCU reaching 100% in the middle of the acceleration (Figure 11, curve 1).

As we mentioned in previous sections of this paper, as the thermal limit is a function of motor speed during acceleration, the acceleration thermal limit (curve 5) shows up differently from the locked rotor limit. Each point on curve 5 corresponds to current value which, in turn, corresponds to motor rotation speed during startup. Based on this, we can indirectly find the reference between motor speed and thermal limit, and construct an updated motor thermal limit curve which will include sections 2 and 5 shown on Figure 10.

The new curve helps achieve a successful motor start (Figure 11, curve 2) despite the fact that locked rotor safe time is shorter than acceleration period. The protection method described above is relevant for an ideal situation with a constant terminal voltage of 100%.

In reality the system voltage can deviate from 100% because of the voltage drop during motor startup. The locked rotor current (LRC) is almost directly proportional to the voltage applied to the motor terminals during acceleration, this fact must be taken into consideration when the acceleration portion of the thermal limit is used in the thermal model algorithm.

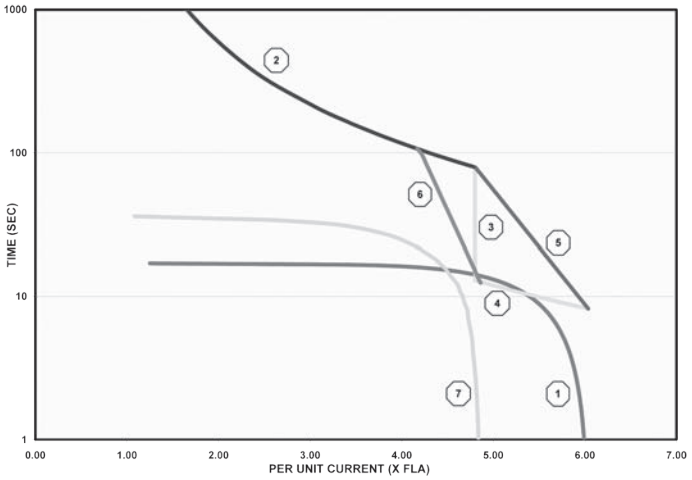

Fig 10.
Voltage Dependent Thermal Limit Curves

For example, for a 100% voltage start (Figure 10, curve 1) the locked rotor thermal limit is calculated based on a LRC of 6 times full load current (FLC) and 8 seconds of the allowed locked rotor safe time, and I^2T is equal to 288. After 14 seconds the motor accelerates to approximately 80% of the rated speed and the current drops to the level of 4.8 times that of FLC.

The allowed time to withstand 4.8 FLA for this stage of acceleration is 40 seconds; I^2T=922. Now let us consider the same application reduced to 80% voltage start (Figure 10, curve 7). LRC at 80% is 4.8 times of FLC. From the 100% voltage case we know that the locked rotor condition is referenced to the thermal limit of 288, and the allowed locked rotor safe time for an 80% voltage start yields 12.5 seconds, but according to the acceleration thermal limit curve (Figure 10, section 5) the thermal limit time corresponding to 4.8FLC is 40 seconds which is much higher than the allowed value. This means that if the

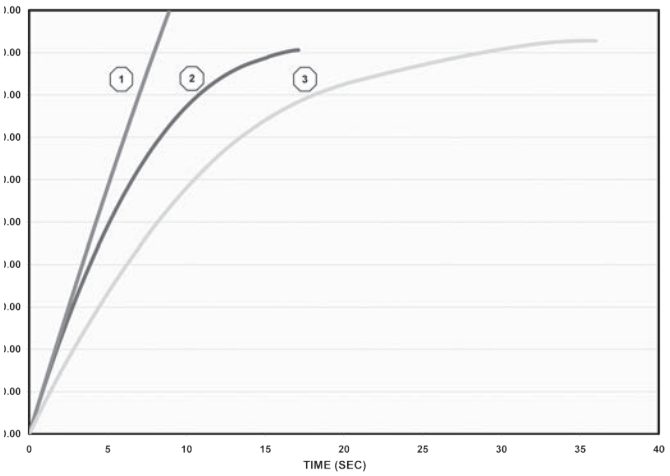

Fig 11.
Thermal Model Response to High Inertia Load Starts

motor stalls under the reduced voltage conditions it becomes underprotected and appears to be in real danger of burning.

To handle this situation the thermal model is equipped with a mechanism capable of dynamically responding to voltage variations during motor startup. Line 6 on Figure 10, shows the new position of the acceleration curve 4, shifted in response to the voltage reduction to 80%. The successful start under these operational conditions is shown on Figure 11, curve 3.

This technique provides adequate thermal protection in cases of high-inertia load application. In some cases where the thermal limit difference between locked rotor and acceleration conditions is not clearly identified, this element should be supported with a zero speed sensor.

6. Application Description

This case study examines the Induced Draft (ID) fan application on the A. B. Brown Unit 2 Selective Ccatalytic Reduction (SCR) Project, located in Evansville, Indiana. Unit 2 is owned by Vectren Corporation, and the role of Black & Veatch (B&V) on this project was to construct an SCR facility in this plant.

The SCR Project Scope of Work included modifying both ID fans for catalyst draft losses. The motors were powered from 13.8 kV switchgear.

Motor ratings and data

Motor Parameter	Value
Motor Horse Power	5500 HP
Rated Voltage	13200 V
Phases	3
Motor Full Load	893 RPM
Service Factor	1.15
Frequency	60 Hz
Rated Full Load Current	226 A
Rated Locked Rotor Current	1205 A
Insulation Class	F
Ambient Temperature	43° C
Temperature Rise @ SF=1.0	77° C
Temperature Rise @ SF=1.15	87° C

Table 3.
Basic Motor Data

Table 3 presents the motor information pertaining to the ID fan motors.

Motor starting and thermal characteristics

The motor manufacturer provided the thermal limit curve under locked rotor, acceleration, and running overload conditions, as well as time-current curves during acceleration at rated voltage and at minimum specified starting voltage. Some of the important motor characteristics (from the manufacturer's data sheet and curves) are summarized in Table 4.

Motor Data		Value
Description	Voltage	
Acceleration time @ Rated Voltage in Seconds	100%	28.0
Acceleration time @ minimum Voltage in Seconds	80%	53.0
Cold Locked Rotor Safe Stall Time @ rated voltage and ambient temperature in seconds	100%	26.0
Cold Locked Rotor Safe Stall Time @ min voltage and ambient temperature in seconds	80%	47.0
Hot Locked Rotor Safe Stall Time @ rated voltage at service factor load operating temperature in seconds	100%	23.0
Hot Locked Rotor Safe Stall Time @ min voltage at service factor load operating temperature in seconds	80%	42.0
Maximum Starts Per Hour	N/A	2
Maximum Cold Consecutive Starts @ rated Voltage	100%	2
Maximum Cold Consecutive Starts @ min Voltage	80%	2
Maximum Hot Consecutive Starts @ rated Voltage	100%	1
Maximum Hot Consecutive Starts @ min Voltage	80%	1
Running Cooling Time Constant in minutes	N/A	9
Initial / Modified (during Startup) Stopped Cooling Time Constants in minutes	N/A	16 / 12

Table 4.
Motor Starting and Thermal Limit Characteristics

Protection philosophy

The ID fans on the A. B. Brown Project are fed from a 13.8 kV auxiliary electric system and are protected by a multifunction motor protection device (MPD). The fundamental philosophies used in setting the MPD are as follows:

- The relay provides thermal protection of the motor during abnormal starting or running conditions, preventing thermal damage to the motor (i.e., the MPD curve is placed below the motor thermal damage curves).
- The relay allows the motor to be started successfully without nuisance trips, in accordance with the number of starts and thermal/cooling characteristics recommended by the manufacturer
- The relay settings allow proper coordination with the respective tie and main circuit breakers on the 13.8 KV bus to which the motors are connected.

Typically the B&V specifications require the motor design to meet the following criterion:

"Motor safe stall time at minimum starting voltage shall not be less than motor acceleration time at minimum starting voltage, plus 2 seconds." The motor manufacturer could not meet this requirement for this high-inertia application and indicated that a speed switch would be provided in lieu of this requirement. The speed switch option was not used because the MPD provided a range of setting options for the overload feature. The MPD was originally set using the custom overload curve feature to match the motor characteristics, in addition to all the above listed protection criteria.

Problems during startup of ID fans

The problem that the commissioning team faced during startup was that the successive motor start-time delays determined by the MPD thermal model were inconsistent with what was allowed by the motor manufacturer. The motor data sheet allowed the following operational characteristics:

- Two successive cold starts or one hot start.
- Following this sequence a new start would be allowed after any of the following:
  - A cooling period of 40 minutes if the motor was running at service factor load and then stopped.
  - A cooling period of 10 minutes if the motor was running unloaded and then stopped.
  - A cooling period of 20 minutes if the motor was de-energized, coasted to rest, and left idle.

It was observed that the MPD was delaying restart by 40 to 43 minutes after every start attempt, regardless of whether it was a second cold restart or the first hot restart. This performance was unacceptable to the client who wanted reliable cold starting as well as a restart time consistent with that indicated by the motor manufacturer. Some of the motor parameters recorded in the MPD during the startup of one of the fans are as follows:

- Hottest RTD Values: 70° C.
- Learned Starting Current: 1.085 A.
- Average Motor Load: 60 percent of the rated current.

It was also noticed that the MPD thermal model was accumulating almost all the available thermal capacity even during the first cold successful start, thus preventing

the motor from performing a successive start. The MPD did not allow a restart for 40 to 43 minutes because of the start-inhibit feature that prevented further restarts when the available thermal capacity was not sufficient for a successful start. This performance was found to be inconsistent with the motor manufacturer's recommendations. B&V requested the involvement of the motor and relay manufacturers to resolve this apparent problem.

Solution to the problem

B&V closely coordinated with all the parties, and the following measures were put in place in sequence:

- The motor manufacturer provided the following recommendations regarding the thermal model settings of the MPD:
  - Use the voltage-dependent overload curve option available in the MPD, and set it with reference to the motor thermal damage curve.
  - To better model the motor during the 9 minutes of coast-down period, decrease the stopped cooling time-constant to 12 minutes.
  - Decrease the safety margin in the start-inhibit function to shorten the lockout time between starts. (The safety margin was changed from 25 to 5 percent.)
- Acting on these recommendations, the relay manufacturer, B&V, and the motor manufacturer collaboratively reviewed the motor protection coordination and relay set points. The following actions were taken:
  - The relay overload curve was changed to the voltage dependent overload curve, with the revised relay points on the hot thermal curve for the starting zone.
  - The stopped cooling time-constant was programmed as 12 minutes, reduced from 16 minutes.
  - Acceleration time was changed to 35 seconds because the motor was observed to start and accelerate satisfactorily within approximately 28 seconds.
  - The thermal capacity used margin set point was changed from 25 to 5 percent.
  - The jogging block function was left on, and the maximum number of starts was programmed to be 2; time between starts was programmed to 0.
  - The restart block was enabled and set to 10 minutes (600 seconds) to comply with the motor requirements of coasting to rest (9 minutes) after being de-energized, before the new start would be allowed.
  - The RTD bias of the thermal model was disabled because it was inappropriate for this application. It is important to mention here that B&V, as part of the control design, always programs an alarm in the relay for high temperature based on RTD inputs.
  - The thermal capacity alarm level setting was left at 85 percent to be readjusted later if required.

Did it work?

The synergistic efforts to problem solving between B&V, the relay manufacturer, and the motor manufacturers paid off. The implementation of voltage-dependent overload curves resolved the issue of unreliable motor starting, and the motor successive restart time delay was reduced to around 20 minutes to the satisfaction of the client. The fans have been successfully commissioned and are now running without problems at the A. B. Brown plant.

Lessons Learned from This Experience

The cited case study highlights the need for flexibility and collaboration between all parties and, above all, a customer-oriented approach to relay coordination studies for complex motor applications. The following are some of the salient lessons:

- The relay application engineer should obtain accurate information about the motor before designing the relay settings. In this respect, it is important that the motor's certified acceleration curves provided by the motor vendor match actual conditions. In addition, the proper cooling time-constants recommended by the motor manufacturer, must be programmed into the relay so that motor behavior may be simulated accurately.
- The motor manufacturer must be consulted and requested to concur on overload relay selection curves in applications where the motor starting curves and the thermal damage curves are very close to one other. The solution that was arrived at in the A. B. Brown case study, where a portion of the overload curve was set on the motor thermal curves, would not have been possible without the motor manufacturer's concurrence.
- All efforts must be made to achieve safe operation of the motor and adequate coordination with other devices and, at the same time, meet the operational expectations of the application.

7. Conclusions

The modern industrial marketplace has a strong demand for a simple, reliable, accurate, multifunctional MPD designed in accordance with industry standards. The major element of a MPD is the thermal model, which must create an accurate image of the motor thermal conditions at any stage of the protected machine's operation.

Theoretical considerations prove that a simplified thermal model based on an equivalent single time-constant model, and overload curves matching motor manufacturers standards for thermal limits, can provide adequate protection at a level of accuracy desirable for this type of application. It can be clearly demonstrated that if the implied thermal constant of the overload curve matches the explicit cooling constant of the running motor, the relay algorithm computes the correct thermal image of the motor during a cycling load.

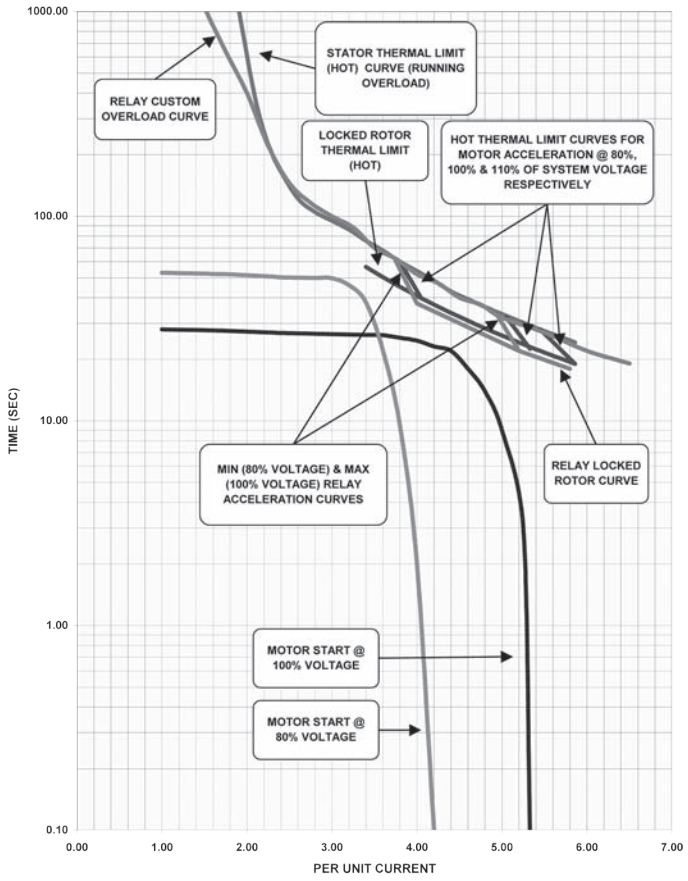

Fig 12.
Coordination of ID Fan Motor Thermal Limit Curves and MPD Thermal Protection Curves.

A detailed explanation of the thermal algorithm actually provides the tools required to calculate the thermal capacity for literally any application. In many cases, it is useful to evaluate thermal model behavior before motor energizing and compare the results with operation restrictions dictated by the motor manufacturer. Analysis of typical motor sequences based on real motor specification data shows how the thermal model algorithm implemented in an MPD can successfully handle excessive motor operation duty and avoid stator and rotor overheating as well as premature machine tripping because of thermal overestimation.

Thousands of motor protection systems employing the proposed thermal algorithm have been successfully installed in various motor applications. However, in a few instances, the setting of motor thermal protection is not as straightforward as it is in the majority of cases.

The A. B. Brown case study presents a unique situation where the close coordination between the parties involved (the end-user, the application engineer, the relay manufacturer and the motor manufacturer) allowed the refinement of application-related information so that proper thermal protection and coordination during commissioning could be provided.

8. References

[1] Sam F. Farag and M. K. Jhaveri, "Intelligent Microprocessor-Based Devices Provide Advanced Motor Protection, Flexible Control, and Communication in Paper Mills" IEEE Transactions On Industry Applications, Vol. 33, No. 3, May/June 1997.

[2] Gabriel J. Paoletti and Alex Rose, "Improving Existing Motor Protection for Medium V oltage Motors", *IEEE Transactions On Industry Applications,* Vol. *25, No.* 3, May/June 1989.

[3] Motor Reliability Working Group, "Report Of Large Motor Reliability Survey Of Industrial And Commercial Installations, Part I". *IEEE Trans. Ind. Appl.,* vol. IA-21, no. 4, pp. 853-864, July/Aug. 1985.

[4] James H. Dymond, "Stall Time, Acceleration Time, Frequency of Starting: The Myths and The Facts" *IEEE Transactions On Industry Applications,* Vol. *29, No.* 1, Jan/Feb 1993.

[5] Sam F. Farag, Robert G. Bartheld, and William E. May, "Electronically Enhanced Low Voltage Motor Protection and Control," *IEEE Industrial and Commercial Power Systems Conference, May 1993, pp. 166-174.*

[6] David R. Boothman et al, "Thermal Tracking – A Rational Approach to Motor Protection", T74 029-5, IEEE PES Winter Meeting, 1974.

[7] Emanuel L. Brancato, "Estimation of Lifetime Expectancies of Motors", IEEE Electrical Insulation Magazine, Vol. 8 No. 3, May/June 1992.

[8] B. H Moisey, "Concepts of Motor Protection. Edmonton, Alberta, 1997.

[9] IEEE Guide for AC Motor Protection. Std C37.96-2000.

[10] IEEE Guide For the Presentation of Thermal Limit Curves for Squirrel Cage Induction Machines. Std 620-1996.

[11] NEMA Standards Publication No. MG 1-1993. Motors and Generators.

[12] Grainger, L.G.; McDonald, M.C. **"**Increasing refiner production by using motor thermal capacity for protection and control", *IEEE Transactions On Industry Applications, Volume: 33 , Issue: 3 , May-June 1997.*

[13] GE Multilin, "Setting The 469 Motor Management Relay for A Cycling Load Application", *GE Publication GET-8478.*

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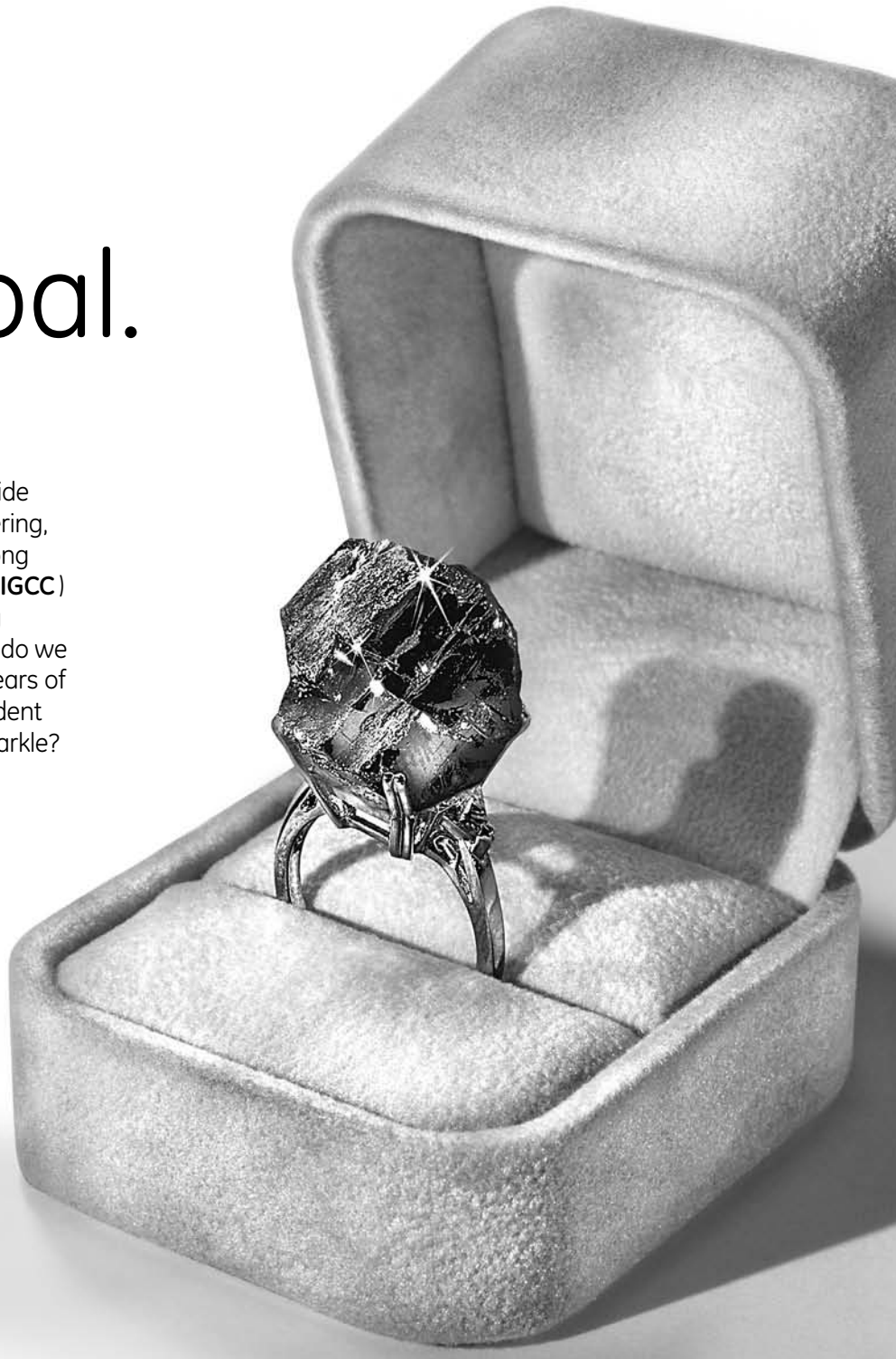

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Synchrophasors: Definition, Measurement, and Application

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1. Abstract

The concept of using phasors to describe power system operating quantities dates back to 1893 and Charles Proteus Steinmetz's paper on mathematical techniques for analyzing AC networks[1]. More recently, Steinmetz's technique of phasor calculation has evolved into the calculation of real-time phasor measurements synchronized to an absolute time reference.

Although phasors have been clearly understood for over 100 years, the detailed definition of a time-synchronized phasor has only recently been codified in the IEEE 1344 and the soon-to-be voted IEEE C37.118 Synchrophasor for Power Systems standards. This paper will review the concept of a phasor and examine the proposed IEEE standard as to "how" a synchronized phasor is to be defined, time stamped, and communicated.

The paper will then examine the issues of implementing such measurements in the face of off-nominal frequency components, timing errors, sensor errors, and system harmonics. Simulations of various system transients and their phasor responses will be presented. Finally, this paper will review the application of synchrophasors to observe power system dynamic phenomena and how they will be used in the real-time control of the power system. Examples of system disturbances will also be presented.

2. Introduction

As the electric power grid continues to expand and as transmission lines are pushed to their operating limits, the dynamic operation of the power system has become more of a concern and has become more difficult to accurately model. In addition, the ability to effect real-time system control is developing into the need to prevent wide scale cascading outages.

For decades, control centers have estimated the "state" of the power system (the positive sequence voltage and angle at each network node) from measurements of the power flows through the power grid. It is very desirable to be able to "measure" the system state directly and/or augment existing estimators with additional information.

Alternating Current (AC) quantities have been analyzed for over 100 years using a construct developed by Charles Proteus Steinmetz in 1893, known as a "phasor." On the power system, phasors were used for analyzing AC quantities assuming a constant frequency. A relatively new variant of this technique that synchronizes the calculation of a phasor to absolute time has been developed[2], known as "synchronized phasor measurement" or "synchrophasors." In order to uniformly create and disseminate these synchronized measurements, several aspects of phasor creation had to be codified3. The following spells out the definitions and requirements that have been established for the creation of synchronized phasor measurements.

3. Synchrophasor Definition

An AC waveform can be mathematically represented by the equation:

$$x(t) = X_m \cos(\omega t + \phi) \qquad \text{Eqn 1}$$

where: X_m = magnitude of the sinusoidal waveform

$\omega = 2 * \pi * f$ where f is the instantaneous frequency

ϕ = angular starting point for the waveform

Note that the synchrophasor is referenced to the cosine function. In a phasor notation, this waveform is typically represented as:

$$\overline{X} = X_m \angle \phi$$

Since in the synchrophasor definition, correlation with the equivalent RMS quantity is desired, a scale factor of $1/\sqrt{2}$ must be applied to the magnitude which results in the phasor representation as:

$$\overline{X} = \frac{X_m}{\sqrt{2}} \angle \phi$$

Adding in the absolute time mark, a synchrophasor is defined as the magnitude and angle of a cosine signal as referenced to an absolute point in time as shown in Figure 1.

In Figure 1, time strobes are shown as UTC Time Reference 1 and UTC Time Reference 2. At the instant that UTC Time Reference 1 occurs, there is an angle shown as "$+\theta$" and, assuming a steady-state sinusoid (i.e. – constant frequency), there is a magnitude of the waveform of X_1. Similarly, at UTC Time Reference 2, an angle, with respect to the cosine wave, of "$-\theta$" is measured along with a magnitude or X_2. The measured angle is required to be reported in the range of $\pm \pi$. It should be emphasized that the

synchrophasor standard focuses on steady-state signals, that is, signals wherein the frequency of the waveform is constant over the period of measurement.

In the real world, the power system *seldom* operates at exactly the nominal frequency. As such, the calculation of the phase angle, θ, needs to take into account the actual frequency of the system at the time of measurement. For example, if the nominal frequency is 59.5Hz on a 60Hz system, the period of the waveform is 16.694ms instead of 16.666ms – a difference of 0.167%.

The captured phasors are to be time-tagged based on the time of the UTC Time Reference. The Time Stamp is an 8-byte message consisting a 4 byte "Second Of Century – SOC", a 3-byte Fraction of Second and a 1-byte Time Quality indicator. The SOC time-tag counts the number of seconds that have occurred since January 1, 1970 as an unsigned 32-bit Integer. With 32 bits, the SOC counter is good for 136 years or until the year 2106.

With 3-bytes for the Fraction Of Second, one second can be broken down into 16,777,216 counts or about 59.6 nsec/count. If such resolution is not desired, the proposed standard (C37.118) allows for a user-definable base over which the count will wrap (e.g. – a base of 1,000,000 would tag a phasor to the nearest microsecond).

Finally, the Time Quality byte contains information about the status and relative accuracy of the source clock as well as an indication of pending leap seconds and their direction (plus or minus). Note that leap seconds (plus or minus) are not included in the 4-byte Second Of Century count.

4. Synchronized Phasor Reporting

The IEEE C37.118 pending revision of the IEEE 1344 Synchrophasor standard proposes to standardize several reporting rates and reporting intervals of synchrophasor reporting. Specifically, the proposed required reporting rates are shown in Table 1. A given reporting rate must evenly divide

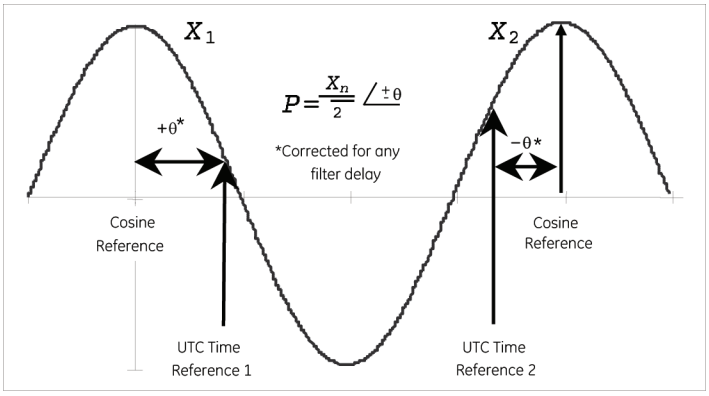

Fig 1.
Synchrophasor Definition

System Frequency:	50 Hz		60Hz				
Reporting Rates:	10	25	10	12	15	20	30

Table 1.
Synchrophasor Reporting Rates

a one second interval into the specified number of sub-intervals. This is illustrated in Figure 2 where the reporting rate is selected at 60 phasors per second (beyond the maximum required value which is allowed by the proposed new standard). The first reporting interval is to be at the Top of Second that is noted as reporting interval "0" in the Figure.

The Fraction of Second for this reporting interval must be zero. The next reporting interval in the Figure, labeled T0, must be reported1/60 of a second after Top of Second – with the Fraction of Second reporting 279,620 counts on a base of 16,777,216.

5. Performance Criteria

The measurement of a synchrophasor must maintain phase and magnitude accuracy over a range of operating conditions. Accuracy for the synchrophasor is measured by a value termed the "Total Vector Error" or TVE. TVE is defined as the square root of the difference squared between the real and imaginary parts of the theoretical actual phasor and the estimated phasor – ratioed to the magnitude of the theoretical phasor and presented as a percentage (equation 2).

$$\varepsilon = (\sqrt{[(X_r(n) - X_r)^2 + (X_i(n) - X_i)^2) / (X_r^2 + X_i^2)]}) * 100 \qquad \text{Eqn. 2}$$

where: X_r and X_i represent the theoretical exact synchrophasor

and: $X_r(n)$ and $X_i(n)$ represent the estimated synchrophasor

In the most demanding level of operation (Level 1), the proposed synchrophasor standard specifies the a Phasor Measurement Unit (PMU) that must maintain less than a 1% TVE under conditions of ±5 Hz of off-nominal frequency, 10% Total Harmonic Distortion, and 10% out-of-band influence signal distortion. The next section examines the issues that result from implementation of the phasor measurement using the classical Discrete Fourier Transform.

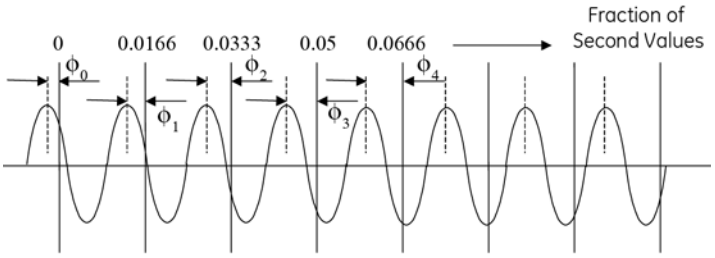

Fig 2.
Synchronized Reporting Intervals

6. Off-Nominal Frequency Effect in a Classical Phasor Estimator

For a classical one-cycle, N samples-per-cycle algorithm, an rms phasor is estimated by the following centered computation:

$$\hat{\mathbf{X}} = \frac{\sqrt{2}}{N} \sum_{k=-\frac{N}{2}}^{\frac{N}{2}-1} x\left[\Delta t\left(k+1/2\right)\right] \cdot e^{-j(k+1/2)\frac{2\pi}{N}}$$

$\hat{\mathbf{X}}$ = one-cycle phasor estimate

Eqns. 3

$$\Delta t = \frac{1}{N \cdot f_{nominal}}$$

$x\left[\Delta t\left(k+1/2\right)\right]$ = current or voltage sample taken at $t = \Delta t\left(k+1/2\right)$

It is assumed that N is even. A 1/2 sample offset is used in both the sampling and the complex exponential to achieve exact centering around the on-time mark.

Suppose that the samples are from a single frequency component, not necessarily at the nominal frequency, with a phase angle measured with respect to t=0:

$$x\left[\Delta t\left(k+1/2\right)\right] = \sqrt{2}\,Real\left[\overline{\mathbf{X}} \cdot e^{j(k+1/2)\frac{2\pi}{N}\cdot\frac{f}{f_{nominal}}}\right]$$

Eqns. 4

$\overline{\mathbf{X}}$ = actual, "true", phasor value of the sequence of samples

$f_{nominal}$ = nominal frequency base for fixed rate sampling

f = actual frequency of the sequence of samples

By substituting equations 4 into equations 1, and simplifying, it can be shown that the one-cycle phasor estimate is related to the true value as follows:

$$\hat{\mathbf{X}} = A \cdot \overline{\mathbf{X}} + B \cdot \overline{\mathbf{X}}^*$$

$\overline{\mathbf{X}}^*$ = complex conjugate of $\overline{\mathbf{X}}$

$$A = \frac{\sin\left[\pi \cdot \left(\frac{f}{f_{nominal}} - 1\right)\right]}{N \cdot \sin\left[\frac{\pi}{N} \cdot \left(\frac{f}{f_{nominal}} - 1\right)\right]}$$

Eqns. 5

$$B = \frac{\sin\left[\pi \cdot \left(\frac{f}{f_{nominal}} - 1\right)\right]}{N \cdot \sin\left[\frac{2\pi}{N} + \frac{\pi}{N} \cdot \left(\frac{f}{f_{nominal}} - 1\right)\right]}$$

The expressions for A and B may seem daunting, but it is possible to draw some conclusions from them. First, it can be seen that as the actual frequency approaches the nominal frequency, A approaches 1 and B approaches zero, so that the phasor estimate is exactly equal to the true phasor value:

when $f = f_{nominal}$ then $A = 1, B = 0$

and $\hat{\mathbf{X}} = \overline{\mathbf{X}}$

Eqns. 6

In other words, when the actual frequency is equal to the nominal, the centered window used in equations 3 produces a phasor estimate that is free from any phase or gain error.

For off-nominal frequency, equations 5 indicates there is both phase and magnitude error. As the actual frequency moves away from the nominal, A drops away from 1, and B moves away from zero - with a positive value for a frequency increase, and a negative value for a frequency decrease - introducing a distortion.

To get a better idea of what the nature of the distortion is, it is useful to recast equations 5 in terms of separate real and imaginary components:

$$\hat{\mathbf{X}} = A \cdot \overline{\mathbf{X}} + B \cdot \overline{\mathbf{X}}^*$$

$$Real\left[\hat{\mathbf{X}}\right] = \left[A + B\right] \cdot Real\left[\overline{\mathbf{X}}\right]$$

$$Imag\left[\hat{\mathbf{X}}\right] = \left[A - B\right] \cdot Imag\left[\overline{\mathbf{X}}\right]$$

Eqns. 7

Equations 7 represent an ellipse. One way to see it is to recast the equations into a more recognizable form:

$$\frac{Real\left[\hat{\mathbf{X}}\right]}{\left[A+B\right]} = Real\left[\overline{\mathbf{X}}\right]$$

$$\frac{Imag\left[\hat{\mathbf{X}}\right]}{\left[A-B\right]} = Imag\left[\overline{\mathbf{X}}\right]$$

$$\left[\frac{Real\left[\hat{\mathbf{X}}\right]}{\left[A+B\right]}\right]^2 + \left[\frac{Imag\left[\hat{\mathbf{X}}\right]}{\left[A-B\right]}\right]^2 = \left[Real\left[\overline{\mathbf{X}}\right]\right]^2 + \left[Imag\left[\overline{\mathbf{X}}\right]\right]^2 = \left|\overline{\mathbf{X}}\right|^2$$

Eqns. 8

Thus it can be seen that the locus of all phasor estimates, for a given phasor amplitude and variable phase angle, is an ellipse with the major and minor axes aligned with the axes of the complex plain. The real and imaginary intercepts of the ellipse are given by:

$$RealIntercept = \left[A + B\right] \cdot \left|\overline{\mathbf{X}}\right|$$

$$ImagIntercept = \left[A - B\right] \cdot \left|\overline{\mathbf{X}}\right|$$

Eqns. 9

As can be seen from equations 3 and 7, the eccentricity of the ellipse worsens as the frequency deviation grows. It can also be seen for small positive frequency deviations that the major axis of the ellipse is aligned with real axis. For small negative frequency deviations the major axis of the ellipse is aligned with the imaginary axis.

Further examination of equations 5 and 9 also reveals that the magnitude of the phasor estimate "shrinks", because A is always less than 1 for off-nominal operation. Figure 3 shows the outline of the rotating phasor for a 55Hz input signal.

7. Out-of-Band interfering signals

Out-of-band signals are those signals occurring on the power system that typically fall in the 0 to 60 Hz range, but specifically those signals that will be aliased if the reporting phasor data rate is too slow for the phenomena being observed. For example, a typical power system swing will operate in the 1 to 3 Hz range.

In order to "observe" a 3 Hz signal, the phasor reporting rate must be greater than twice the 3 Hz swing frequency or 10 phasors per second (the lowest proposed standard rate). More specifically, if there is an interfering signal of 10 Hz with 10% magnitude modulation on the AC waveform (see Figures 4A and 4B for examples) and the reporting rate on the PMU is still set for 10 phasors/second, the proposed standard specifies that influence from the interfering signal shall not raise the TVE above the 1% level.

8. System Architecture

As the implementation of phasor measurement proliferates around the world, there are a number of architectural considerations that need to be addressed. First is physical location. It should be noted that, given PMUs with synchronized current measurement capability, complete observability could be obtained by locating PMUs at alternate nodes in the power system grid.

Current flows from a substation could be used to estimate the voltage at remote stations by calculating the $I_1 * Z_1$ voltage drop along the line. In general, it is expected that these values will be correlated through a process equivalent to existing state estimators – only 20 times faster.

The next architectural issues to address are those of communications channels and bandwidth. Bandwidth is driven by the user's appetite for data. For example, choosing a phasor reporting rate of 60 phasors/sec for a voltage, 5 currents, 5 Watt measurements, 5 Var measurements, frequency, and rate of change of frequency – all reporting as floating point values – will require a bandwidth of 64,000 bps. On the other hand, a data reporting rate of 12 phasors/second for 1 voltage, 5 currents, and frequency – reported in 16 bit integer format – can be accommodated over a 4800 bps channel.

In making the choice of channel bandwidth, both present and future requirements should be considered. In particular, the possibility of future closed loop control should be considered in as much as the speed of this control is a function of the available bandwidth.

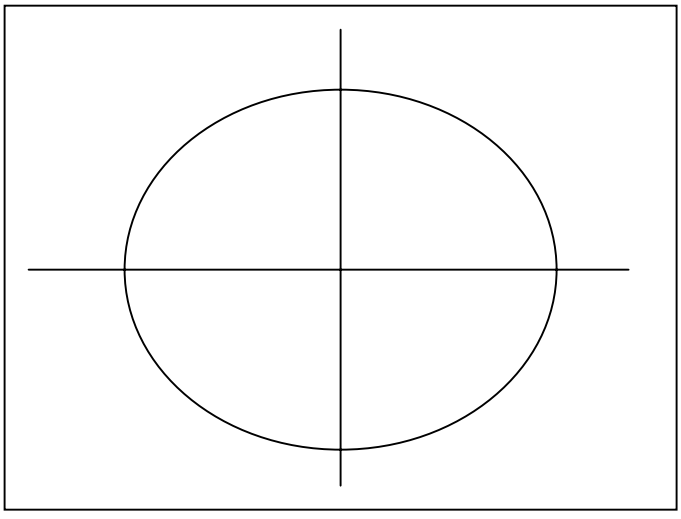

Fig 3.
Classic Fourier Response for 55Hz Input

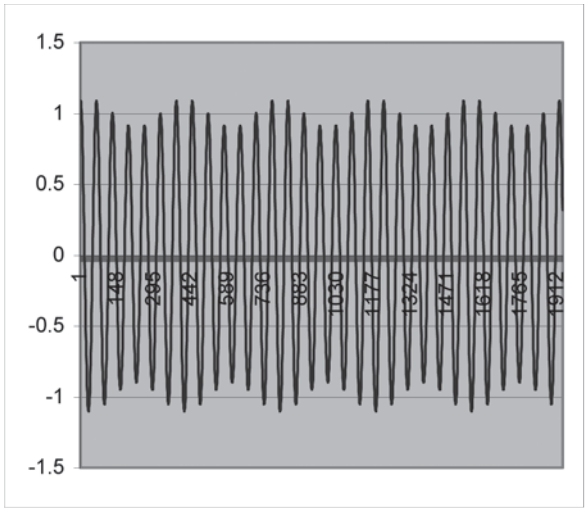

Fig 4A.
10 Hz Multiplicative Interfering Signal

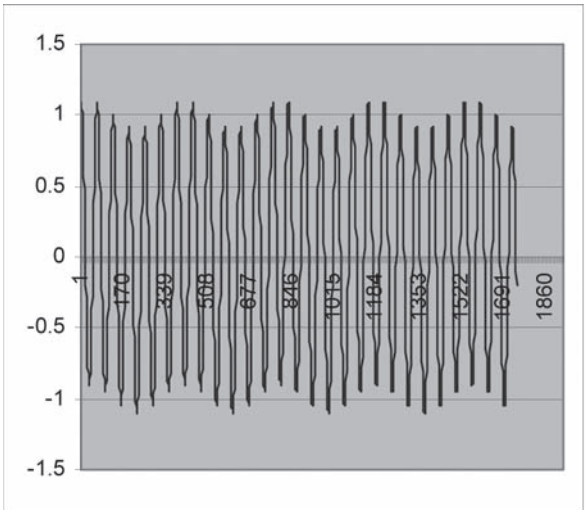

Fig 4B.
10 Hz Additive Interfering Signal

The next architectural choice is that of a physical communication channel. This choice is driven by several functional requirements, namely:

- Bandwidth required
- System availability requirements
- Data availability (i.e. – how many lost packets are tolerable)
- End-user data distribution

These requirements drive a topological architecture as shown in Figure 5.

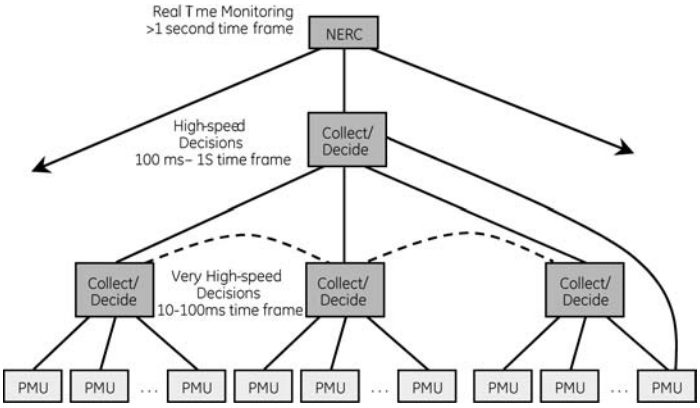

Fig 5.
Synchrophasors Data Collection Topology

In this architecture, there are several data paths shown each of which will require a different data pipe size and characteristic, and there are multiple collection and decision levels that address different operational constraints – the most important being that of speed of response in the case where closed-loop control is involved.

The first line data path is the one from the PMU to a first level Phasor Data Concentrator (PDC) where the data is received and sorted by time-tag from multiple PMUs. Choices for this link include serial data operating with data rates from 9600 bps to 57,600 bps and Ethernet operating at either 10 or 100 MB. Note that the Synchrophasor standard specifies the data format for the PMU to PDC data link. In many cases, communication redundancy may be required or multiple consumers of data may exist.If serial data links are used, either multiple output ports from the PMU must be supported or a multi-drop serial link must be employed. When supporting multiple consumers through Ethernet, either multiple connections must be supported by the PMU or the PMU can support multicast data transmission.

A particularly useful Ethernet construct that facilitates point-to-multi-point communications is that of the Virtual LAN or VLAN. The VLAN construct adds a 12 bit VLAN identifier to every Ethernet data packet. Ethernet switches that support VLAN can read the VLAN tag and switch the data packet to all ports connected on the same VLAN. Since the switching is done at the data link layer, there is a minimum time delay in switching this data through a network.

Data sharing between PDCs at the same hierarchical level, as well as aggregation PDCs at higher levels, will be required. It is expected, however, that data exchange between PDCs will take place at lower data rates of about 10 synchrophasors/second. Although the data rate is 6 times slower (60 vs. 10 phasors per second), aggregated data streams may contain data from 16 to 32 PMUs. For these aggregated data streams, communication transports such as T1, SONET, and Ethernet should be considered.

One other area to address architecturally is that of data exchange between the PDC and the application software. Inasmuch as the application SW will most likely be multi-vendor, architectural guidelines suggest that a standard generic interface would best serve the industry.

The recently released IntelliGrid Architecture4 addresses this issue and recommends the Generic Interface Definition (GID) High Speed Data Access interface for this application. In a practical implementation, this is implemented via the OLE for Process Control standard (OPC). An implementation of this PDC architecture is shown in Figure 6.

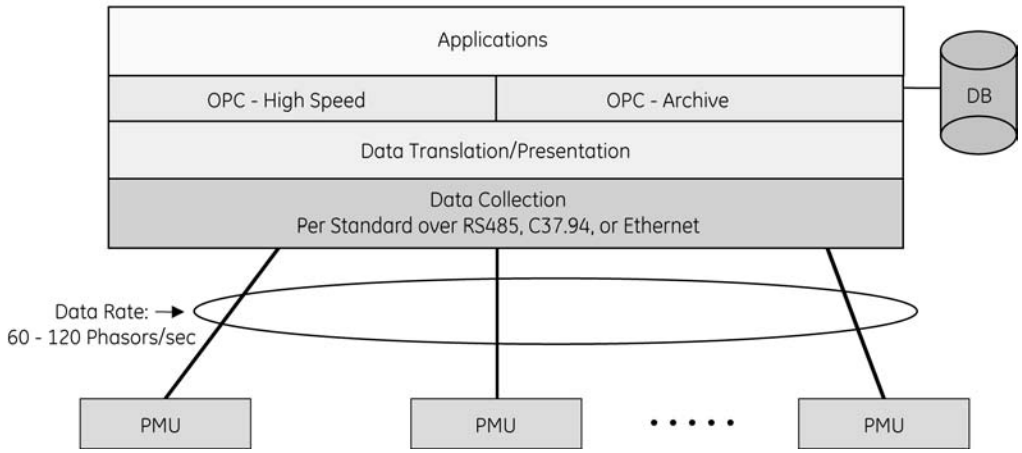

Fig 6.
Phasor Data Concentrator Architecture

9. Applications

The utility industry has taken a 2-phase approach to the development of applications in the synchrophasor domain. Phase 1 (where most of the world is presently operating) is a data visualization stage / problem identification phase. Visualization tools have been developed that look at dynamic power flow, dynamic phase angle separation, and real-time frequency as well as rate of change of frequency displays. Figure 7 is an example of a real-time plot of the voltage phasor. The contour of the surface indicates instantaneous voltage magnitude and the color indicates phase angle with respect to a user-chosen reference angle. At a glance, any depression indicates a Var sync and the color variation (blue to red) indicates instantaneous power flow. In a control room, this graphic could be animated to show undulations in real time due to power swings.

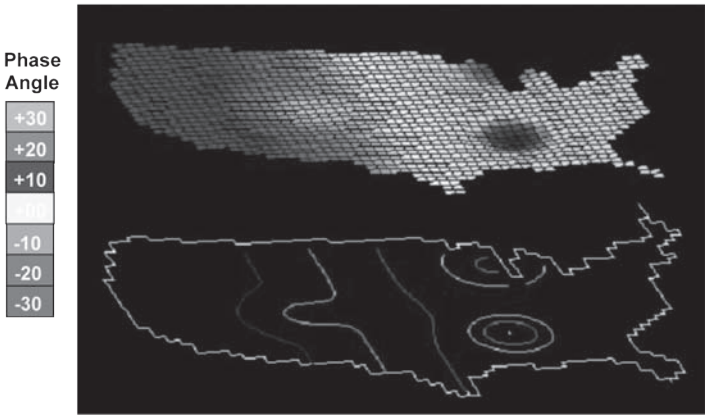

Fig 7.
Wide Area Voltage View Example

Other visualization tools that have been developed include a synchroscope view of all the phase angles, frequency and rate of change of frequency plots, oscillation frequency and damping coefficient plots, and general power flow plots.

Phase 2 involves development of a phasor based closed loop control system (Figure 8). In such a system, aggregated measurements from one or more PDCs is passed to a "decision algorithm" that computes, in real-time, a control strategy and issues the appropriate outputs to the controllable devices located around the system. Control speeds will need to vary, based on the severity of the disturbance. If a potentially unstable power swing is detected, the controller has between ¼ and ½ second to compute and initiate a control action.

On the other hand, if the function being implemented is a system-wide automatic Voltage control algorithm, then a control in the multiple-second range is quite adequate. Other potential control algorithms include inter-area oscillation damping, enhanced power system stabilization, automatic voltage regulation, out-of-step tripping and blocking, and voltage collapse detection and mitigation.

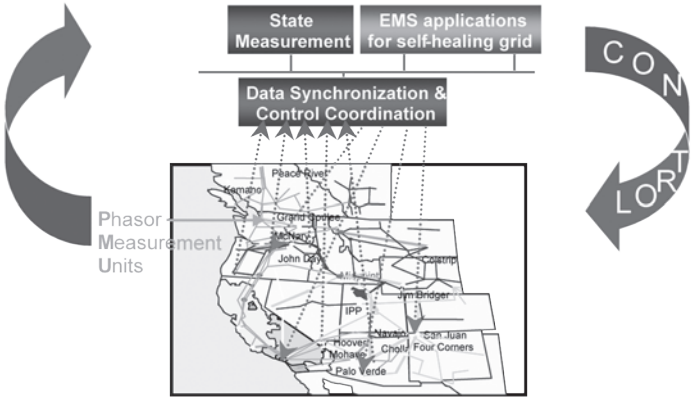

Fig 8.
Closed Loop Power System Control

10. Conclusions

The technology and necessary standards for the measurement and communication of synchronized phasor measurements are becoming available across a range of operating platforms. The need of, and potential applications for, this technology are evolving in parallel; the technology will be called upon to maintain stable operation of the electric power grid of the future.

11. References

[1] Complex Quantities and their use in Electrical Engineering; Charles Proteus Steinmetz; Proceedings of the International Electrical Congress, Chicago, IL; AIEE Proceedings, 1893; pp 33-74.

[2] A New Measurement Technique for Tracking Voltage Phasor, Local System Frequency, and Rate of Change of Frequency; A. Phadke, J. Thorp, M. Adamiak; IEEE Trans. vol. PAS-102 no. 5, May 1983, pp 1025-1038

[3] IEEE Standard for Synchrophasors for Power Systems; IEEE 1344 – 1995.

[4] IntelliGrid Architecture (formerly the Integrated Energy and Communication System Architecture; www.e2i.org.

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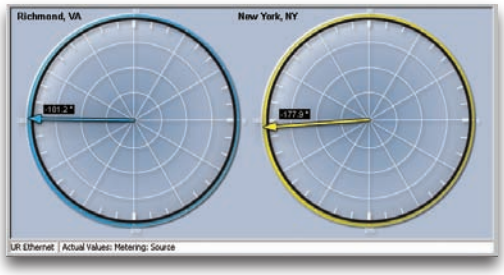

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Implementation and Operational Experience of a Wide Area Special Protection Scheme on the Salt River Project System

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1. Abstract

As existing transmission system infrastructure is challenged to support loads beyond original design limits, the implementation of "wide area" Power System Protection Systems (PSPS) is often required to maintain transmission system integrity. Such a system, with stringent performance and availability requirements, has recently been designed and installed on the Salt River Project (SRP) system. In particular, measurements of generation levels on one side of the system must affect load balance on the other side of the system over 150 miles in less than 1 second.

This paper starts by presenting the need for the PSPS and the resulting design requirements. It then discusses the architecture that resulted from the requirements and the subsequent implementation and testing issues. Actual operation and performance results, including end-to-end timing tests, will be presented. The paper concludes with a discussion of desired improvements in the architecture and new solutions that are available through Generic Object Oriented Substation Events (GOOSE), Virtual LAN (VLAN), and priority messaging technologies that are now available through the IEC61850 communication protocol.

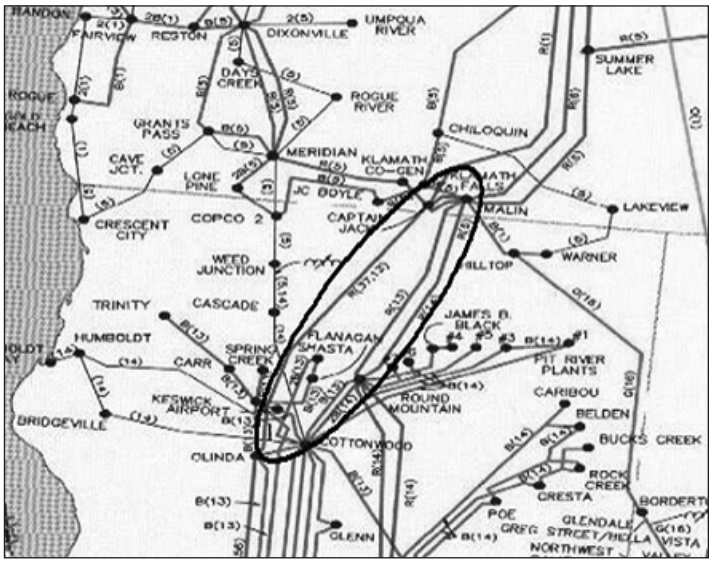

Fig 1.
California-Oregon Intertie Area of Concern

2. Introduction

Palo Verde is the largest nuclear power plant in the western hemisphere and is located approximately 50 miles west of Phoenix Arizona, in the United States. The power plant has three reactors that originally produced 1287 MW each, yielding a total output of approximately 3860 MW. The plant is situated in a transmission corridor that supplies power to the Los Angeles basin and Southern California. Consequently, loss of multiple units at Palo Verde can cause voltage dips, frequency excursions, and cascading problems throughout the Western Electricity Coordinating Council (WECC) region. WECC modeled the loss of two of these units to determine stability guidelines for loss of single blocks of generation in the region. With the originally planned generation output levels, the WECC region remained stable with the loss of 2 units and, as such, no remedial action was needed.

The design of the original units allowed room for augmenting the output of the generators. The owners of Palo Verde decided this additional generating capability and re-rated the output of the generators. This re-rating initiated a new study to review the stability in the WECC region. In the re-study, it was found that the loss of two units plus this upgraded margin caused problems on flows of the California Oregon Intertie (COI – Path 66 – see Figure 1). Specifically, the studies indicated that the loss of these units could cause COI lines to overload and also indicated that the frequency in the region would decay to slightly less than 59.75 Hz. Given this finding, mitigation was required to resolve this problem. Studies showed that shedding the up-rated portion of the generation would mitigate the problem. This required the implementation of a load-shedding scheme to shed only a value of load equal to the upgraded amount. Since the first unit was being upgraded by 120 MW, the system had to shed 120 MW on the loss of two units operating at the up-rated level.

The scheme to implement this load shedding qualified as a Remedial Action Scheme (RAS) by the Western Electric Coordinating Council (WECC). The WECC Region provides a review process of Special Protection Schemes (SPS) or RAS in the region by a Subcommittee. The SC reviews any remedial action scheme that is required to prevent cascading problems from affecting other control areas. The SC also provides a stringent examination for credible failures of the scheme. The scheme

must not have common mode failures that would prevent the successful operation and subsequent mitigation.

The owners needed the solution implemented quickly so that the retail sales of the upgrade could be realized. The quick mitigation scheme that was chosen was to arm a pro-rata share of the ownership (plus some margin for error) to trip at an underfrequency value of 59.75 Hz. This solution was approved by WECC which allowed the owners to proceed and utilize the up-rate of Unit 2. However, each owner assumed a certain risk with this solution as other electrical disturbances in the region could also cause frequency excursions below 59.75 Hz and result in an undesirable load shed. It should be noted that this under-frequency load shed scheme was always "armed" – even when it didn't have to be. The owners wanted to remove this exposure as soon as possible to provide a more dependable and secure solution.

The solution decided on by the owners was to provide an intelligent tripping system that would arm when needed and provide load shedding in various locations throughout the owners control area. It was determined very early that the cost of secure, redundant digital communications across all the owners' territories and across three states was cost prohibitive.

The targeted implementation time was five months and the only practical solution was to implement the load shed in the Phoenix area, as Palo Verde is located only 50 miles to the West of the Phoenix metro area. This decision reduced the scope of the project to a magnitude that could be achieved in the short time frame targeted as SRP's digital communication system was well distributed in this region to allow the load shedding to be dispersed through the metro area and thus reduce the need to drop one large block of contiguous load.

As mentioned earlier, the interim under-frequency load shed solution with relays set at 59.75 Hz was armed at all times and had the potential of operating for non-generation issues. To prevent inadvertent load shed based on frequency alone, logic would be needed that could dynamically measure the unit loading, arm the required amount of load to shed, and only operate the scheme when the proper generation loss criteria were met. This scheme required the relays to measure the generation level of each unit and sum the totals of each pair of units. This sum could be compared to a set point equal to the original output of two units and provide arming if the paired unit loading was exceeded.

As it was neither practical nor desirable to shed one large block of contiguous load, a scheme was designed, using SRP's digital communication system, to allow load to be shed in smaller blocks at many locations throughout the Phoenix metro area. In creating this load-shed scheme, various loading and timing parameters had to be considered. The load profile of each site had to be measured and total load available to shed had to be calculated to insure enough load was available at all times. The common mode failure of the communication system needed to be considered and no single failure could prevent the system from operating. Critical customers would have to be avoided.

The load in the Phoenix area typically reaches a peak in the late afternoon and settles at its minimum values in the early morning hours with a minor peak in mid-morning. The monitored sites were required to provide at least 120 MW of sheddable load at the system minimum and were found to provide up to 650 MW of load at system peak. The system needed to be smart enough to arm and unarm sites as needed and still guarantee that enough sites were available to provide 120 MW of sheddable load when needed. The available load at each site was added together to determine the load profile of the monitored system. As a site was chosen, the monitored load profile would be re-examined to make sure that the required mitigation amount (120 MW) was always available. The overall system arming and load selection logic is shown in Figures 2a and 2b respectively.

Besides the availability of sheddable load in a station, the choice of which substations to select in the shed scheme included the availability of redundant communications. Although most SRP distribution substations contained SONET multiplexers, not all of the nodes were part of a ring that provided redundancy. Ultimately, a site was chosen if it had sufficient load, was not

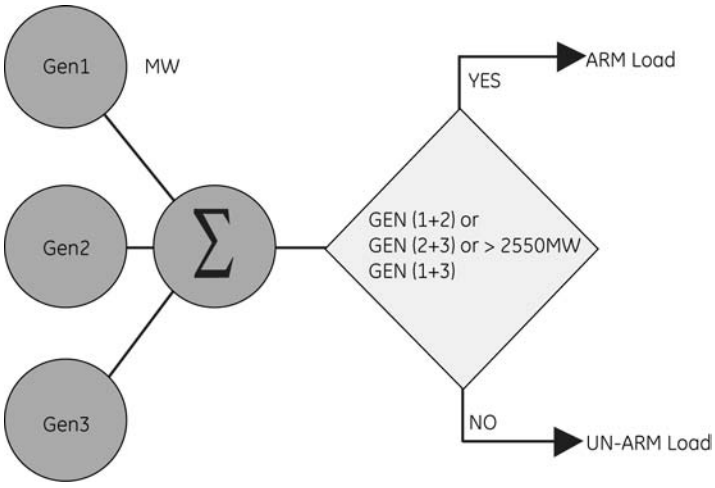

Fig 2a.
Load Shed Arming Logic

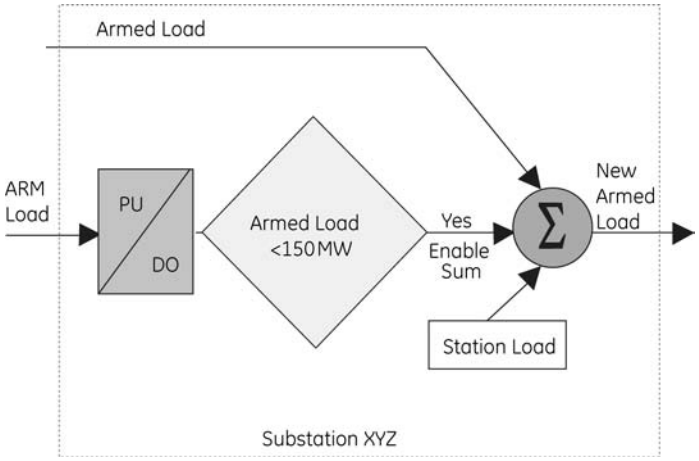

Fig 2b.
Load Calculation Logic

located on another site's communication ring, and did not have any critical customers such as hospitals. The iterative process of choosing sites and examining load and communication ring availability produced a total of 14 sites. These sites provide a total of at least 150 MW of sheddable load at all times. The 150 MW provided a 30 MW margin in case of failure of multiple components, numerical roundoff, or unavailability of sheddable load in a station.

3. System Design

Given the requirements of optimized load shed, high availability, and performance, the system design was centered around the interface of modern measurement relays as connected into SRP's SONET communication system. SONET or Synchronous Optical Network is a fiber-based communication system that is typically built in a ring configuration (see Figure 3). Data from any node in the ring is sent two directions around the ring to the intended receiver(s). If any part of the ring structure fails, the receivers can dynamically switch to the alternate data source in as little as 3 ms. To implement high system availability, redundant measuring relays were implemented – each with redundant communication channels, namely, an Ethernet channel and 64,000 bps synchronous serial communication channels via a G.703 physical interface.

The solution required watt flows to be measured at all 15 sites and then communicated to each site. The power flows at the generator and load centers were input into the measuring relays from 0 to 1ma watt transducers at each location. As the available communication data formats only supported single bit status information, in order to transmit power in this format, it was necessary to scale the computed power into 8-bit integers which could then be mapped into 8 status points in the respective messages.

In the case of the Ethernet channel, the UCA Generic Object Oriented Substation Event or GOOSE (IEC61850 Generic Substation Status Event – GSSE) was used as the message carrier. The GOOSE is a multi-cast message originally designed to carry binary state information among multiple relays connected to the same Ethernet network inside a substation. As a multicast message, the GOOSE can be sent to many other devices through an Ethernet switch (Level 2) but cannot be routed, as the GOOSE message does not contain any routing (Internet Protocol – IP) information. One of the interface options into the SRP SONET multiplexer was an Ethernet card, which acted as a level 2 switch. As such, when connected to the measuring relay, the SONET Ethernet card would accept and carry the multi-cast GOOSE message over the SRP SONET network to any node equipped with an Ethernet card. This application was able to create a "free range", wide area GOOSE.

With the G.703 communication system, each measuring relay had two G.703 – 64000 bps ports which were configured to transmit information out of both ports on a change of state. This capability enabled the G.703 communication path to be configured in a ring. At each of the 14 nodes in the ring, the received data was captured for local use and then repeated for the other devices in the ring to be able to access the transmitted information. The G.703 ring topology enabled the implementation of several communication diagnostics such as ring timing, high packet error rate, and broken G.703 ring detection. Data integrity on both media was ensured by data integrity checking through a 32-bit Cyclical Redundancy Code (CRC).

Both the Ethernet and the G.703 interfaces were connected into the SONET multiplexer system. As some of the rings were only connected with single tie connectors, the communication paths of both communication interfaces were designed to be different to avoid the possibility of a single point failure taking the system down.

To start the scheme process, a decision had to be made as to when to "arm" the system. The criteria, as stated above, was that the total power output of any two units was greater that 2550 MW (see Figure 2a). To implement this function, the power

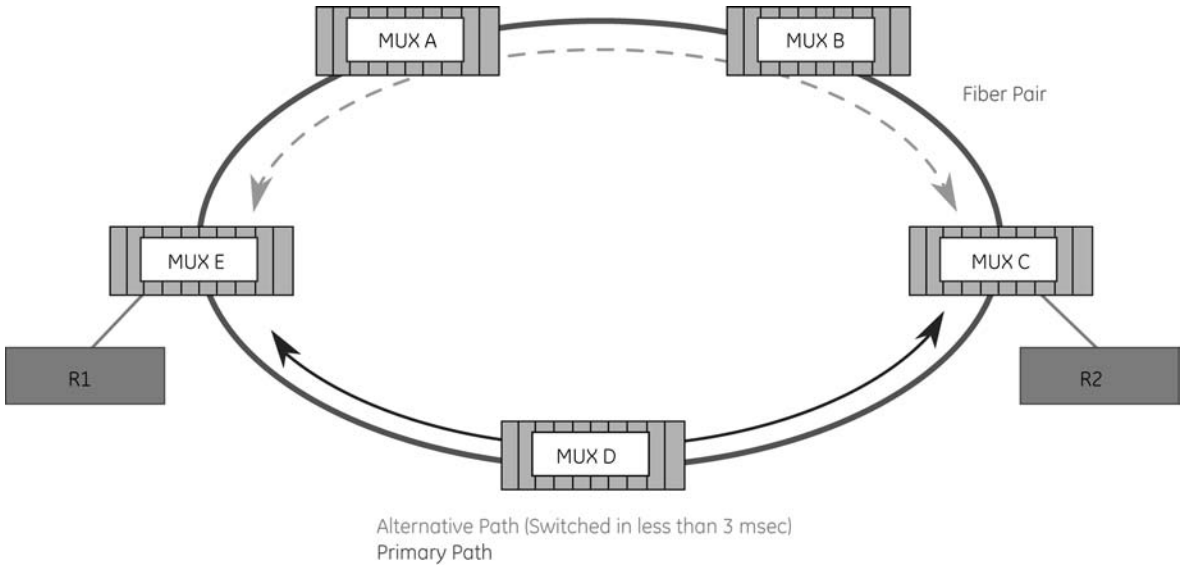

Fig. 3
SONET Concept

output of units 1 and 2, units 2 and 3, and units 1 and 3 was measured and summed. Each power sum was then compared against the arming threshold of 2550 MW. If any of the three combinations of unit power outputs was greater the threshold, an "arming" signal was sent to all the connected substations (14 of them) in the RAS.

Given that an arming signal had been issued and after a programmed delay time, the first unit in the string would "arm" itself to shed load and would then transmit the amount of load it could shed (read from a 0 to 1ma transducer) to the next substation in the string. The "summed" watt value was also transmitted back to Palo Verde where it was compared against the set point of 150 MW (see Figure 2b). If the arming signal was still high after a pre-programmed amount of time, the next substation in the string would then add its MW contribution to the "total" and send the total to Palo Verde. If the total amount of "armed" Watts was greater than 150 MW, the arming signal was turned off.

A "digital summer/comparator" was used to add the various MW values together and to check the limits of the armed load. The sign of the "B" input could be dynamically changed to perform subtraction if desired (see Figure 4). The comparator had a pickup level setting, direction of comparison (over limit/under limit), compare mode (absolute vs. signed), and a hysteresis range. If the summed value of available load reached the required shed value (150 MW), then no more load was sought to arm. As the transmitted data was only 8-bit, only 1% of full-scale could be achieved in a measurement. As such, the quantization limits of the digitizers had to be factored into the set points and summing logic. These numerical limitations resulted in additional load needing to be armed and arming of the system at generation values less that needed.

Given an armed system, "shedding" logic was needed to detect loss of generation at Palo Verde. The shedding logic looked for the tripping of two Palo Verde units within 5 minutes of one another and would then issue a "shed" command. Once initiated, the "armed" devices, based on a pre-calculated schedule, would sequentially open the substation breakers over the course of 1 second. It should be noted that there is no automatic restoration with this system as load restoration must be coordinated with the system security coordinator and the loads are manually restored once permission is given.

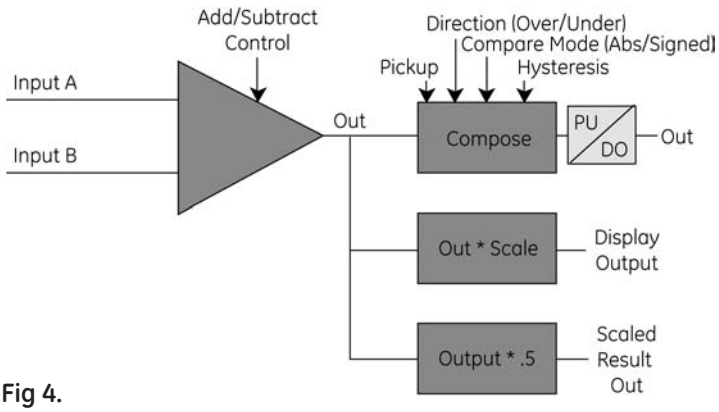

Fig 4.
Summer - Comparator Function

Over the course of the day, the load at the various substations would normally increase and where at the start of the day, 150 MW would have been armed, the armed load would typically increase significantly above this value. To minimize the amount of load armed, when the revamped total exceeded 250 MW, a "disarm" command was issued. Given this command, the selected substations, in reverse sequence, would remove themselves from the shed group thereby minimizing the amount of load shed and maintain an armed load band width of 150 to 250 MW.

The two systems operated independently and the variance of the digitizing and summing features would sometime lead to each system arming and unarming sites at slightly different times. Occasionally each system would get "out-of-sync" and have different sites armed. This was undesirable and would result in the shedding of more load than was needed if a trip occurred. Because each system would maintain the 150 MW of armed load but with different sites. If the two systems became unsynchronized, the operators would have to cycle each system OFF and then ON (one at a time). As the systems powered up they would re-synchronize and once again, arm just the load needed.

4. Implementation Issues/New Solutions

In the initial testing of GOOSE communication, several routers were encountered in the desired paths that prevented passage of the GOOSE message. In contacting Cisco (the router manufacturer) it was discovered that an add-on software package was available known as Cisco's Internetworking Operating System software or IOS. The IOS software package was configurable such that it could be programmed to "bridge" any multi-cast data packets – such as GOOSE. With the IOS properly configured in the routers, GOOSE packets were demonstrated to be switchable throughout the SRP network. In the actual implementation, a "flat" Ethernet ring was constructed such that there were no routers to pass through and, as such, configuration of the IOS software was not needed in this implementation.

Since this system has been installed, a new solution space has been made available through the communication capabilities of IEC61850 GOOSE. IEC GOOSE brings with it several desirable new features for future implementations, namely:

- The ability to directly send analog data values
- The ability to map data onto a VLAN
- The ability to set the priority of the message through a switch

IEC GOOSE [1], in contrast to UCA GOOSE, carries a "user defined" dataset. The dataset can be configured with any "visible" data object in the relay such as volts, watts, vars, breaker status, etc. The data items in the dataset carry the same "type" (such as Float32, Integer 16, Boolean, etc) as the original data item. In the application of transmitting power flows, data, in engineering units, can be easily transferred among all locations as needed.

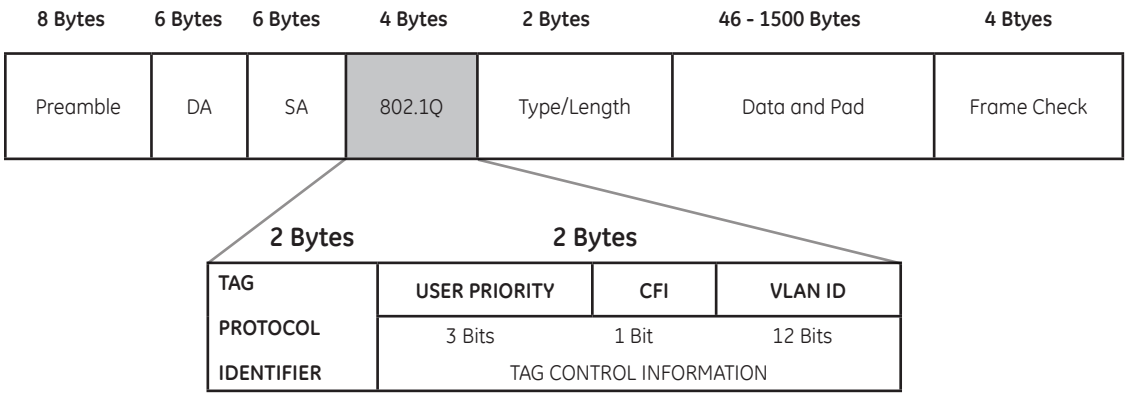

Fig 5.
Extended Ethernet Frame

With UCA GOOSE, when the multi-cast packet left the station, the packet would travel anywhere there was an Ethernet switch. This resulted in GOOSE packets being delivered to more locations than they had to be. A new feature supported in IEC GOOSE is the ability to logically restrict the flow of data to a particular broadcast domain through the creation of a Virtual Local Area Network or VLAN [2]. This dataflow restriction is achieved by adding four bytes to the Ethernet data frame per the IEEE 802.1Q [3] standard (see Figure 5). The extended dataframe is identified by a two-byte Tag Protocol Identifier value of 8100 hex. The other two bytes include 12 bits for a VLAN ID, 3 bits for priority encoding of the Ethernet message, and one bit for backward compatibility with Token Ring. Once identified as an extended Ethernet frame, a device (switch/bridge-router) in the network can decode the VLAN ID or VID. This ID is read by the device and "switched" to those ports programmed with the same VLAN ID. Figure 6 shows the delivery of a message to multiple devices connected to VLAN ID 5.

The third area addressed by IEC GOOSE is that of Ethernet priority in communication. Ethernet has traditionally been known as "non deterministic" in that collisions on a shared wire made the delivery time of a message a random variable. With the introduction of Layer 2 full-duplex switch technology, Ethernet collisions no longer exist. Switches receive all messages and store and forward them to the destination locations as programmed. It is possible for a single port to have several messages queued for delivery which would add a certain amount of delay in the processing of a message. Ethernet priority, however, even removes this delay. Upon receipt of an Ethernet message with "high priority", the received message is moved to the front of the queue and becomes the next message to be input to the receiving device thereby eliminating all processing delay in Ethernet communication.

5. System Performance

As part of system commissioning, round trip time for a message from Palo Verde to several of the remote substations was measured. The timing test involved logging when a message was sent from Palo Verde, receiving the message a remote substation, replying back to Palo Verde, and logging the return receipt in the original sending relay's event log. This test was performed on both the Ethernet and the G.703 communication systems. Results from these tests can be found in Table 1.

Referring to Table 1, the Ethernet System (System B) did not appear to be dependant on distance from the sender to the receiver and typical propagation times recorded were typically 14 ms or less implying a one-way communication time of less than 7 ms (as there is some internal relay processing included in the 14 ms). It should be noted that there was not much traffic on the Ethernet system other than the 15 relays installed for this scheme. Since the original implementation, several devices have been added to the Ethernet system and re-testing of this system will occur this May to see if the propagation delays have changed. The G.703 - System A - was more dependant on channels bank processing and took more time as the sender and receiver were separated by distance and number of channels banks. Each channel bank and relay combination introduced some communication delay time. Overall, both systems performed well within the required tripping time of 1 second.

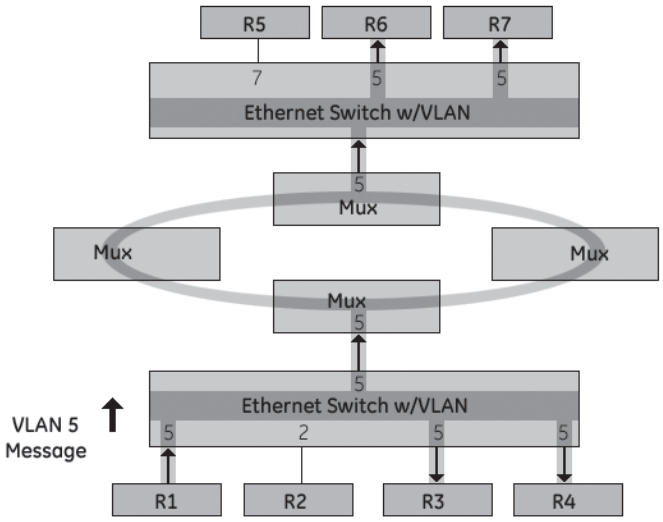

Fig 6.
Track of VLAN Message

6. Testing

The RAS Systems are tested annually from Palo Verde. Normal SRP practice is to schedule maintenance and outages of the RAS through the scheduling coordinator of the Operations Department. This will include notification to the Owners of Palo Verde Nuclear Generating Station (PVNGS), California ISO, and PVNGS itself.

There are three tests that are performed, namely:

- Scheme Checks
- Logic Tests
- End-to-End Tests.

The Scheme Checks verify the wiring, contact continuity, input function, etc., and are used to verify the physical connections to the relay and schematics. The Logic Tests are used to test the settings and logic of each relay. The End-to-End Test verifies that the arming and tripping from Palo Verde to each distribution site is functioning properly.

Each distribution site and Palo Verde are equipped with test switches. These test switches disable tripping and dispatching is automatically notified when the distribution site is placed in the test position. When the test switch is placed in the "test" position at Palo Verde, a signal is sent to the distribution stations that will block the trip contacts from operation. Dispatching is also notified when Palo Verde is placed in the test position.

The End-to-End Test can only be performed when Palo Verde and the site being tested are in the "test" position. There are push buttons for each site located at Palo Verde that can be used to test the transmission of the trip signal (see Installation picture of Palo Verde – Figure 7). The pushbuttons, however, cannot initiate a trip unless the test switches in Palo Verde and the site under test are in the "test" position. Performance of a System Test requires maintenance personnel to be at both Palo Verde and the distribution site being tested.

7. Operational experience

The system has been in service for a year now and has had no false operations, has not been called upon to operate, and properly did not operate during a recent trip-out of the plant.

Station	Ethernet Timing	G.703 Timing
Gaucho	14 ms	11 ms
Alameda	14 ms	20 ms
Indian Bend	14 ms	33 ms
Buckhorn	14 ms	46 ms

Table 1.
Palo Verde to Station Round Trip Communication Timing

8. Conclusions

Utilities are finding themselves drawn to Remedial Action Schemes on their systems. Drivers include the increasing complexity of the power system and the social and economic pressures that inhibit the construction of new power lines. As such, real time control schemes will increasing play a role in maintaining the security, stability, and integrity of the electric power network. Today's digital relays – in close integration with advanced communication networks – promise to provide solutions for remediation of identified power system problems. A tightly linked network of relays was demonstrated to provide an intelligent wide area protection system at a significantly lower cost than building a new transmission line.

Although the system worked well, room for improvement in several areas were identified – many of which are addressed by new technology such as analog data transmission, VLAN, and priority – all of which are enabled by the new IEC61850 communication standard. The tools and infrastructure for implementing Wide Area Protection and Control are here today and promise great things in the future.

9. References

[1.] IEC61850 Communication networks and systems in substations – Part 7-2: Basic communication structure for substation and feeder equipment – Abstract communication service interface (ACSI); www.iec.ch

[2] IEC61850 Communication networks and systems in substations – Part 8-1: Specific Communication Service Mapping (SCSM) –Mappings to MMS (ISO 9506-1 and ISO 9506-2) and to ISO/IEC 8802-3; www.iec.ch

[3] 802.1Q - Virtual LANs;
http://www.ieee802.org/1/pages/802.1Q.html

Palo Verde Installation

Typical Substation Installation

Fig 7.
Installation Pictures

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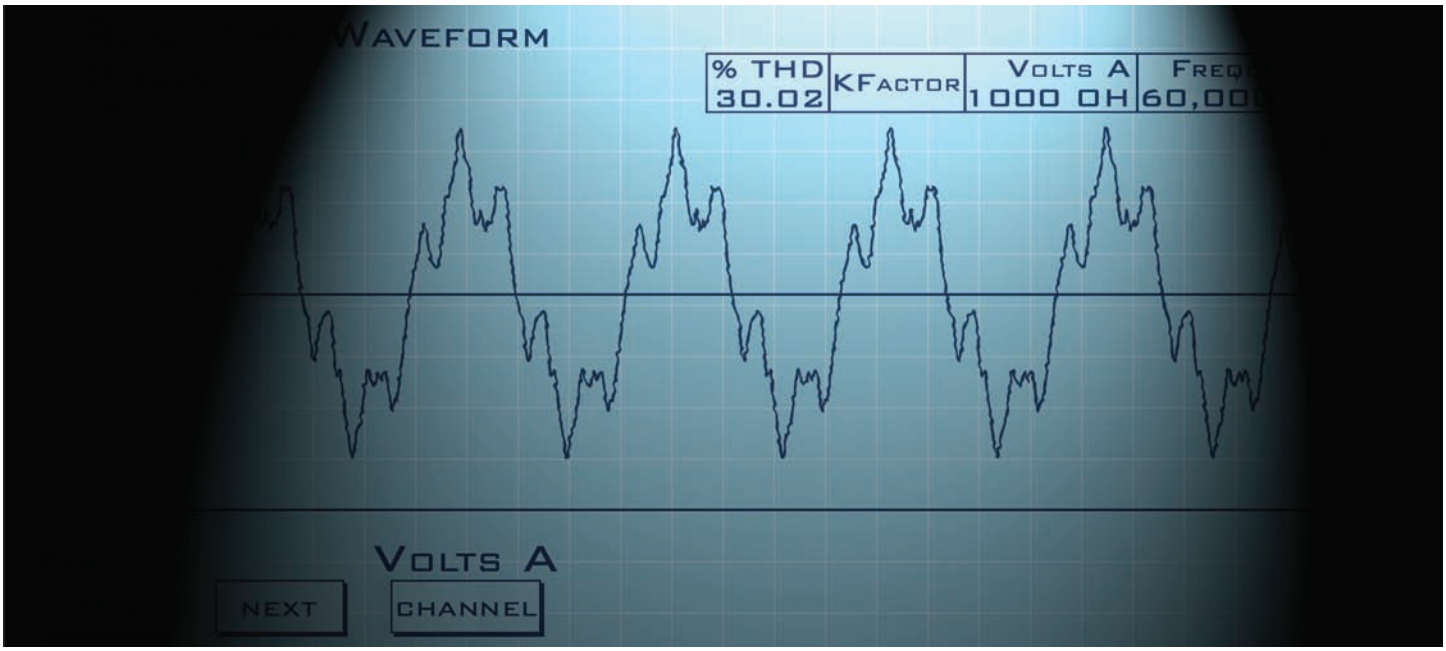

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Applying Digital Line Current Differential Relays Over Pilot Wires

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1. Abstract

Digital current differential protection has the advantages of application simplicity, operation speed, and high sensitivity. Traditionally, current differential protection communication channels are either direct fiber optic cable or multiplexed channels using short copper links from a relay to a multiplexer.

Pilot wire analog differential relays are commonly used for protection of short lines. Many utilities still have copper twistedpair, links with pilot wire relays in service. However, these relays do not meet modern requirements and are can-didates to be replaced. Utilities, however, are reluctant to invest in new communication links to replace existing pilot wires.

This paper presents both problems and practical solutions (for example, modern HDSL communications modems) for applying digital line current differential protection over copper wires.

2. Introduction

Pilot wires are continuous copper connections between substations; however, the pilot wire relays communication pilot wires are not connected directly to existing pilot wires. For protection against GRP, they are connected through insulating transformers or repeaters.

By principle, pilot wire relays are very close to digital current differential relays using the same biased differential principle, same unit protection, and the same need for the pilot channel. The major difference between them is that pilot wire use analog signals while current differential relays digitize analog values into digital quantities transmitted at 64/56 kbps channels.

Both results of extensive testing and successful field ap-plications are presented. As a result, it becomes a very attractive alternative to retrofit existing analog relays with modern microprocessor-based current differential relays utilizing existing pilot wires.

Leased telephone lines are another low-cost alterna-tive. Several problems have to be overcome while applying current differential, using a 64 kbps communications channel over copper wire. Two major problems are noise and ground rise potential protection in the form of isolation transformers.

3. Basics of Pilot Wire Circuitry

The phase sequence network is connected to current trans-formers in the three phases, as illustrated in Figure 1. This network converts the three phase currents from the line current transformers into a single-phase voltage, which is applied to the relay circuits via the saturating transformer.

There are two basic types of pilot wire relays: “circulating current” or “opposed voltage”. “Circulating current” means that current circulates normally between line CTs through pilot wires and “opposed voltage” indicates that current does not normally circulate through pilot wires. Pilot wire relays only use two wires; therefore, it is necessary to derive a representative single-phase quantity. The insulating transformer, mounted inside the pilot wire relay case, acts as an impedance matching device between the relay circuit and pilot wires. The primary winding is connected to the restraint and operate circuits; the two secondary windings are connected in series across the pilot wires as shown in Figure 1. The turns ratio is one to four from the relay side of the transformer to the pilot wire side.

The pilot is a twisted pair of wires connected between two (or three) terminals of the protected transmission line. Insulation capability of the pilot should be based on the maximum induced voltages that may occur in the pilot circuit, with the proper protection installed. The limitation on pilot length is determined by the acceptable magnitudes of the loop resistance and the shunt capacitance. For two-terminal lines, it is recommended that the series resistance of the pilot loop, including the neutralizing reactor windings if present, not exceed 2000 ohms and that the shunt capacitance be less than 1.5 microfarads.

Pilot loop resistance can be based on information supplied by the communication utility if the pilot is leased, or it can be calculated given the wire size and length of the pilot run, using dc resistance data published in wire tables. Pilot loop resistance

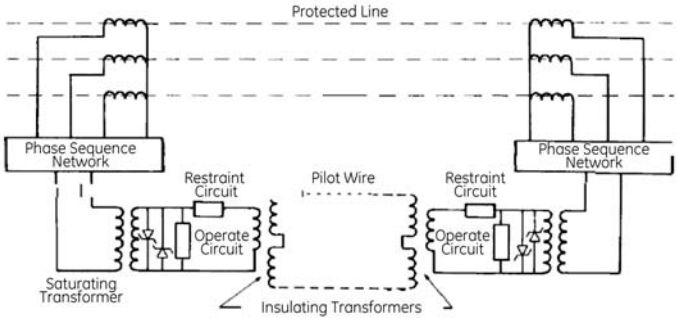

Fig 1.
Pilot wire simplified arrangement

can also be determined by direct measurement from one end with the remote end shorted for two terminal lines, or from each terminal to a short at the junction of the T for three terminal lines. This should be a dc measurement, since the shunt capacitance will influence an ac measurement.

The most likely source of difficulty in an ac pilot wire relaying scheme is the pilot circuit itself. Because the pilot circuit extends over a considerable distance, it is exposed to a number of hazards that can interfere with the proper operation of the scheme or cause damage to the pilot circuit and associated equipment. The most common hazards are:

1. Rise in station ground potential (GPR).
2. Induced voltages.
3. Lightning.

A substantial voltage rise can occur at the substation ground mat relative to the remote ground potential. This voltage rise can cause excessive insulation stresses on the pilot wire relay, the pilot wire monitoring relay, the pilot wires, and between pilot wires and other conductors in the same cable.

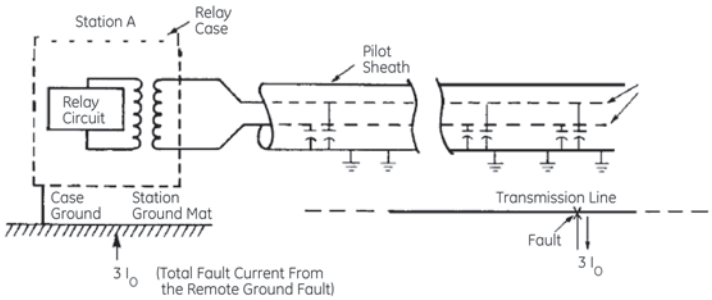

Fig 2.
Station mat.ground potential rise

As illustrated in Figure 2, the typical condition resulting in ground potential rise is a single-phase-to-ground fault on the power system. With ground current flowing through the Station A ground mat, there will be a voltage difference between this mat and the remote ground potential. The magnitude of this voltage depends on the magnitude of the current and on the impedance between the station ground and the remote ground. The value of the ground current is usually available from system fault studies. The impedance between the mat and the remote ground is determinedby calculation or test.

The diagram in Figure 3 represents a typical voltage profile of the potential difference between the pilot cable and ground during a single-phase-to-ground fault. As is apparent from the plot, the potential of earth near the pilot wire cable tends to be at the remote ground potential for most of the length of the pilot run. Hence, if the cable is not grounded, it will assume a potential near that of the remote ground because of the capacitive coupling. Thus, the potential rise of the station ground mat results in a significant voltage difference between the station ground mat and the pilot cable with its connected station equipment. If this voltage difference becomes too great, there is danger to personnel and the possibility of damage to the

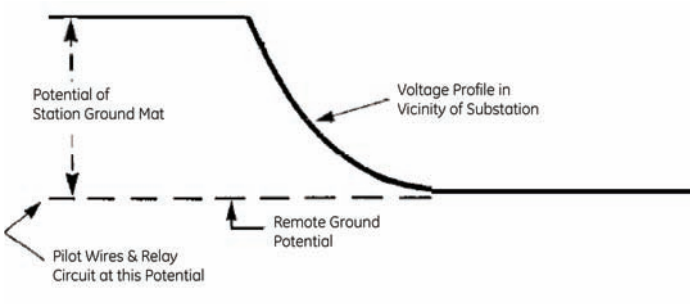

Fig 3.
Typical Ground Potential Profile During SLG Fault

pilot wire relays, the connected equipment, and the pilot wire itself. If this voltage difference exceeds 600 volts, protection of the pilot wires is usually necessary since this is the continuous voltage insulation level of the connected relays, terminal boards, panels and standard telephone cables.

4. Premises for Current Differential

Consider a communication link between two substa-tions that is twisted-pair wire and with all CTs and control wiring on the panels. This requires the ability to pass digital data over pilot wire without hazard and susceptibility to noise that could lead to possible misoperations. The following was successfully employed for current differential applications.

4.1 P31042 56kbs/HDSL Data Isolation Interface

This device is produced by SNC Manufacturing. This standalone transformer provides an isolated interface for two-wire data circuits. It is a passive, magnetic-coupled device. Primary to secondary isolation is rated at 65 kV BIL. Types of data circuits protected include Synchronet services and digital data services operating at 72k bits per second (bps) and subrates (including 72, 64, 56, 25.6, 19.2, 12.8, 9.6, 6.4, 4.8, 3.2 and 2.4 kbps), basic rate ISDN, HDSL, analog signals for data modems, SCADA, tone relay control, analog carrier, and tone signaling up to 100 kHz. The HDSL modem operates at 1024 to 2048 kHz signal. At this rate signal loss is less than 0.1 dBm, which is al-most negligible as a signal attenuation for the modem.

4.2 HDSL modem

There are a variety HDSL modems available on the market. However, not all meet industrial applications requirements. Modems must meet applicable environmental and communications standards to be safely applied for such applications. In general, HDSL modems support different interfaces. For this type of application, an RS422 interface was

chosen; however, other galvanic interfaces like X.21 or G.703 can also be successfully applied. For the RS422 interface, one modem was set to generate a communications clock (Master) while other (Slave) was set to recover the clock from received data from the peer modem.

Set the modem interface as per manufacturer instructions. GE Multilin employed modems made by Schmid Telecommunications (Watson 2 or 3 HDSL modems) and Route 66 Communications, Inc (Crocus HDSL modems, not industrial hardened).

There is a limitation in length of the DSL cable depending on the modem driver and pilot wire gauge. Typical transmit power is 13.5 dBm at 135 Ω line impedance. Note that pilot wire characteristic impedance is 600 Ω at the voice band frequency. At DSL operating frequencies, it is about 120 Ω, which matches HDSL modem input impedance. AWG18 allows for 12 km pilot length and AWG22 allows for 8 km pilot wire length.

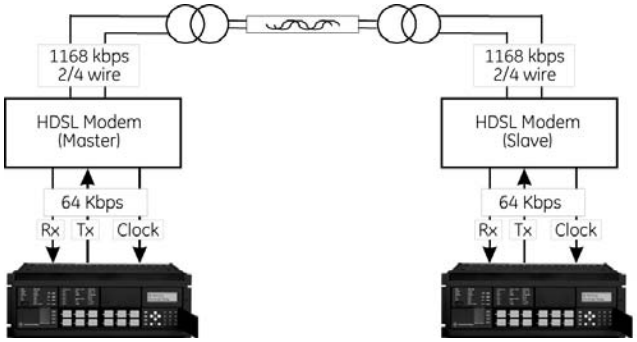

Fig 4.
Configuration of communication link over pilot wire

The HDSL modems are packaged with software for configuration as per specific application. On the DSL side, CRC checks are performed per DSL frame for each channel and direction. The software to count the block-errors of the respective DSL channel and to evaluate its error performance according to ITU-T G.826 standard uses CRC errors. It usually supports two-channel capability, which fits well into redundant channel concept for current differential relaying. This increases reliability of the protection system significantly. For example, for some applications customers used two independent modems via two separate pilot wires routes to increase security and availability of the protection system.

5. Applications Considerations

There are few application considerations have to be taken into account;

a. Channel availability;
Which in its turn is affected by noise presence on the channel. ITU-T G.821 recommends that when a 64 kbit/s channel is available, severely errored seconds should be limited to less than 0.002% of the time, and errored seconds should be limited to less than 0.08% of the time. An errored second is a one second time interval in which there are one or more bit errors, which comes out to be an equivalent Bit Error Ratio (BER) of about 1.5E-5 at 64 kbit/s.

A severely errored second is a one second time interval during which the BER is greater than 1E-3. For example, the 87L function is unavailable when its BER rises above 1E-4 or when the channel is down altogether. We recommend, if not more than 0.06% of overall "in service time" is "unavailable time" to be a reasonable margin to consider Channel as adequate for single-channel application.

For two-channel, two-terminal configuration, both channels must be unavailable for 87L to be unavailable. Assuming independent communications channel operation, the probability that 87L will not be available drops to 0.006%*0.006% percent of the time, or 0.000036%. 87L function has to detect in timely manner that protection is not available to switch to the backup strategy.

b. Noise immunity;
As route of the pilot wire is completely unprotected from electromagnetic interference with other sources. Usually, HDSL modems themselves have CRC-4 or CRC-6 protection against noise, which is not adequate for line current differential protection security. Therefore, 87L has to rely on its own noise detection mechanism and supervising functions.

Good example of protecting communication packet against communications noise is utilizing CRC-32 in the differential relay. The most severe situation as far as false operation is concerned is a high bit error rate, because a 32-bit CRC detects all one, two, and three bit errors in a message, so the necessary condition is an error of four or more bits. In the this worst case scenario of a collection of random bits, the probability of a corrupted message sneaking by the 32-bit CRC check is ½**32, or approximately 2.33E-8%.

According to above indicated recommendation of channel unavailability, this worst-case scenario occurs no more than 0.06% of the time during errored seconds. At 60 Hz, the differential relay, which sends 2 packets per cycle in a two terminal single channel configuration, transmits 9.5E8 packets per year in each direction. The probability of a false operation in a year is equal to the product of the probability of the 32-bit CRC failing to detect a severely errored packet times the fraction of severely errored packets, times the number of packets transmitted in a year. Multiplying 2.33E-10, 0.0006, and 9.5E8 together, we arrive at an upper bound for the prob-ability of a false operation of 0.0133%, or less than one false operation in 7,500 years.

c. Channel monitoring;
This includes; channel delay measurement and compensation, lost packets count and CRC errors count are essential differential relay means to determine

quality of the channel during commissioning and maintenance.

d) Redundancy;

Channel Failures have to be considered as imminent. Most reliable approach would be having 2 separate pair of pilot wire via two separate pairs of HDSL modems. However, in the case if both channels fail, fallback strategy has to be considered. Modern current differential relays have enough backup elements, like distance, overcurrent, directional etc, to provide essential backup protection for such case.

e) Security;

security is a measure of how well the relay avoids responding to conditions that do not warrant true internal fault presence. For the relay, which heavily depends on communication channel integrity that means receiving erroneous data not detected by relay's security means and leading to false operation. Even CRC-32 has finite capability in detecting packet's corruption as indicated above. Therefore, to eliminate even this remote possibility of misoperation, simple current disturbance detectors would be beneficial to use as supervising 87L trip elements. Usually, burst of noise occur during fault due to electromagnetic interference and this is exactly the situation when relays have to operate correctly.

f) Dependability;

Dependability is a measure of how well the relay detects the fault and issues the appropriate command (such as breaker opening). In the context of current differential protectoin, this means either burst of noise will take relay out-of-service for time enough to miss true a fault presence. Atypical scenario is an internal fault with corona leading to a burst of noise, which is gradually decreasing during the fault, and in question is relay response to such conditions.

6. Summary

Current differential relaying can be easily applied over pilot wires. Modern technologies like HDSL modem fa-cilitate such applications. GE relays have been in-service over pilot wire application for several years trouble free. This allows replacing out of date pilot wire relay with modern current differential relay with a minimum invest-ment and labor.

7. References

[1] C. Russell Mason, "The Art & Science of Protective Relaying", GE Publication GER-3738, 1967.

[2] "Application Guide AC Pilot Wire Relaying System SPD and SPA Relays", GE publication GET-6462A

[3] SNC Manufacturing Company HDSL/56kbps Data isolation Interface Part #31042 specification.

[4] GE Publication GEK-112994A, 2005, L90 Line Differential Relay, Instruction Manual.

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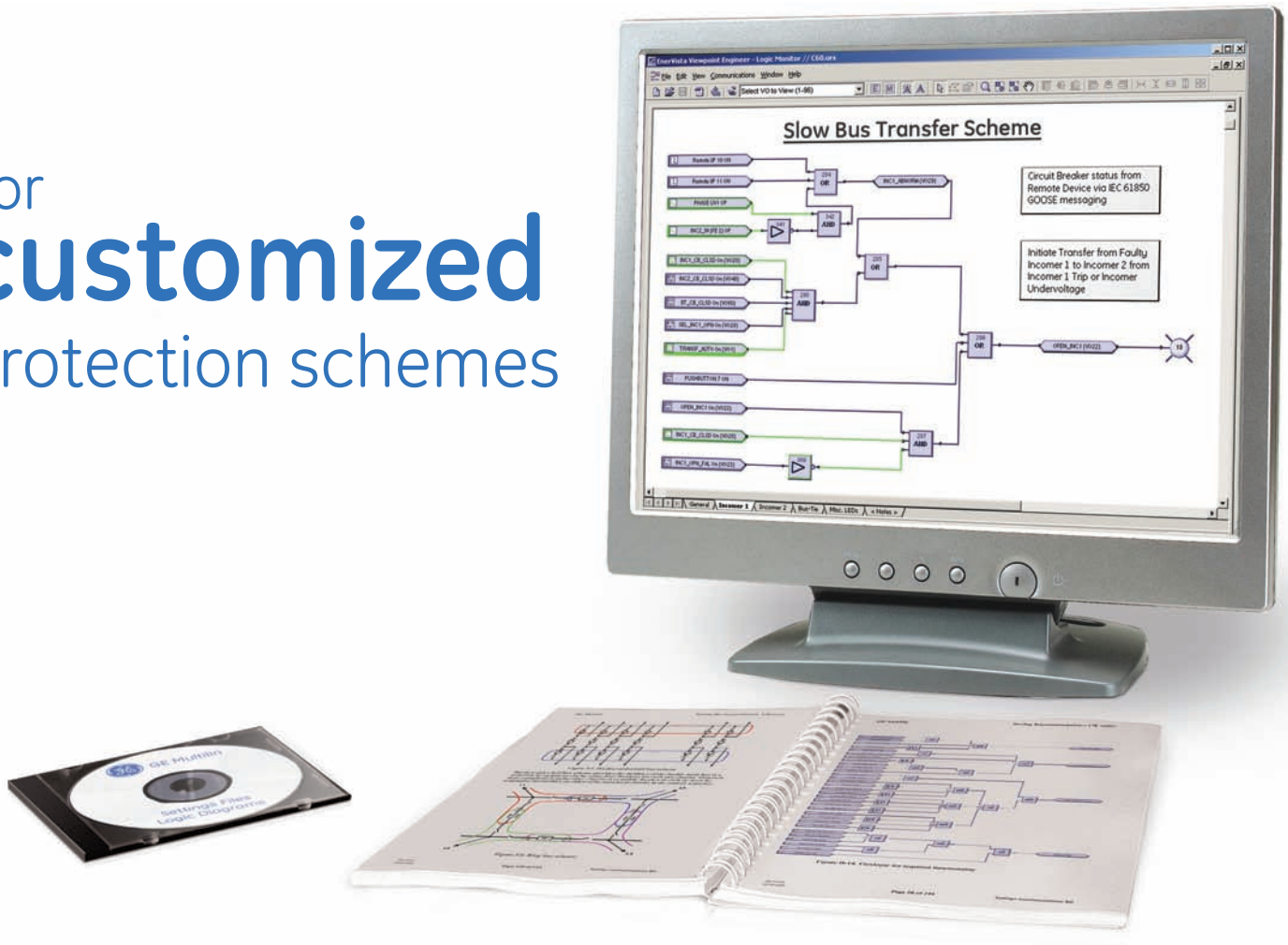

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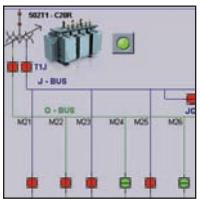

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1. Introduction

As "junction points" at all voltage levels, carrying energy in electric power schemes, power substation buses are critical to scheme topology. Exposure to high-fault currents imposes stringent performance requirements on both bus protection relays and current transformers. Saturation of current transformers (CTs) caused by external problems may jeopardize the security of bus protection due to unbalanced currents in the differential relay.

Improper operation of a bus relay, in turn, considerably changes scheme topology and significantly impacts both power delivery, in the case of a distribution bus, and scheme stability in the case of a transmission-level bus.

Historically, Pacific Gas and Electric Company (PG&E) has standardized on the double-bus single-breaker arrangement for major transmission buses (Figure 1).

The standard protection for these buses has been a high impedance bus differential relay. The single breaker double bus configuration, formerly used, required complex switching of the bus differential CT, dc tripping circuits and breaker failure tripping circuits whenever the bus configuration was changed by operating the bus isolator switches. Operations personnel were often required to execute more than 100 switching steps to reconfigure the bus in order to take one breaker out of service by bypassing and clearing it while maintaining protection of the circuit using a substitute breaker.

Low-impedance microprocessor-based bus protection schemes have provided a better solution to protecting the double-bus single-breaker bus configuration. Such schemes monitor all currents as well as the positions of breakers and isolators, and dynamically adjust their zones of protection for

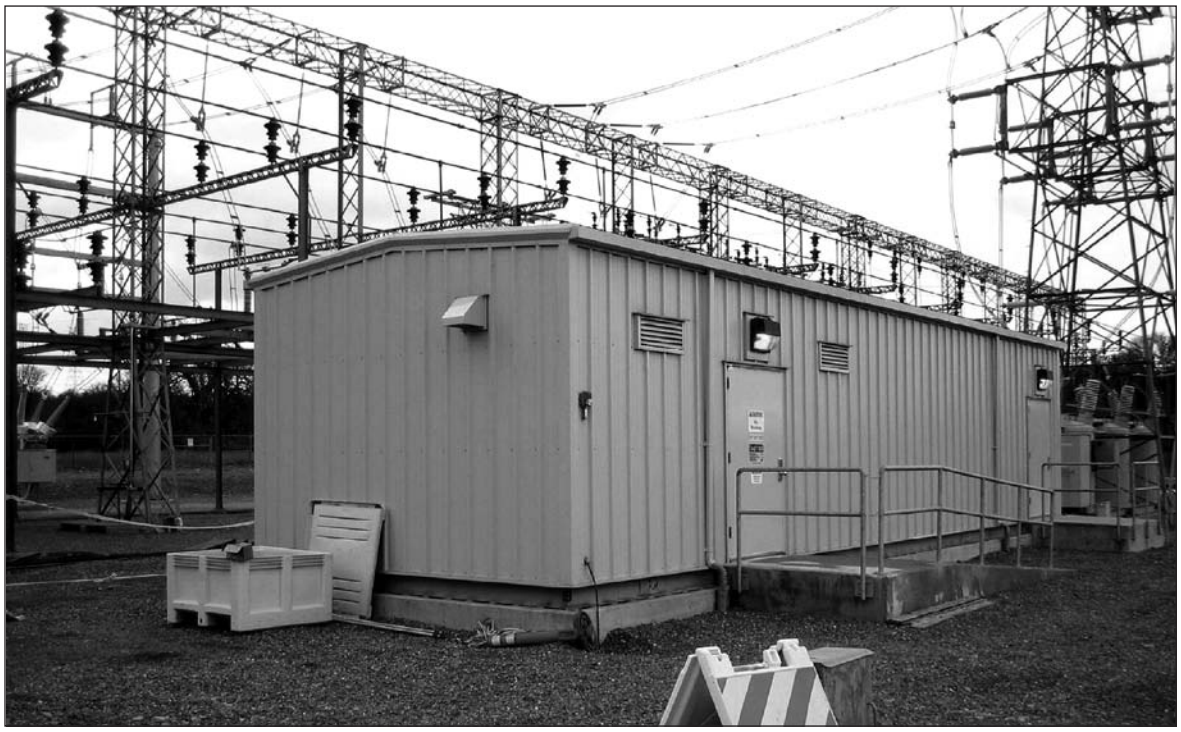


Fig 1.
115 kV single breaker double bus and control building.

Fig 2.
60 kv bus with outdoor relay cabinet and indoor control building

optimum selectivity while the bus is being switched. These schemes do not require operator intervention, which saves time and reduces the risk of an incorrect operation. The schemes can also be installed in outdoor cabinets close to the protected bus, reducing the length of CT wiring to the differential relays (Figure 2).

Other reasons for the increasing penetration of low-impedance microprocessor-based relays are their advanced monitoring functions, integrated breaker failure protection, and cost. This penetration became particularly noticeable after several vendors released affordable phase-segregated low-impedance bus relays around 2002 [1].

Lastly, and most importantly, the installation a low-impedance differential makes it easier to accommodate added generation or expansion of existing buses because it is not necessary to change existing CTs or add slip-on CTs as is sometimes required for high-impedance bus differentials.

The high-impedance bus differential requires that all CTs have the same ratio, preferably no tapped CT windings, and similar excitation characteristics. Traditionally, robust high-impedance schemes may fail to operate correctly if all the CTs are not properly matched. Modern low-impedance solutions show very high immunity to extreme cases of CT saturation; in many such cases, performance is better than that of the high-impedance schemes [2]. The low-impedance microprocessor-based relay is a complex piece of protection equipment to commission. Quite often the scheme consists of many ac current inputs, ac voltage inputs, trip outputs, and several - perhaps hundreds - of status inputs.

This paper reviews some of the basics of bus protection, discusses some unique logic requirements for handling switching and bypassing of breakers on a double-bus single breaker configuration, and focuses on some of the practical aspects of commissioning complex bus schemes.

2. Cost-Efficient Bus Protection Schemes

While monitoring bus configuration is unimportant for many bus arrangements (Figures 3 and 4), for other configurations monitoring bus topology and following it in terms of measuring and tripping zone boundaries, is essential (Figure 5).

Reconfigurable buses, such as is shown in Figure 5, are best protected by low-impedance microprocessor-based bus differential schemes. Such schemes recently became quite affordable and relatively easy to install, with the introduction of a phase-segregated version such as solution [3-4].

From the perspective of the most important area of protection, the bus differential function (algorithm) is naturally phase-segregated, which means that no information is required regarding currents in phases B and C in order to fully protect phase A. The results are as follows [2-4]:

- Completely independent microprocessor-based devices can process the ac signals that belong to phases A, B and C. No data transfer is required between the individual devices of the bus protection scheme.

- Sampling synchronization is not required between the separate microprocessor-based relays that process signals from individual phases.

These facilitate phase-segregated busbar protection. In Figure 6, three separate relays (Intelligent Electronic Devices (IEDs)

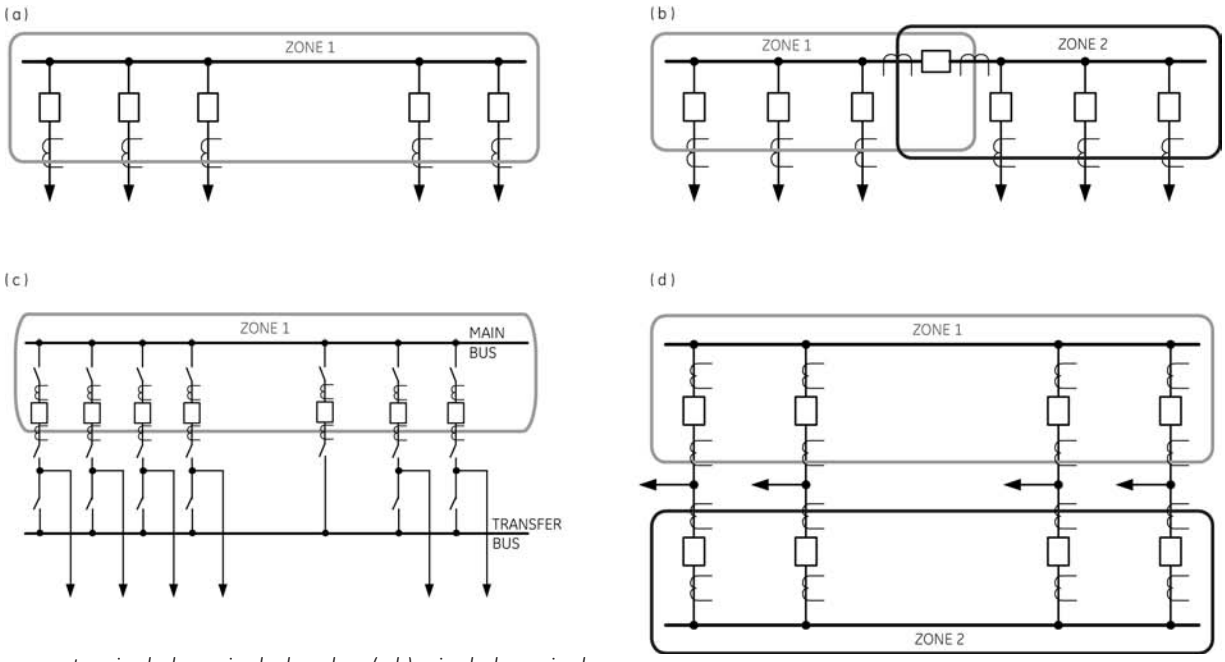


Fig 3.
Bus arrangements: single-bus single breaker (a,b), single-bus single-breaker with a transfer bus (c), double-bus double-breaker (d).

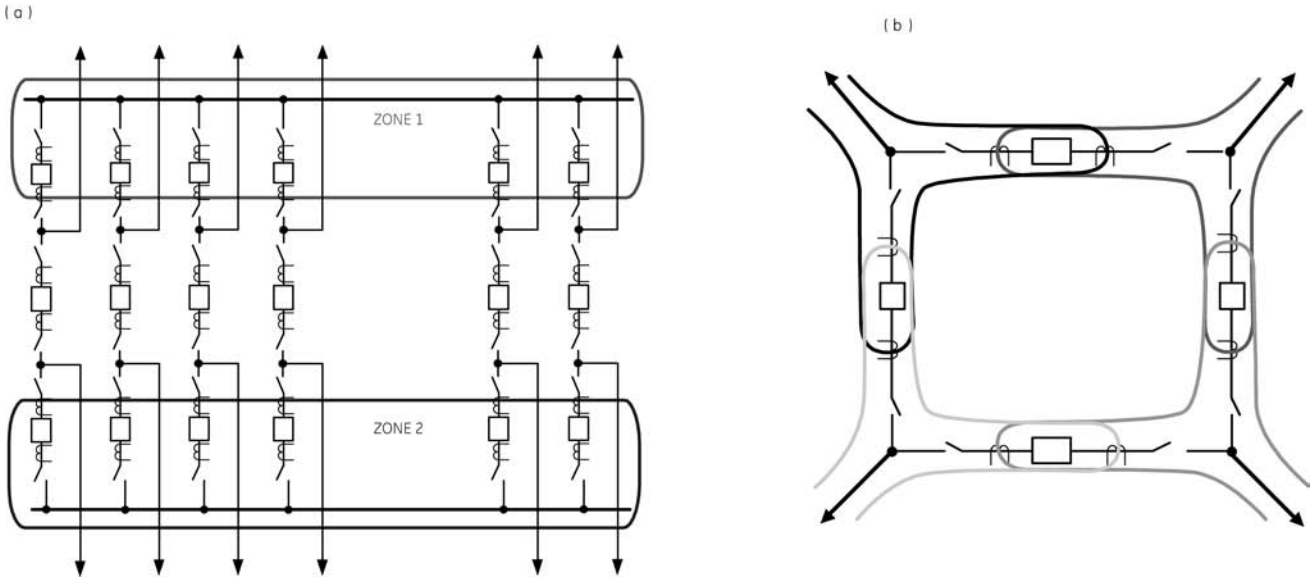


Fig 4.
Bus arrangements: breaker-and-a-half (a) and ring-bus (b).

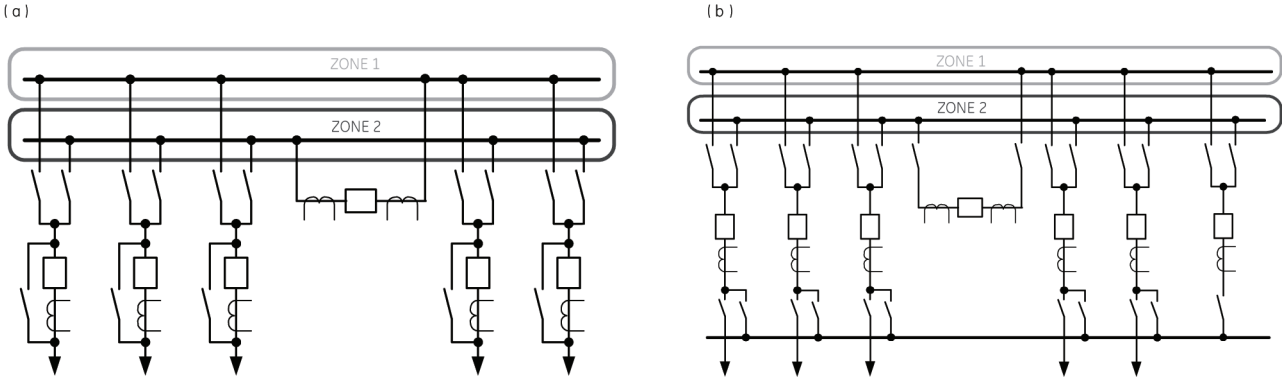


Fig 5.
Bus arrangements: double-bus single-breaker without (a) and with (b) a transfer bus.

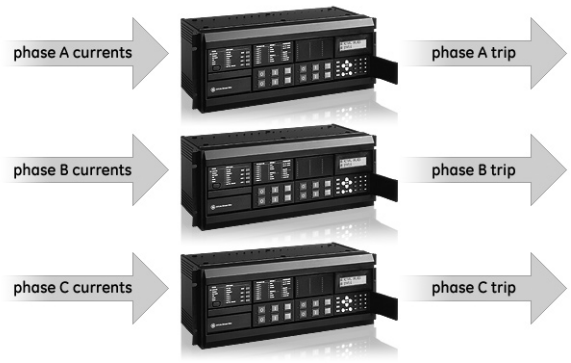


Fig 6.
Idea behind phase-segregated bus protection schemes.

[1]) are used to provide protection for a three-phase busbar. Each phase of each device is fed with its own ac currents and voltages, the signals are processed, and the trip/no-trip decision is made. At least one device operates for any type of fault. For phase-to-phase faults, two relays operate.

Traditional low-impedance bus differential protection schemes monitor all bus currents, derive differential and restraint signals, and apply these signals to a pre-configured operating characteristic for the tripping/restraining action.

Modern relays [1,2] sample their input signals relatively fast 64 samples per cycle, or faster – and are therefore capable of incorporating sophisticated and robust means of dealing with CT saturation while maintaining excellent sensitivity and speed of operation.

3. Switching Procedures in Typical Double-Bus Configurations

Double-busbar configurations in this case study, have 9 or 10 circuits on average, connected via isolator switches to either bus, have a bus coupler connecting the two buses, and use sectionalizing breakers to divide bus sections (Figure 5a). In addition, each feeder circuit breaker is equipped with a by-pass switch. This switch facilitates breaker substitution where the coupler is temporarily used to protect any of the feeder or transformer bank circuits when the original breaker is taken out of service for maintenance. During the breaker substitution, one bus becomes a part of the transmission circuit, with all the other circuits routed to the other bus.

Low-impedance differential protection applied in this case [1] provides continuous monitoring of all isolator switches, and dynamically includes or excludes currents into or from the applied differential zones. Allocation of trip commands to individual breakers follows this dynamic bus image. The same situation applies to trip commands from the breaker fail function where the secondary breakers are selected dynamically for the failed breakers based on the topology of the busbar at the moment. The isolators are switched either manually or automatically. When a circuit needs to be transferred from one bus to the other, the isolator switch connecting the circuit to the target bus is closed, after which the other isolator, connecting with the original bus, is opened, and the transfer is complete.

Isolator positions are indicated by LEDs on the relay faceplate, allowing the operator to validate that the bus differential relay is accurately reading the bus configuration before and after switching.

For a short time, when both isolators are closed during switching, the two buses are connected together via the isolator switches of the transferred circuit. In the case of a fault occurring at this time, the faulted bus cannot be separated from the other bus (no breaker; two isolators connected in series). In addition, the relay cannot identify the faulty bus (Bus #1 or Bus #2) as the CT associated with the transferred circuit measures only the sum of the currents flowing towards each of the paralleled buses without knowing how much current is flowing into each bus. The bus protection relay takes this into account by treating the double-bus as one single bus for the period of time that both isolators are closed for any breaker [3,4].

Breaker substitution is another switching strategy used in this case study. The goal is to isolate a breaker for maintenance while keeping a specific circuit energized. First, with the coupler closed, all other circuits are transferred to one bus (Bus #2 for example) by operating the appropriate isolators. The circuit of interest remains as the only circuit on the other bus (Bus #1). Next, protection of this circuit is provided by enabling substitute relays on the coupler breaker. These relays have CTs on the coupler breaker and are also wired to trip the same breaker. At this time, Bus #1 is part of the transmission circuit from the standpoints of both fault detection (CT) and isolation (CB). The breaker to be maintained is then bypassed by closing the bypass switch, after which disconnects are opened on each side of the breaker in question, to facilitate the work on it.

When the CT on this breaker gets by-passed, its measurements become incorrect (a current divider of an unknown and random division factor). The bus protection zone that uses that current (Bus #1) must therefore be inhibited. Note that differential protection on Bus #1 is not needed at this point, because the bus is already protected as a part of the circuit, by the substitute relays on the coupler breaker. Logic has been developed for the low-impedance bus protection relay, that automatically re-adjusts the bus protection zones of protection when the breaker by-pass switches are operated. During commissioning, bypass switches are operated on selected breakers to verify that the differential scheme is stable, and that the correct zone of protection is blocked. LEDs on the front of the relay indicate when a zone of protection is blocked.

Breaker failure (BF) detection is another important feature supported by the low-impedance bus differential protection and logic. When the breaker is bypassed, and substituted by the coupler, this feature is automatically switched to the coupler. In general, BF trips are always routed dynamically in order to trip the minimum zone required to isolate the failed breaker under any possible bus topology.

4. Scheme Configuration

The bus protection scheme for the double-bus single-breaker configuration in this case study, consists of seven relays mounted on two panels, test switches, terminal blocks, and an Ethernet switch for engineering access and SCADA communications (Figure 7).

Each phase relay is populated with modules supporting binary inputs, output contacts, and ac input cards, in order to match the needs of the application. Three relays are used to provide bus protection zones and BF overcurrent sensing for the three phases of the power scheme. The trip outputs also reside on these relays so that a bus fault can be cleared very fast, without the time delay involved in communicating the trip signal to another IED of the bus scheme. Typically these three relays are configured identically.

The fourth relay is configured to accept inputs from the bus isolator auxiliary contacts, and provide bus replica information for the phase relays. Dynamic association of currents to zones of protection is achieved by monitoring the status of each isolator connecting the circuit to either of the buses (Figure 8). Each isolator auxiliary switch is equipped with a pair of NO and NC contacts wired to the relay and used to provide the "opened", or "closed" isolator position to the relay. Relay logic looks for discrepancies between these contacts, such as when both auxiliary contacts are opened, or both closed, and can be programmed to issue an alarm, to continue to run individual protection zones, to issue a signal inhibiting switching within the bus, or to provide for one overall (hence less-selective) zone of protection. The fifth relay is dedicated to BF timing and tripping.

The sixth relay is populated with only latching output contacts, which provide the physical isolation of the circuit breaker tripping circuits, replacing traditional cut-out/in switches. Output tripping contacts from the phase relays are wired in series with these latching contacts. Latching contacts are controlled from the seventh relay.

The seventh relay is used for remote control of the scheme, using 12 large programmable faceplate pushbuttons, and for SCADA interface. Bus Differential Tripping, Zone 1 Protection, Zone 2 Protection and Automatic Reclosing can be controlled from this relay.

All relays are connected via dedicated redundant rings of fiber-optic cable and exchange hundreds of digital signals to distribute bus status, logic, or indications (Figure 9). Note that this communication is isolated from the rest of the substation network. It is based on optimized protocol and dedicated hardware, and is not based on Ethernet. The Ethernet connection is for Engineering and SCADA access only.

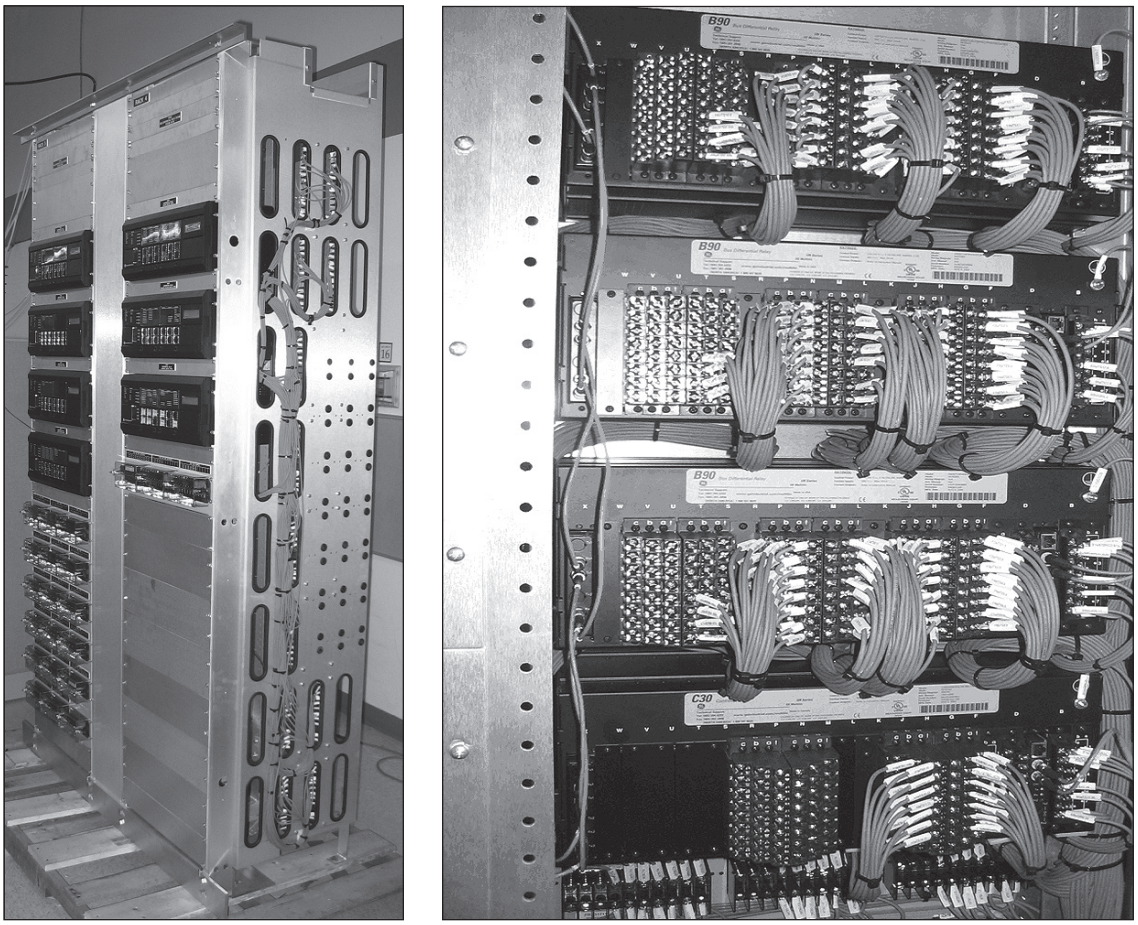


Fig 7.
Multi-IED phase-segregated bus scheme: allocation of functions and physical arrangement.

5. Commissioning Tests

Commissioning of bus protection schemes for such reconfigurable buses, requires good knowledge of the applied bus relays: inputs, outputs, protection, logic, indications, interfaces, and bus switching procedures, used by a given utility. Another very important aspect when commissioning, is the actual design and application of sufficient tests to prove all scheme components and logic.

5.1. Logic testing

A RTDS digital simulator was used for proof-of-concept testing of the unique scheme logic that was developed for the double-bus single-breaker bus protection scheme. Several scenarios were modeled to simulate bus switching under load conditions and to check for correct operation of the scheme under internal and external fault, and saturated CT, conditions.

5.2. Importance of testing auxiliary contacts of isolators

Proper testing and tuning of the isolator's auxiliary contacts is an important aspect of configuring and testing such bus protection schemes. Whether motorized or manual, isolators usually take a few seconds to move from one position to another. The same mechanism that moves the isolator main contacts changes the auxiliary contacts, but at slightly different times during the movement of the isolator main contacts

For example, to assure smooth insertion of the feeder circuit current into the bus differential zone, the auxiliary contacts are adjusted to read status "closed" at 75-80% of the isolator's travel distance, when the isolator is moved from open to closed. When the isolator is moved from closed to open, the auxiliary contacts are adjusted to change their state and read "open" at 35% of the travel distance, right after the main isolator contacts separate. The bus differential relay scheme is set to detect any auxiliary NO/NC contact pair discrepancy, issue an alarm, and optionally block bus switching, until the problem is fixed.

During isolator transitions, security of bus protection is ensured by the application of the check zone or undervoltage trip supervision, or both. However, it is necessary to ensure that the NO/NC auxiliary contacts perform reasonably well and do not generate unnecessary discrepancy alarms.

5.3. Polarity check of current transformers

One of the most important tests on the installed scheme is the CT's polarity check, as the chances of making wiring mistakes are proportional to the number of connections made.

First, the CT ratio and current contribution are checked for each bus circuit breaker by forcing secondary current from each circuit breaker to the respective relay inputs in order to assure a complete current circuit.

Next, with all tripping outputs disabled, the normal scheme load currents are allowed to flow through the bus differential scheme. The load currents are verified with a simple crosscheck of magnitudes and angles of currents as measured by the bus relay, and as measured by meters/relays in the individual circuits. A single bus potential is used as a common reference for the bus relay and feeder relays. In some cases the loading on one feeder circuit may be below the relay's minimum measurement threshold, making it impossible to validate the proper CT phasing of that circuit. This can usually be resolved by switching the power scheme to increase loading on that feeder circuit.

Lastly, the differential relay's metering function is used to check that no differential current is seen for each zone of the bus protection scheme, and that the restraint quantities are as expected. Even though absence of the differential current is a good indication of correct polarity, this check alone is not enough. It could happen that all the currents presently included in the zone have inverted polarities, and are therefore balanced for this particular topology, but would manifest problems when the zone boundary gets dynamically changed as the bus switches its circuits.

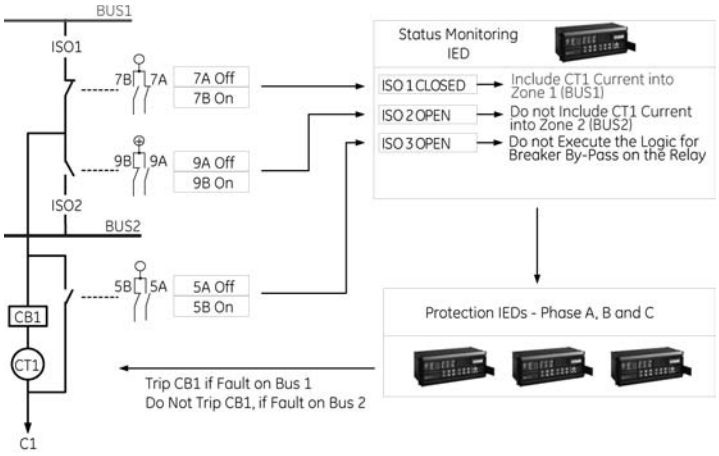


Fig 8.
Implementation of the dynamic bus replica.

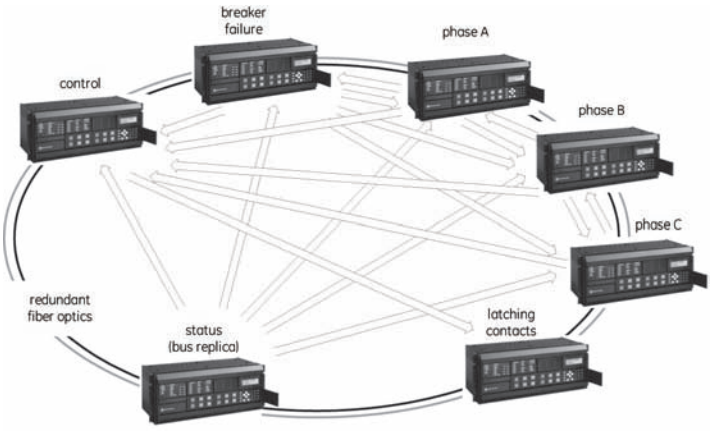


Fig 9.
Redundant Fiber Ring

5.4. Check of the transfer / paralleling logic

Normally each circuit is connected to only one of the two buses, and the scheme applies separate zones of protection for each bus. During the short period when transferring a circuit, the two buses cannot be protected individually. This particular application is developed to expand the two zones to cover the entire bus (Figure 10). For example, ISO1 and ISO2 closed simultaneously trigger the BUS 1 AND 2 PARALLELED condition. This in turn acts to include all circuit currents into both zones of protection. With the logic identical for all circuits but the coupler, all currents become part of zones 1 and 2 making the two zones identical. The coupler, in turn, is removed from both zones under the BUS 1 AND 2 PARALLELED condition (internal circulating current that must not be measured).

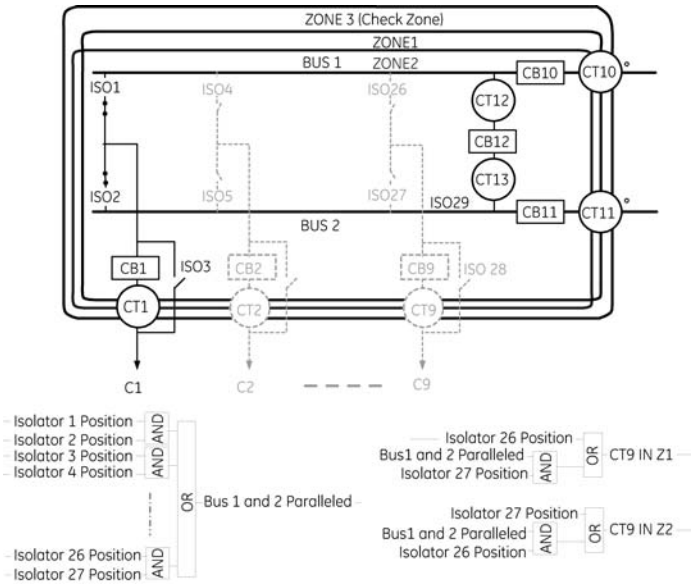


Fig 10.
Logic covering the case of paralleled buses when transferring a circuit.

The applied logic must be exercised during commissioning by transferring each circuit breaker from the preferred bus to the alternate bus and back again, thus checking both the operation of the scheme under load and the proper operation of the isolator auxiliary contacts.

5.5. Breaker by-pass and substitution

Figure 11 shows the breaker substitution case. Circuit C1 is transferred to the coupler (CT12, CB12). Its original breaker is bypassed by closing ISO 2. At this point zone 2 must be stopped because the CT12 and CT1 currents will not balance (CT1 is bypassed and measures a fraction of the current in the C1 circuit). This portion of the logic is checked by forcing the breaker substitution condition and examining the bus zone boundaries. These zone boundaries can be easily checked by reading the internal relay flags via PC software, or via LED indication on the relay faceplate [1]. During commissioning, one circuit breaker is set up to be bypassed on each bus in order to prove proper operation of the bypass switch auxiliary contacts and the relay logic.

6. Trip Tests and Verification of Voltage Supervision

Trip checks are performed on each zone of the bus differential by simulating an internal fault either by injecting test currents or by shorting out currents from the circuit with the greatest load and verifying that the proper circuit breakers are tripped. Coordination with voltage supervision is critical to making this test a success. At the same time as the fault is simulated, the bus voltage to the relay must be momentarily reduced below the voltage supervision pickup in order to get a trip output.

Individual zones for the two buses adjust constantly to the changing bus topology. For security, the check zone and an undervoltage condition “supervise” the trip signals originating at the bus protection zones. There are two reasons for this:

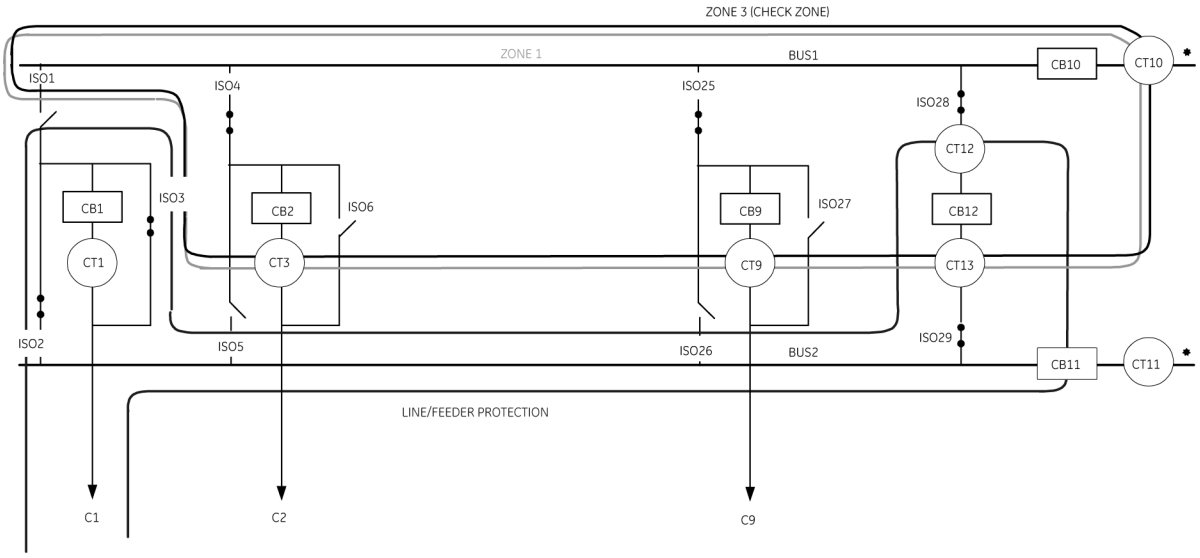


Fig 11.
Protection zones under breaker substitution.

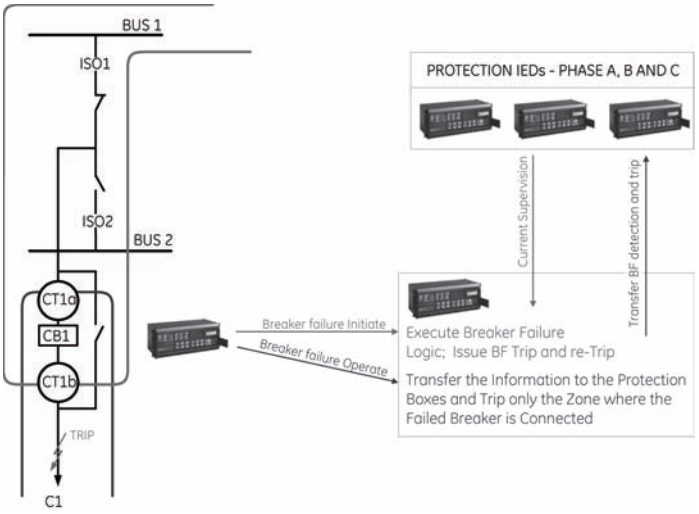


Fig 12.
Breaker Failure protection.

First, there are conditions in the logic that re-assign currents between the two zones of bus protection during switching. This is a necessary consequence of the response time of auxiliary contacts during switching, and the lack of "advanced" signaling by certain switching operations. The voltage supervision prevents false operation of the bus differential during these transitions.

Second, a CT problem condition may occur resulting in a wrong current reading if there is a problem in the main CT wiring, test switches or the input circuitry of the relay. In such a case, the voltage supervision blocks tripping and the relay can be set to alarm only, or block tripping of the affected zone.

The check-zone includes all the currents on the outer boundary of the entire bus. These currents are assigned permanently to say Zone 3. Zone 3 picks up conditions for any fault within the bus, and can release Zones 1 and 2 for operation. Zones 1 and 2 are responsible for selectivity and security. Zone 3 should have CT saturation detection or similar features disabled, as there may be a circulating current between input currents to the check zone. Circulating currents may fool features aimed at detecting CT saturation problem, and may thus inhibit operation during internal faults.

Undervoltage supervision uses bus voltage for security. Note that phase A protection is supervised from either AG, AB or CA voltage. Sometimes two sets of voltages must be wired to the relay and proper voltage must be selected for each of the two buses, to cover the case where the two buses are entirely isolated.

The tests described above are performed during commissioning to make sure that spurious pickup of the tripping zones is stopped by the check-zone and/or overvoltage condition (security). At the same time, both the check-zone and the undervoltage must be checked for dependability.

7. Breaker Failure Considerations

The microprocessor bus differential has logic built in to provide breaker failure protection with fault detectors and timers that can be set independently for each circuit breaker. In this particular case study an external BF function is used. With reference to Figure 12, the BF trip signal is issued by the line/feeder relay and is input to the bus protection scheme. The bus relay selects breakers that need to be tripped to isolate the problem, based on the bus topology at that moment.

A second BF function, integrated with the bus relay, is used for bus faults. The BF is initiated from the 87B function and sent to the line/feeder BF relays in order to force the re-trip and provide for redundancy of the BF function.

Commissioning tests include simulation of breaker failure for each circuit by closing the corresponding BFI and External BF contact inputs to the bus differential scheme, and verifying that the trip contacts trip only the breakers connected to the same bus as that of the failed breaker.

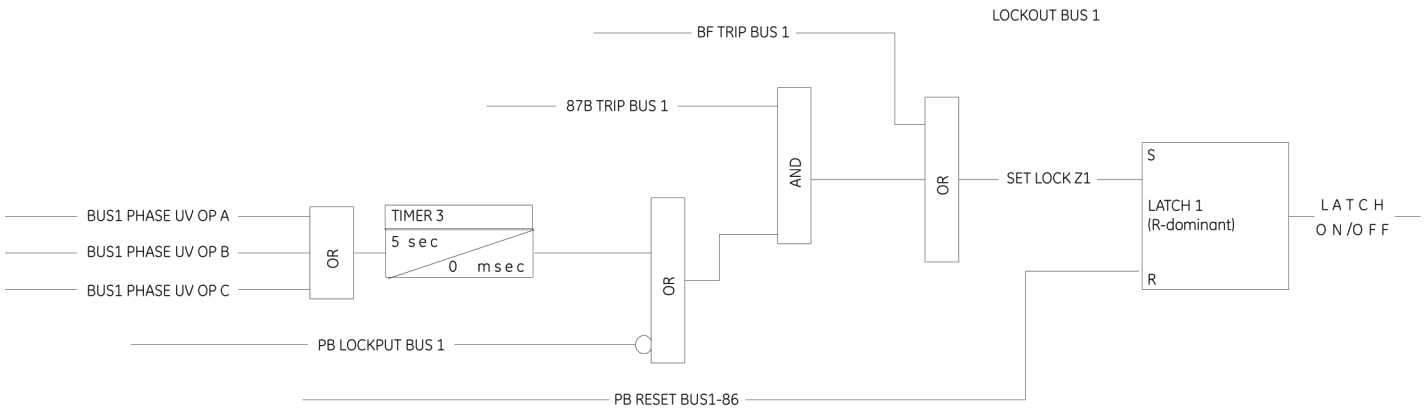


Fig 13.
Lockout logic

8. Lockout and Reclose Block Functionality

The scheme incorporates internal lockout logic to block auto reclose of the bus following a permanent bus fault or breaker failure operation. A combination of a software feature (non-volatile latch) and NC output contacts is used to implement this feature. The logic includes a feature to enable/disable auto reclose by one breaker in order to test the bus following a bus fault. If this test is unsuccessful, further auto reclose actions are blocked by the lockout relay.

Figure 13 presents the applied logic. Based on this solution, the lockout will not be initiated when the first bus fault occurs unless the test is eliminated. If a second fault occurs after the scheme has detected undervoltage for at least 5 seconds, the lockout will be set. This feature can be enabled or disabled by the operator and is tested during commissioning by simulating an auto reclose operation.

9. Pushbuttons

This microprocessor relay design uses pushbuttons in place of conventional control switches, to enable and disable (a) bus protection, (b) breaker failure protection on each breaker and (c) auto reclose following a bus fault. This design simplifies both wiring and overall design of the scheme and allows the substation operator to control the scheme from one location, such as a control building, if the protective relays are installed in a remote location.

10. Self-Monitoring

Microprocessor relays have a great advantage over electromechanical relays because they are self-monitoring. Each microprocessor relay in the bus differential scheme has its typical self-monitoring features and provides an alarm for critical failures such as failure of the processor or power supply. In addition, alarms are provided for communication failures between relays, for disagreement between the auxiliary contacts on the isolator and bypass switches, and for failure of a CT. This last one is very important since it can identify a failed CT before the scheme is called on to operate for a bus fault. A high impedance relay scheme can fail to operate due to a CT failure and this scheme has no way of detecting this type of failure. Each of these alarm conditions is tested as part of commissioning.

11. Operator Training

Operator training was provided as part of the final testing and commissioning of the microprocessor bus differential relay scheme, because of the significant differences between it and the previous high-impedance differential design. One major difference is that the new scheme has essentially no relay switches for the operator to switch while switching is being performed on the bus isolators. Previously, the operator was required to manually operate one control switch to connect the two bus differentials prior to switching the bus, and to manually operate another switch for each breaker being switched to match the position of the isolators on the bus. In addition, the operator had to manually take the scheme out of service and place it in test mode after switching, in order to confirm that the differential was balanced prior to disabling the relay. Operators also need to understand how to interpret the LED status and relay alarm indicators, and how to operate the pushbuttons to enable tripping and automatic reclosing.

12. Conclusions

Modern bus protection solutions may be developed as multi-IED phase-segregated schemes. They are built on standard software and hardware platforms, resulting in significantly lower costs compared with first-generation microprocessor-based bus relays, and providing a high degree of user familiarity, initial product maturity, and flexibility of application [1]. Application of these relays to reconfigurable and relatively complex buses can be done in user-programmable logic allowing accommodation of various protection philosophies, greater flexibility, and "future proofing." Modern relays support remote access, enhanced faceplate indicators, metering, oscillographic recording and other features that facilitate testing and commissioning as well as provide a record of scheme faults. This case study shows that a complex bus application, pre-tested at the factory (Figure 5), can be commissioned within a 2 to 3-day time period.

Built in logic allows operators to perform routine switching of the bus without the need for manually operating relay control switches, thus saving time and eliminating the possibility of incorrect operation.

13. References

[1] B90 Bus Differential Relay (Instruction Manual), GE Publication GEK-106387, 2003 (http://www.multilin.com).

[2] Kasztenny B., Brunello G., Sevov L., "Digital Low-Impedance Busbar Protection with Reduced Requirements for the CTs", Proceedings of the 2001 IEEE T&D Conference and Exposition, Atlanta, GA, October 28 – November 2, 2001, paper reference 0-7803-7287-5/01.

[3] Kasztenny B., Cardenas J., "Phase-Segregated Digital Busbar Protection Solutions", Proceedings of the 57th Annual Conference for Protective Relay Engineers, College Station, TX, March 30 – April 1, 2004. Also Proceedings of the 58th Annual Georgia Tech Protective Relaying, Atlanta, GA, April 28-30, 2004.

[4] Kasztenny B., Brunello G., "Modern Cost – Efficient Digital Busbar Protection Solutions", Proceedings of the 28th Annual Western Protective Relay Conference, Spokane, WA, October 21-24, 2002. Also presented at IV Simposio "Iberoamericano Sobre Proteccion de Sistemas Electricos de Potencia", Monterey, Mexico, November 17-20, 2002; 2003 T&D Conference, Adelaide, Australia, November 16-19, 2003.

Engineering Quick Tip:

Ensure Relay Settings Match Those Programmed In The Settings File

Incorrectly programmed protection devices create a serious security risk to the stability and reliability of your protection system. Periodically confirming that the device settings are programmed the same as the original settings issued by the protection engineer ensures that the relay's operation will match the system specifications.

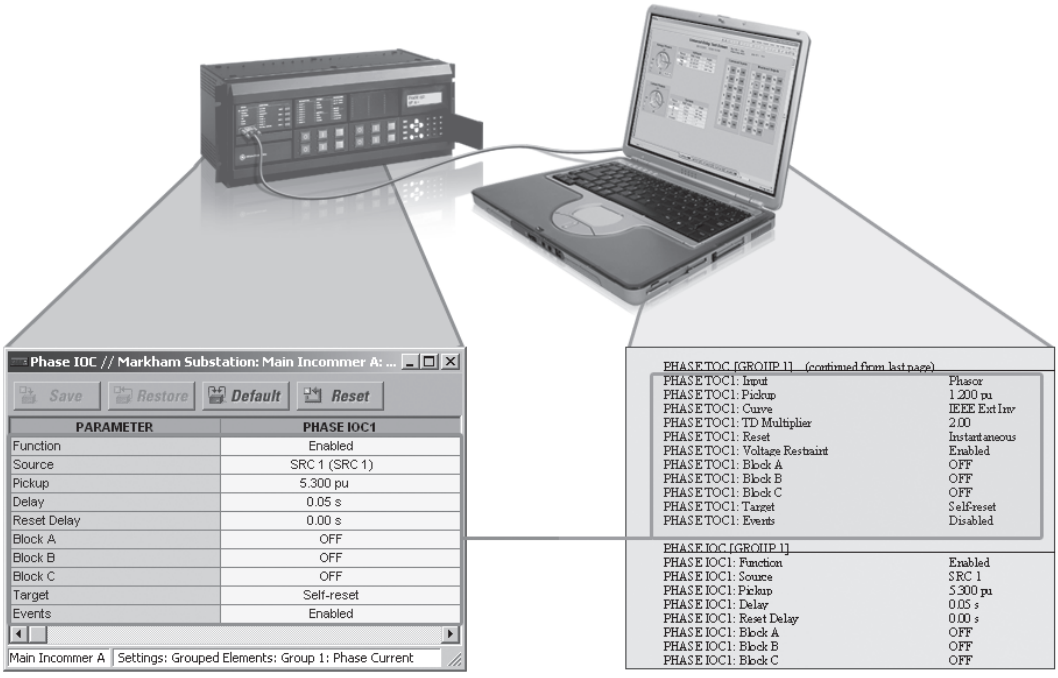


Fig.1. *Identify the differences between the Setting File and the Relay's configuration*

GE Multilin's *Enervista UR Setup* program allows you to compare the settings that are programmed in a relay with a file stored on your computer. This can be done while the relay is online and protecting the system, requiring no down time at all. When completed, a report will be generated outlining any settings in the relay which do not match the settings programmed in the file.

The following is an example of how to compare the relay settings to a saved file.

1. Select the *Quick Connect* button and enter the information required to establish communications with your relay.

2. Right click in the *Offline Window* and select *Add Existing Settings File*. Open the saved file associated with your relay.

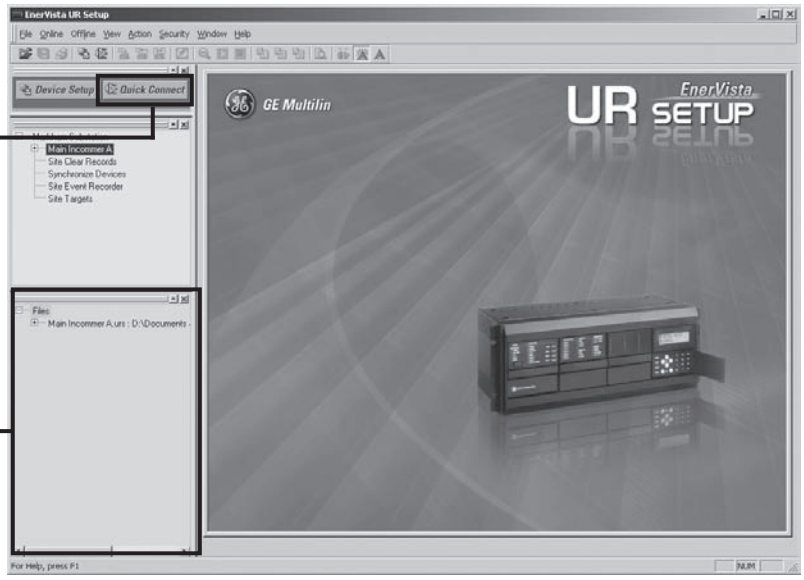


Fig.2.

3. Right click on the Quick Connect Device that was just added and select *Compare with Setting File* from the pop-up window.

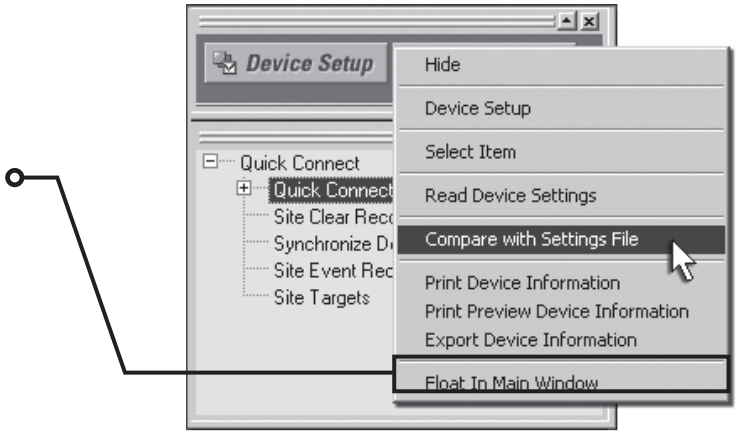


Fig.3.

4. A window will open asking you to select which file you wish to use for the comparison. Any files that have been opened in the *UR Setup* program's Offline Window will appear here.

Select your file, and then OK.

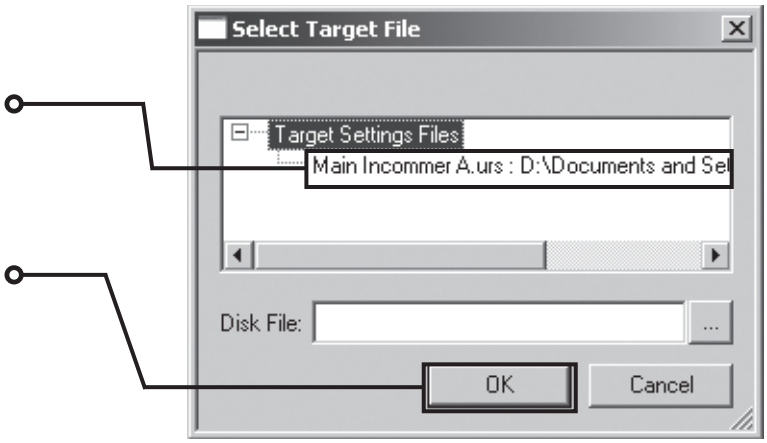


Fig.4.

If the relay's programming matches all settings in the saved file, a message will be displayed indicating that no differences were found.

If the relay's programming does not match the settings in the saved file, a message will be displayed indicating the number of settings that are not the same.

Selecting OK will generate a report of all mismatched settings.

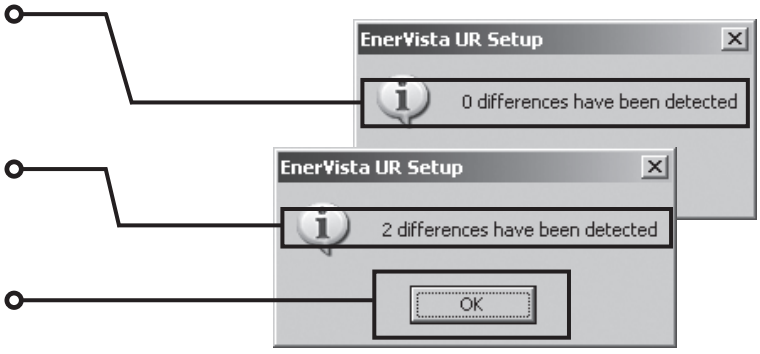
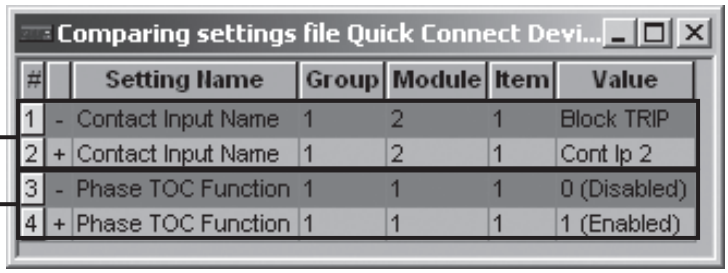


Fig.5.

Setting Difference Example

Example 1: Relay settings have Contact Input 2 named as *Block TRIP*. The settings file has the contact named *Cont Ip 2*.

Example 2: Relay settings has the Phase Time Overcurrent (TOC) *Disabled*. The settings file has the TOC function *Enabled*.



#		Setting Name	Group	Module	Item	Value
1	-	Contact Input Name	1	2	1	Block TRIP
2	+	Contact Input Name	1	2	1	Cont Ip 2
3	-	Phase TOC Function	1	1	1	0 (Disabled)
4	+	Phase TOC Function	1	1	1	1 (Enabled)

Fig.6.

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Engineering Quick Tip:
Reduce the Time Required to Retrieve Fault Information from your Devices

When a system fault occurs, the first step in troubleshooting is to retrieve all of the available critical fault information from the devices protecting the system. Depending on the location of the protection relays, and the number of devices that need to be accessed, simply retrieving the required troubleshooting information can cause additional and expensive down time.

The Viewpoint Monitoring software package provides automatic retrieval of Event Records and Oscillography files from all connected GE Multilin devices. Automatically retrieving the critical fault data means that as soon as the fault occurs, you will have all of the information needed for troubleshooting at your fingertips.

VIEWPOINT *monitoring*

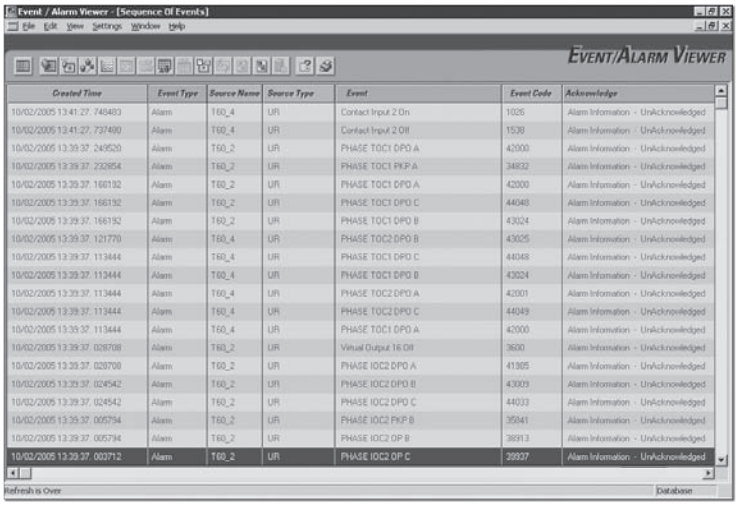

Fig.1. System Event Record

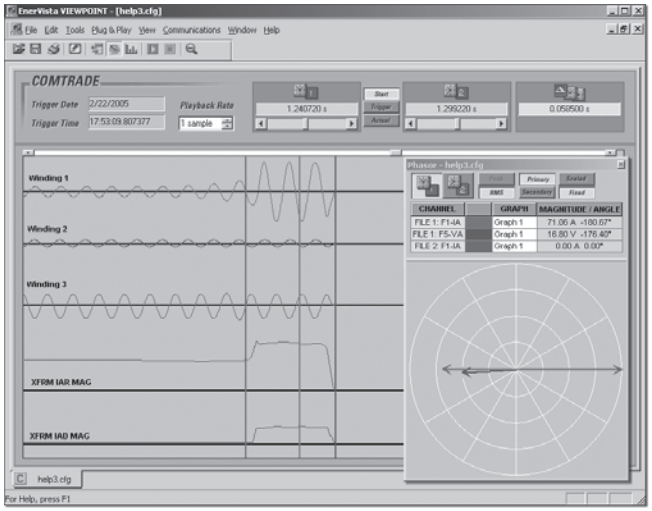

Fig.2. Automatically Retrieved Oscillography File

The following steps will outline how to configure Viewpoint Monitoring to automatically download Events & Waveforms.

1. Click on *Device Setup* from the *Viewpoint Monitoring* main page to launch the Setup window.

2. After entering all of the required communications settings, make sure that the *Waveform* and *Events* boxes have been checked.

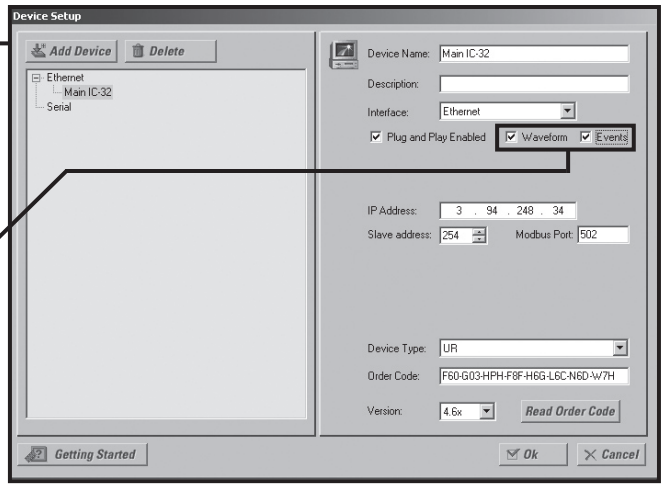

Fig.3.

As soon as the device configuration is complete, Viewpoint Monitoring will connect to the relay and download all event and waveform files. As new event and waveform files are generated by the relay, they will be automatically downloaded to Viewpoint Monitoring.

3. To view the saved Events, select the *Events* option from *Viewpoint Monitoring*. The *Event/ Alarm Viewer* window will open, allowing you to view all of the events that have been recorded from all devices connected to the *Viewpoint Monitoring* software.

This information can be sorted based on a number of criteria, including the device it originated from, when the event occurred, as well as the cause of the event.

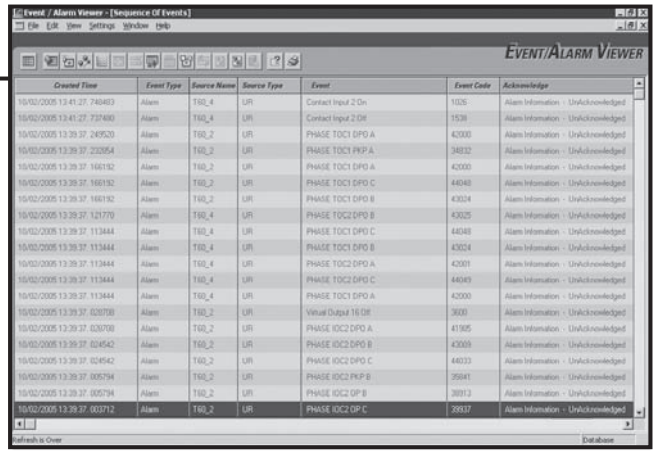

Fig.4.

4. To view the saved Waveform files, select *Waveforms* from the Viewpoint Monitoring main page. Select *View* from the *Automated Retrieval* window.

When a file is selected, the comtrade viewer will open, displaying the selected waveforms.

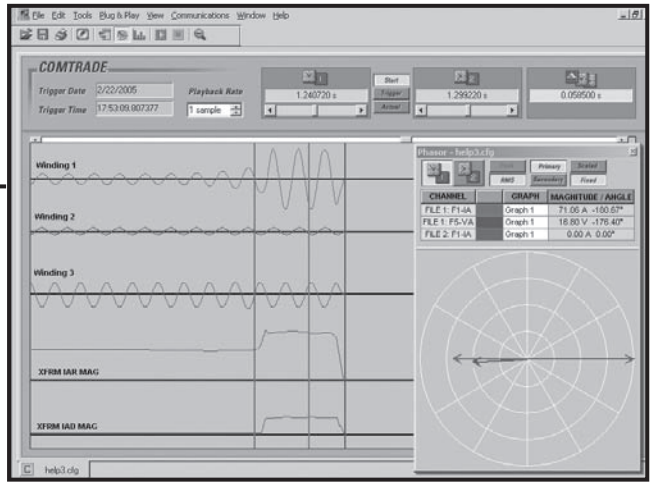

Fig.5.

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Engineering Quick Tip:
Identify Wiring and Logic Status to Simplify System Commissioning

Commissioning a protection system requires confirming both the wiring of the relay inputs and interlocks, as well as the programmed logic of the protection devices. When devices do not operate as expected during commissioning tests, reviewing physical wiring, logic states, programming, and output states can prove to be a very time consuming task.

The ***Logic Monitor*** function of GE Multilin's ***Viewpoint Engineer*** provides graphical real time monitoring of programmed logic, including relay inputs, protection element flags, and logic outputs. A single screen will clearly define all of the logic input states, allowing you to quickly identify which inputs are causing the relay not to operate as expected.

VIEWPOINT *engineer*

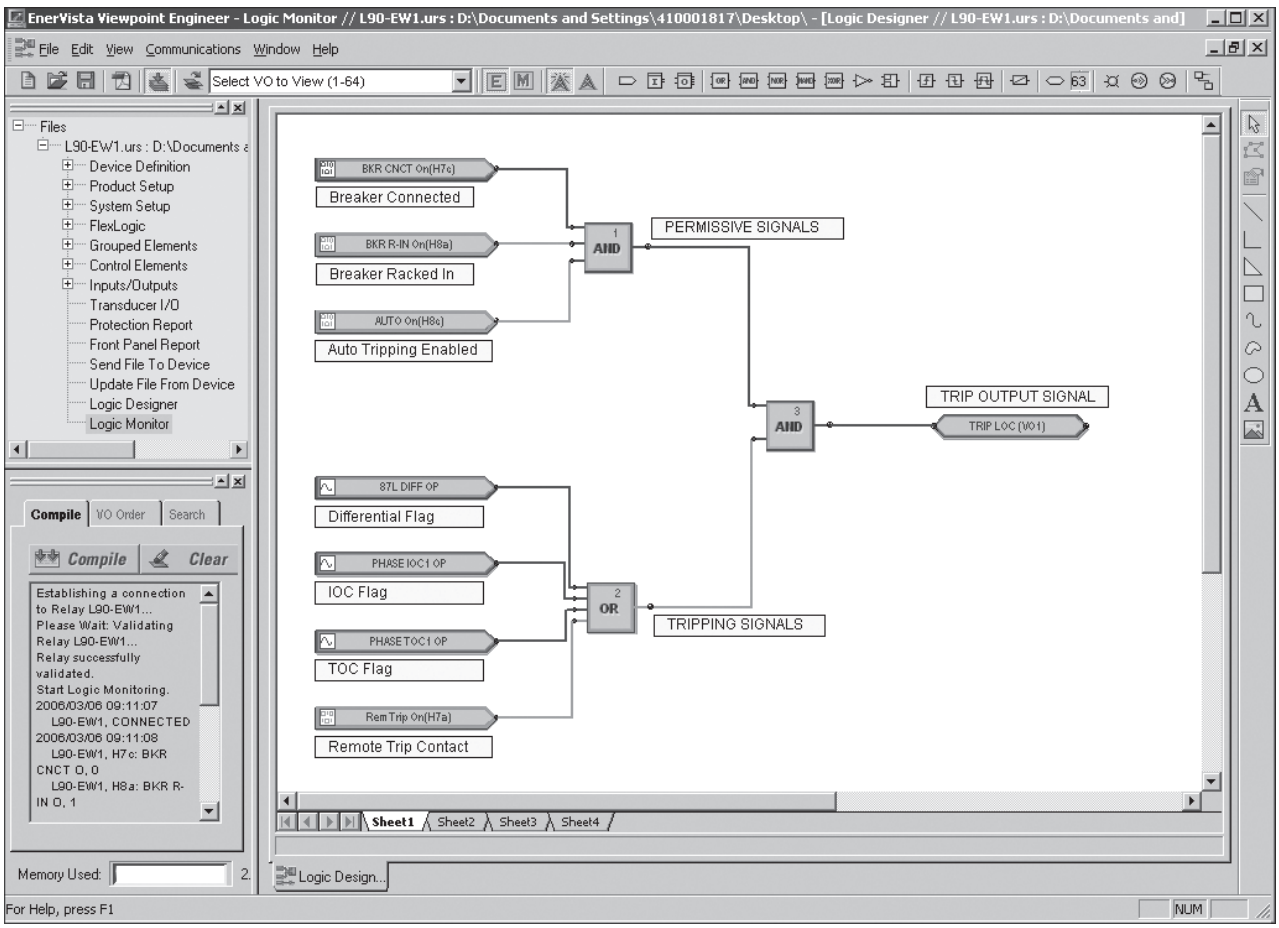

Fig.1. Note: The TRIP output will not operate since the Breaker Connected input is not active

Use the following steps to activate your Real Time Logic Monitor:

1. Select the *Logic Monitor* option from *Viewpoint Engineer* Toolkit.

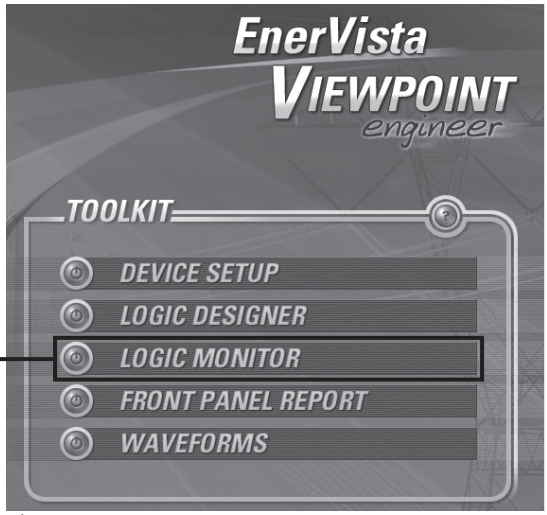

Fig.2.

2. Select the Open File icon and select the setting file of the relay you wish to monitor. This must be a saved copy of the setting file that is programmed into the relay you will be communicating to.

Fig.3.

Viewpoint Engineer will now establish communications with the relay and compare the programmed logic with the logic in your setting file. If the logic matches, the program will retrieve and display the states of all logical inputs and outputs.

The Setting File Tree allows you to choose a UR's Setting File and begin monitoring the logic status of a particular device.

The Active window graphically displays the real time status of the programmed logic inside the relay. Active inputs or logical outputs are easily identifiable by their green lines.

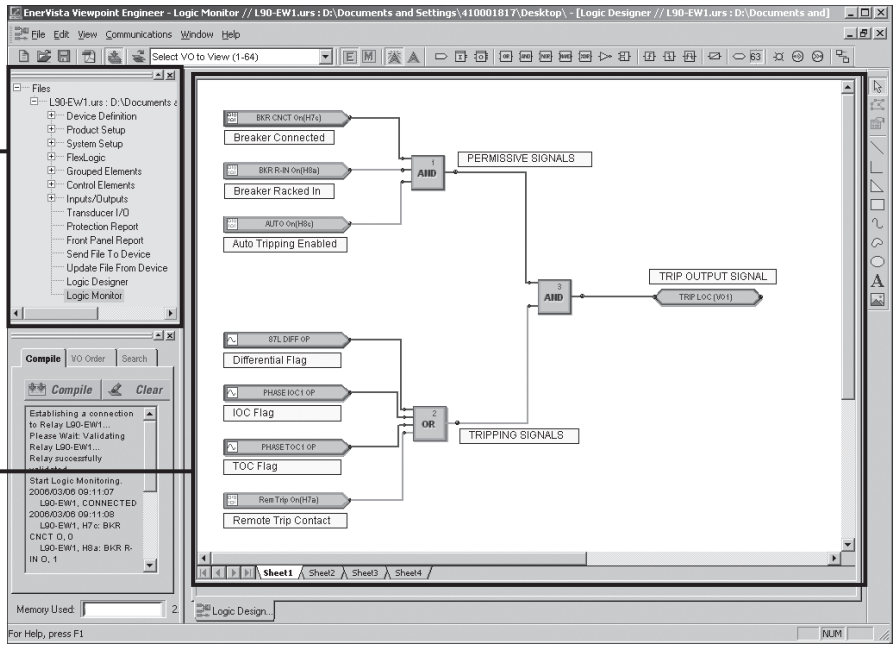

Fig.4.

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Engineering Quick Tip:

Enhance System Security while Providing Traceability to Device Settings

In today's utility and industrial applications, system security has become one of the greatest challenges. Part of this challenge is ensuring that the settings programmed into system devices are not changed, either by accident, or intentionally. Any change in the protection configuration can jeopardize system reliability and functionality.

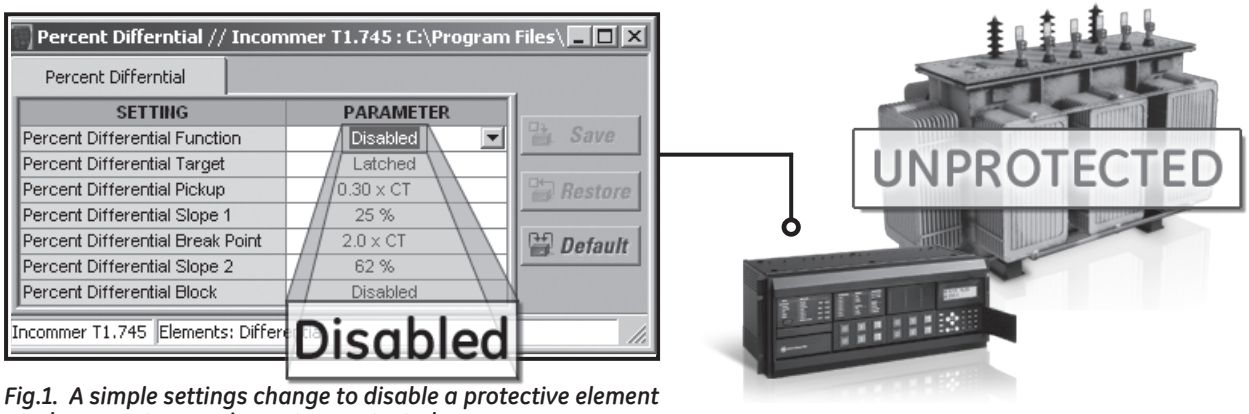
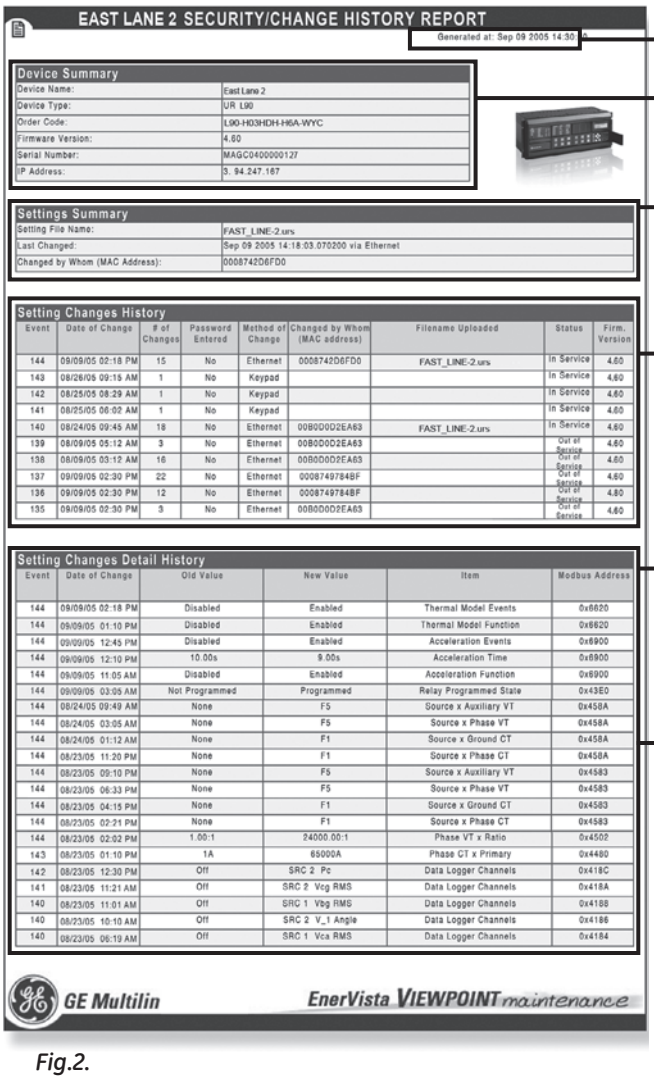


Fig.1. A simple settings change to disable a protective element can leave system equipment unprotected.

The *Viewpoint Maintenance* software package provides an easy to use Security Audit Trail. This report will outline when a device's settings were changed, who made the changes, as well as the specific settings and values which have been altered.



VIEWPOINT *maintenance*

Date and Time that the Security Report was generated

Description of the GE Multilin Relay

- Equipment Name
- Relay Model and Firmware version
- Relay Serial Number

Summary of the last time the configuration was changed

- Name of setting file
- Who loaded the file
- When the file was loaded

History of the last 10 occurrences the configuration was changed

- Date and time of the configuration change
- Number of setting changes at this time
- Method used to change the relay settings
- MAC address of the computer sending settings
- Name of the setting file sent to the relay
- The relay status after the setting changes

Detailed description of all changes made to the relays configuration

- Date and time of the configuration change
- Description of the setting that was changed
- Setting value before change was made
- Setting value after change was made

Convenient File Format

- On-line and off-line copies
- Easily zip these reports with other pertinent Files such as setting files and fault reports to share with engineers

Fig.2.

To create your Security Audit Report, simply perform the following steps:

1. Open *Viewpoint Maintenance* and select *Security Report*.

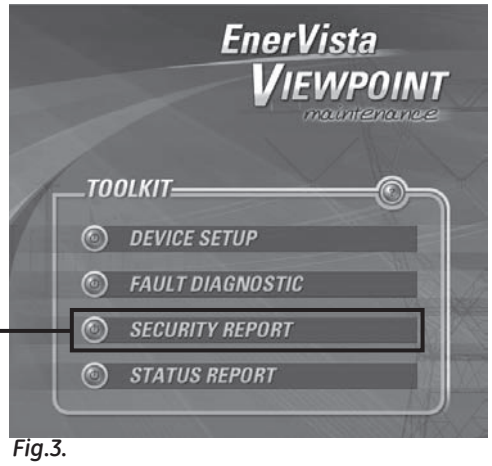


Fig.3.

2. Select the device you wish to create the Security Report for.

Note:
If the device is not seen in the drop down menu, it will need to be configured under the Device Setup menu of Viewpoint Maintenance.

3. Select the *Check IED for latest Security Report* button to perform the settings verification.

Note:
When performing security reports for relays that do not store the Security Audit Trail internally a security report will not be generated the first time the program is run. The settings will be saved from the relay, and these settings will be used as the baseline for any future reports.

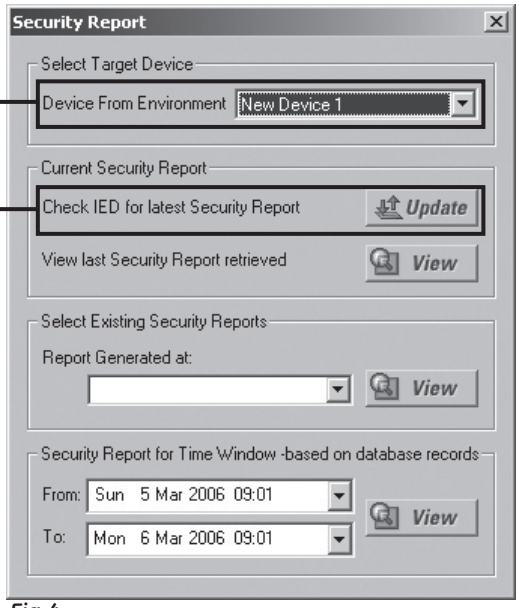


Fig.4.

4. To view Security Reports that were previously generated, select the date that the report was created from the Select Existing Security Reports drop down menu

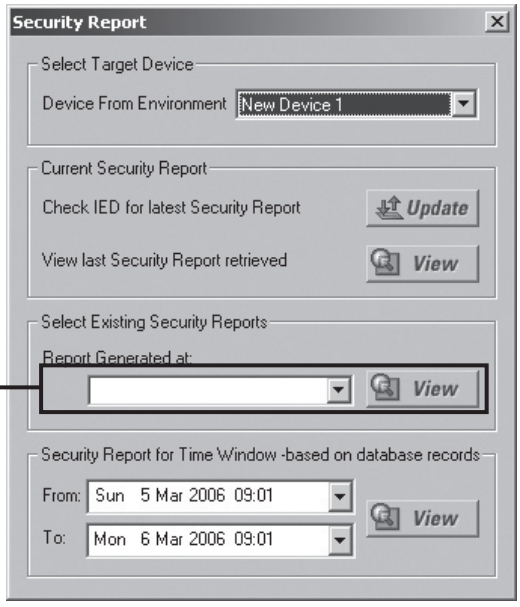


Fig.5.

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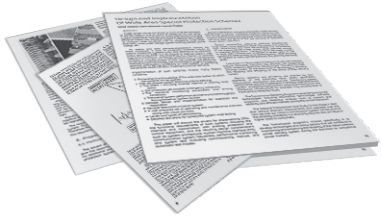

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SCHEDULED COURSES IN NORTH AMERICA

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UR Advanced Applications	$3,000 USD	3.5			23-27 Toronto, CAN		
UR Platform	$1,800 USD	2.1	14-16 Toronto, CAN		17-19 Toronto, CAN		4-6 Toronto, CAN
Industrial Power Systems Communications	$1,200 USD	1.4		21-22 Toronto, CAN			
Utility Power Systems Communications	$1,200 USD	1.4	23-25 Toronto, CAN				7-8 Toronto, CAN
Distribution Protection Principles & Relaying	$1,800 USD	2.1		18-20 Toronto, CAN		28-30 Toronto, CAN	
Fundamentals of Modern Protective Relaying	$2,400 USD	2.8		12-15 Toronto, CAN		14-17 Toronto, CAN	
Motor Protection Principles & Relaying	$1,800 USD	2.1			3-5 Toronto, CAN		18-20 Toronto, CAN
EnerVista Software Suite Integration	$600 USD	0.7			6 Toronto, CAN		
F650 Bay Controller	$1,800 USD	2.1					
Introduction to the IEC61850 Protocol	$1,800 USD	2.1		26-28 Toronto, CAN			12-14 Toronto, CAN
Substation Automation Fundamentals	$1,200 USD	1.4					
Metering with the PQM & EPM series Meters	$1,200 USD	1.4			11-12 Toronto, CAN		
JungleMUX Hands-on	$3,800 USD	3.5		11-15 Vancouver, CAN		13-17 Denver, US	

SCHEDULED COURSES IN EUROPE

Courses for 2006	Tuition	CEU Credits	AUG 06	SEP 06	OCT 06	NOV 06	DEC 06
UR Advanced Applications	$3,000 USD	3.5		25-29 Bilbao, Spain		27-Dec 1 Bilbao, Spain	
UR Platform	$1,800 USD	2.1		20-22 Bilbao, Spain		22-24 Bilbao, Spain	
Distribution Protection Principles & Relaying	$1,800 USD	2.1					
Fundamentals of Modern Protective Relaying	$2,400 USD	2.8					11-14 Bilbao, Spain
Motor Protection Principles & Relaying	$1,800 USD	2.1					
F650 Bay Controller	$1,800 USD	2.1				6-8 Bilbao, Spain	
Introduction to the IEC61850 Protocol	$1,800 USD	2.1				9-10 Bilbao, Spain	

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