Application of Modern Relays to Dual-Breaker Line Terminals

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1. Introduction

Standard practice today with respect to protecting dual-breaker line terminals – breaker-and-a-half or ring-bus – is to sum the two breaker currents externally and feed a single-input line relay (distance, line current differential or phase comparison) with the total cur-rent flowing into the protected line. Breaker failure protection requires monitoring the two breakers and currents separately, and is typically implemented as a stand-alone device out-side of the main protection relay. Reclosing and synchrocheck control functions require monitoring and controlling both breakers as well as measuring two pairs of voltages for the purpose of synchrocheck, are also – in majority of cases – implemented outside of the main line protection device.

This paper discusses several protection and control aspects in relation to dual-breaker line terminals.

First, breaker failure and reclosing functions are discussed as applied to dual-breaker configurations.

Second, the paper talks about protection security as related to saturation of Current Transformers (CTs) under fault currents flowing locally through the two breakers. When the two currents are summated externally, the CT errors – if significant – can override the potentially low actual line current, and cause stability problems for the main line protection. Not only sensitive ground overcurrent functions are jeopardized, but also distance, current differential, or phase comparison. The paper explains the problem and presents solutions.

Stub bus protection is also discussed as pertaining to dual-breaker configurations.

The paper looks at the above applications from the point of view of a modern micro-processor-based relay. New generation of line relays support dual CT inputs to monitor both breakers individually, and three voltage points to provide for the main line protection, and synchrocheck across both breakers. These relays often include two breaker failure, two synchrocheck, and dual-breaker autoreclose functions. This allows integrating protection, breaker failure and reclose functions into a single relay. The paper points to advantages and disadvantages of such integration, and provides some guidance regarding dual-breaker line applications.

2. Capabilities of Modern Line IEDs

Modern microprocessor-based line protection relays (or Intelligent Electronic Devices, IEDs) allow for protection and control of the dual-breaker line arrangement from a single device. Application of separate breaker failure and/or synchrocheck relays is no longer dictated by limitations of the main protection relay, but driven by the user's protection philosophy to either combine the required functions, mostly for the for cost benefit, or to keep them separate for security, retaining present testing and maintenance practices, avoiding re-training the personnel, etc.

With reference to Figure 1, a modern IED capable of the dual-breaker application supports two three-phase current inputs in order to measure both the currents individually for the breaker failure protection (50BF), backup overcurrent protection (51P), and associated metering functions. The two currents are added internally in the relay's software to become the input for the distance (21) or high-set overcurrent (50) functions. When properly implemented, the line current differential (87L) and phase comparison (87PC) functions use individual currents for stability under through fault conditions.

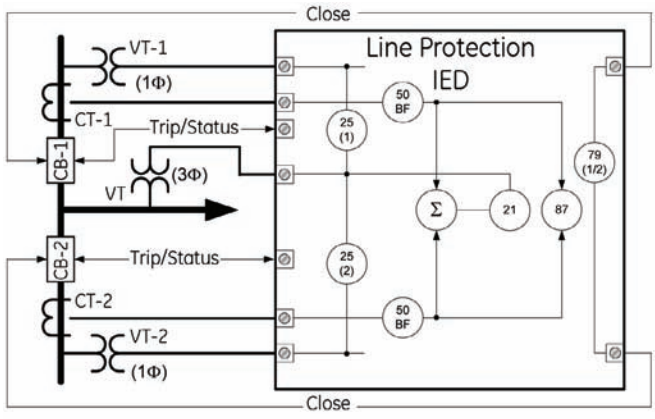

Figure 1.
Modern dual-breaker line IEDs.

Such modern IED typically support one three-phase voltage input required for the main (distance) or backup protection (distance backup on line current differential or phase comparison relays), and at least two single-phase voltage inputs in order to facilitate synchrocheck (25) across both the breakers. A dual-breaker autorecloser (79) controlling both breaker simultaneously and capable of advanced reclose modes (sequential, simultaneous, breaker out of service, etc.) completes the application. A suite of backup and auxiliary functions are typically attached to the voltages and the three currents (breaker 1, breaker 2, line).

In addition to the required AC inputs these IED are designed to support enough binary inputs (breaker status, external breaker fail initiate) and output contacts (trip for both breakers, reclose per breaker, breaker fail re-trip and trip, etc.) to facilitate protection and control of a dual-breaker line terminal from a single IED.

3. Breaker Failure Considerations

Being a backup function, the BF protection may be required to use a different CT core, an independent current path, independent relay hardware, and a separate tripping path. This requirement is naturally met when using a stand-alone BF relay, but can as well be accomplished on multi-function relays without a separate BF device, at the expense of extra signaling between the relays.

Figure 2 presents four approaches to distributing the Fault Detection (FD) and BF functions between multiple relays.

Figure (a) is a traditional scheme with a dedicated BF relay.

Figure (b) presents a simple scheme with an integrated BF function per each fault detection function. No external BFI signals are used.

Dependability is directly proportional, while security is adversely proportional, to the number of operational copies of a given protection function. Predominately, we deploy one BF function per breaker, and the associated performance characteristics primarily in terms of spurious operations, are closely related to this practice. Currently this performance is considered satisfactory.

Wide penetration of simple integrated BF schemes that follow the approach of Figure 2a with codependency on the common signal path and relay hardware, and with 2 to 4 BF elements per each breaker, may significantly elevate the risk of large outages due to BF misoperations.

This danger can be alleviated while integrating the BF functions but at price of increased complexity.

Figure (c) shows a crosscheck scheme. Each fault detection function initiates its own BF function. This BF function is placed on the other relay so that a crosscheck is made between detecting the fault and detecting the BF condition. This scheme calls for wiring the BFI signals, and cross-monitoring of relay fail safe outputs so that upon the failure of one of the relays the other relay could switch to its own internal BF function.

Figure (d) presents a solution with a single BF allocated statically to one of the relays.

Figure (e) shows an integrated and single BF but in a switchover scheme. Normally both relays initiate the same integrated BF (one internally and one externally). Upon the failure of the relay that normally performs the BF function, the other relay switches to its own integrated BF element.

The configuration of a stand-alone BF relay (Figure 2a) fits naturally the past protection practice with external summation of CTs for the line relay. Traditional line relays did not measure the two currents individually and could not integrate the BF function for both the breakers anyway.

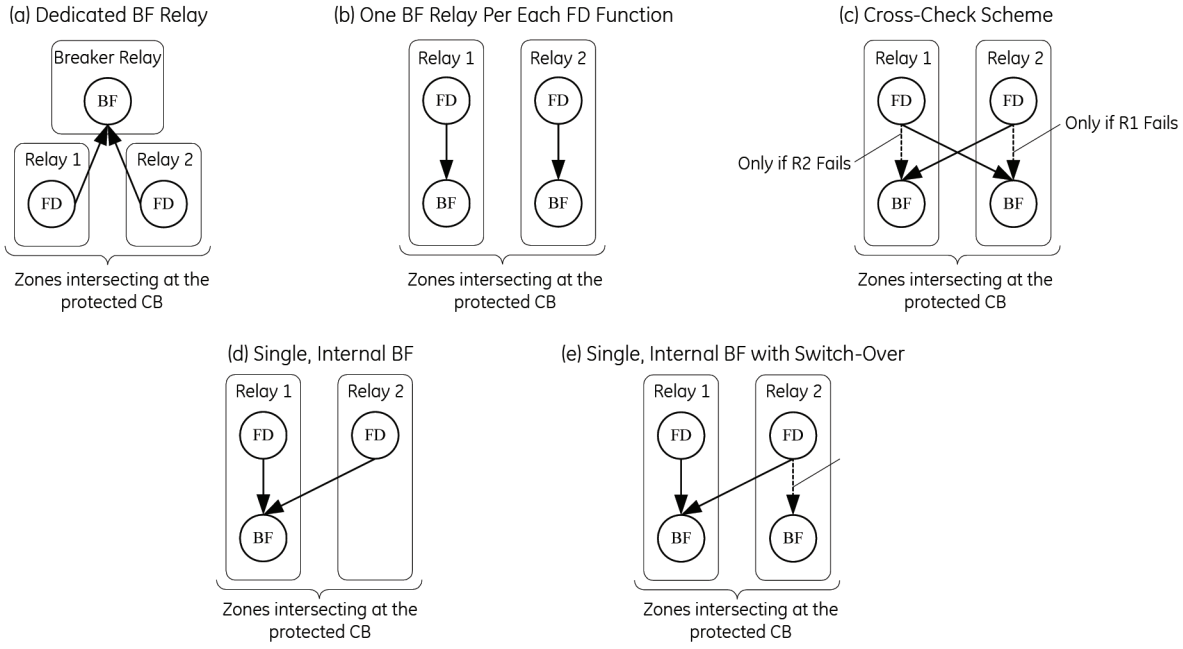

Figure 2.
Allocations of the fault detection (FD) and BF functions between relays.

With modern line relays the BF for dual-breaker terminals can be integrated using any of the approaches outlined in Figure 2. For example, Figure 3a shows the "one BF per each fault detection function" approach of Figure 2b; and Figure 3b shows an implementation of the crosscheck scheme of Figure 2c.

Note that with the BF initiation from the adjacent zone for one of the two breakers, the other breaker of the dual breaker arrangement needs to be tripped. With this respect the solution of Figure 3a requires wiring the BF Trip signals while avoiding wiring the BFI signals; and solution of Figure 3b calls for wiring more BFI signals, but some BF trips are routed internally in the relays.

Advantages of integrating BF in dual-breaker applications are:

- Cost and space advantage by eliminating stand-alone Breaker Failure relay(s).
- Simplified wiring and interlocking. Every wiring termination is a potential point of failure, so reducing the amount of wiring increases reliability.
- BF simpler and easier to test thus reducing probability of spurious BF trips due to human errors during maintenance.
- More flexible initiation logic such as from voltage or frequency triggered trips.
- Easier application of multiple setting groups (banks) to adapt the BF function to changing system conditions.
- Direct access to the existing DTT/pilot channels via line relays for tripping re-mote breakers.

Disadvantages of utilizing integrated BF in dual-breaker applications are:

- Impact on security: The BF function uses same current inputs, hardware and software, and the tripping paths as the fault detection function. This minor disadvantage can be addressed by crosschecking as explained in Figures 2c and 3b.
- Impact on security: Multiple copies of the BF function operational for the same breaker potentially increase the probability of misoperation. As a backup function, the BF should not be duplicated or quadrupled. This problem can be solved by using a switchover scheme of Figure 2e or a pre-selected BF location of Figure 2d.

The above advantages and disadvantages should be weighted accordingly taking into account other factors, relaying philosophy and maintenance practice in particular. Factors to consider are:

- Preferred degree of security and reliance on remote versus local backup.
- Degree of integration of primary (fault detection) and backup (BF) functions on a single multifunction relay.
- Existing maintenance/testing practice, willingness and capacity to adjust.
- Preferences with respect to simplicity and cost targets.

4. Automatic Reclosing Considerations

Similarly to the BF protection function, the Autoreclosure (AR) control function can reside in a standalone dedicated breaker control relay, one per each breaker; or can be integrated in a multifunction line relay.

In any case, fundamental AR issues are the same; initiation, blocking, lockout, switch onto the fault logic, dead time for different types of the faults and different shot counts, tripping during evolving faults in single-pole tripping and reclosing applications, and the master-follower logic.

Proper treatment of the middle breaker is yet additional factor specific to dual-breaker applications. The middle breaker is controlled from both the line zones that intersect at the breaker.

In the case of integrated BF, multiple BF functions for the same breaker may not be viewed as beneficial from the security point of view, but are certainly acceptable as a simple solution.

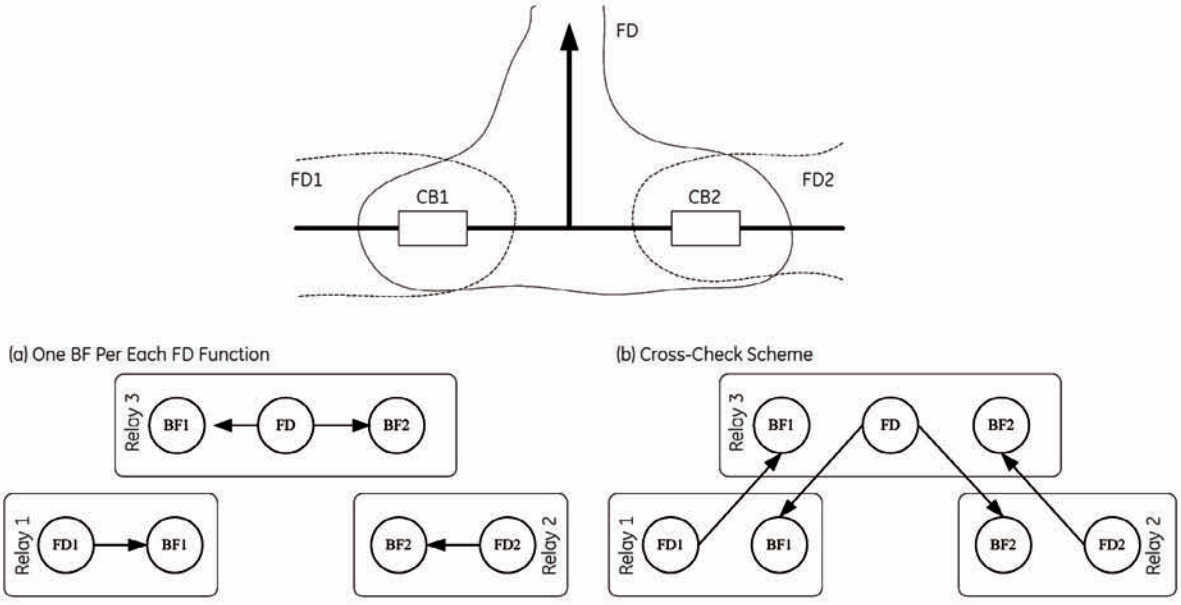

Figure 3.
Selected BF schemes of Figure 2 as applied to dual-breaker line terminals.

On the other hand, multiple copies of the AR function for the same breaker are typically considered not acceptable. The AR is a complex and sequential controller. Paralleled, not synchronized instances of the AR would cause performance problems and pose testing and maintenance challenges. As a result, solutions depicted in Figure 2a (stand-alone AR), 2c (single preselected internal AR) or 2d (internal AR in a switch-over scheme or "hot stand-by") can be considered.

The "one AR at a time" philosophy applies to multiple possible allocations of the AR function (A and B systems, 2 adjacent zones).

Beyond the common requirements ARs for dual-breaker applications should support the following features:

- Allowing choosing sequence of reclosing (1-2, 2-1 or simultaneous reclose operation).
- Ability to transfer the close command from one breaker to another if the breaker pre-selected to close first is taken out of service or failed to close.
- Ability to recognize that breaker was open prior to the line fault either manually or by adjacent protection. If used, lockout relays solve this problem. If the operational philosophy relies on the reclosers to lockout under the time-extended trip commands, the dual breaker AR needs to be designed/configured accordingly to lockout one breaker while permitting to control the other.
- If required for a given system topology, ability to check synchronism across each breaker individually, as the transmission system may become electrically isolated across each breaker and/or remote terminals.
- When required, ability to perform single-pole operation including tripping and reclosing under evolving faults considering simultaneous or near simultaneous faults on the parallel line that call for tripping and reclosing of the common (middle) breaker.

5. Protection Security under CT Saturation

Fed with externally added currents (Figure 4a) a typical line relay responds to a vectorial sum of the two local currents. If both the CTs operate with no errors, the sum of the cur-rents is an accurate representation of the line current at this terminal. If one of the CTs saturates, the produced error signal will effectively superimpose on the true line current and cause potential problems for the protection security. The situation is particularly dangerous if the feed through the line is weak, and the CT carrying the reverse current saturates on a close in external fault (Figure 4b). A portion of the missing reverse current will leave the forward current not balanced, and appear to the relay in the forward or tripping direction.

It may appear that line current differential relays would not have problems with saturated CTs. This is true only if a given relay measures all currents of its differential zone individually and produces proper restraint or other countermeasures to the problem of CT errors. If fed with externally summated currents a line current differential relay produces the restraint signal as per its design equations based on the summation of the two local cur-rents. Because the relay does not respond to the individual currents, but to the sum of thereof, a combination of restrained and unrestrained differential principles is effectively applied, and as such, it may face stability problems. For example, with weak feed from the remote terminal(s), and a large through fault current along the breaker-and-a-half diameter, CT saturation errors would manifest themselves as a spurious differential current while relatively small restraint would be produced from the small, remote-end currents (high through-diameter current not seen by the relay, low through-line current seen by the relay as depicted in Figure 4b).

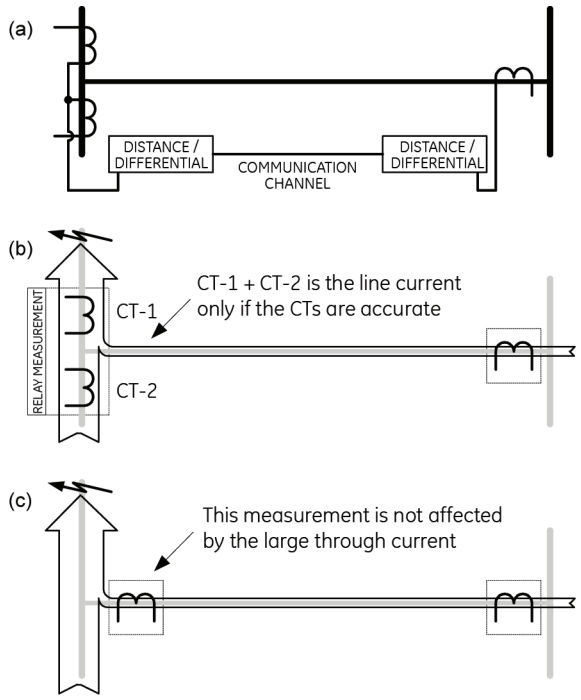

Figure 4.
Dual-breaker arrangement: external CT summation (a), through fault under weak remote and strong local systems (b), through fault in a single-breaker application (c).

This problem does not exist in single breaker applications (Figure 4c). With the line cur-rent measured directly in single-breaker applications there is no danger of producing a large error signal even if the line CT saturates. If an error occurs due to CT saturation, it is properly restrained by the principle of percent differential protection.

The problem in the dual-breaker configuration demonstrates itself not only under severe CT saturation, but could become significant under relatively small CT errors, including linear errors related to the CT accuracy class. As long as the through current of the line is considerably higher compared with the error current produced by the CTs, there is no danger of the CT error signals overriding the actual through line current. When the error current is comparable with the through current, the protection system is in danger of misoperation. The through current could be low for long lines and/or when the remote system is relatively weak. The short circuit level of the local system alone controls the current flowing along the dual-breaker diameter. With the local terminal strong, and the remote terminal weak, any relay could be brought to its design limits by saturating one or more CTs on the diameter.

Distance relays are also exposed to this problem. During close-in reverse faults, the volt-age is depressed to very low levels, and stability of the relay is maintained solely by the directional integrity of the currents as measured. If, under such circumstances, CT that carries the current away from the terminal saturates (CT1 in Figure 4b), an error current appears in the direction of the line. With enough error current, the through line current becomes over-ridden, and the actual reverse fault direction may be seen as forward by the relay. As a result, with the voltage depressed and the current elevated and flowing spuriously in the for-ward direction, distance functions may pickup inadvertently. This includes a directly trip-ping under-reaching zone 1, as well as an overreaching zone 2 typically used by communication-assisted schemes. In both cases, a false trip could occur.

Current-reversal logic, application of a blocking or hybrid permissive schemes, or similar approaches, may enhance the performance and solve the problem partially. These approaches, however, often rely on a reverse-looking distance zone 4. The latter may spuriously drop out when the effective current gets inverted from the true reverse to a false for-ward direction due to CT errors. Extending the blocking action by using timers is a crude solution, but would jeopardize dependability and speed of operation on evolving external-to-internal faults.

Ground directional overcurrent functions, neutral and negative-sequence specifically – being both fast and sensitive – are good supplements enhancing performance of communication-assisted schemes [4]. They, however, face similar security problems in the dual-breaker applications. With reference to Figure 5 consider an external line-to-line fault on the diameter. In this case performance of all four CTs (A1, A2, B1 and B2) affects the neutral current. With any of the CTs saturating, a spurious neutral current will be created. There is no real neutral current through the line for this type of fault. Therefore, the operating signal for the Neutral Directional Overcurrent function is entirely driven by CT errors. The remote terminal will see the fault via its distance function and key permission to trip, unless separate pilot channels are used to key from distance and ground directional functions. Combined with the spurious operation of the neutral directional function at the local terminal, the received permission would cause a false trip.

The above problem with sensitive ground directional overcurrent functions also exists in single-breaker applications. However, in single-breaker applications the relay would measure the elevated phase currents. Modern relays allow for positive-sequence restraint in neutral or negative-sequence directional overcurrent functions, effectively solving the problem [4]. In a dual-breaker terminal with external CT summation, the positive-sequence restraint would not work.

Phase comparison relays supplied with the external sum of the currents would face the same stability problems in dual-breaker applications. Contrary to the commonly understood immunity of the phase comparison principle to CT saturation, the 87PC function requires all currents of its zone to be measured individually and included in its coincidence timing. Only by looking at the two local currents individually, a phase comparison relay would have a chance to recognize the through fault condition and develop a proper countermeasure as per the principle of phase comparison.

6. Supervision Logic for Impedance-based Protection

This section outlines a simple supervisory logic to ensure security of the main line protection during through current conditions on the dual-breaker diameter with weak feed through the line. The logic can be programmed from a number of standard Instantaneous Overcurrent elements (IOCs) and Phase Directional (Ph Dir) elements of a relay.

The supervisory logic has been developed to meet the following requirements:

- The supervision should not penalize the speed of response to internal faults (trip time) or sensitivity of the relay to high-resistance internal faults. Therefore, permission to trip should be given all the time unless a through fault condition is detected.
- Permission to trip should be maintained during transitions from load conditions, possibly a reverse load, to internal faults.
- The supervision should allow the relay to trip an evolving external-to-internal fault, in particular with both faults present at the same time, i.e. before the external fault is cleared by the associated protection system.
- The supervision should respond to elevated phase currents as the high phase currents cause CT errors and the latter could jeopardize security of the line protection. Responding to sequence components is not preferred because under evolving faults flows of negative-sequence and neutral currents may be considerably changed from expected.
- The supervision shall be easily applied to distance, differential, and overcurrent directional functions.

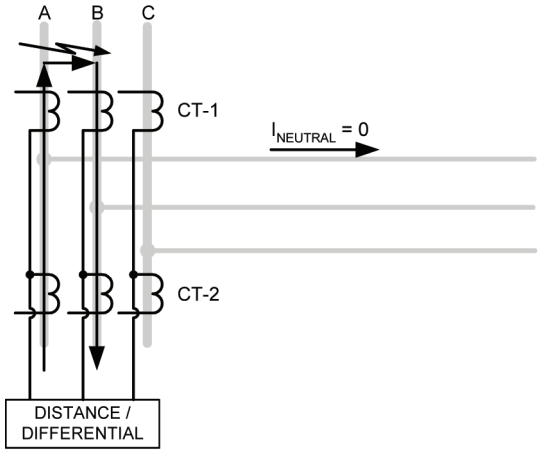

Figure 5.
Danger of a spurious neutral current in a dual-breaker line application.

6.1 Protection Elements Used by the Supervisory Logic

With reference to Figures 1 and 6 the following elements are used:

- IOC 1 to respond to forward current of CT-1. The element shall be set at 2-3 times the nominal of CT-1, and is used to unblock the relay on external-to-internal evolving faults.
- IOC2 to respond to elevated current of CT-1; set at 1.5-2 times the nominal of CT-1 and used to supervise the blocking action.
- PHS DIR 1 to respond to reverse current direction at CT-1.
- IOC3 – similar to IOC1, but for CT-2.
- IOC4 – similar to IOC2, but for CT-2.
- PHS DIR 2 – similar to PHS DIR 1, but for CT-2.

The directional functions in one particular application [1-3] use quadrature polarization with memory action, if required.

6.2 Supervisory Logic

A reverse direction for CB-1 (Figure 6a) is declared if both currents are elevated (IOC2 and IOC4) and the directional element sees a reverse direction (PHS DIR 1 BLK). Similar logic is implemented for CB-2, and phases B and C. The reverse direction flags will be asserted only if an elevated current is flowing through the diameter, and the direction is re-verse in one of the breakers.

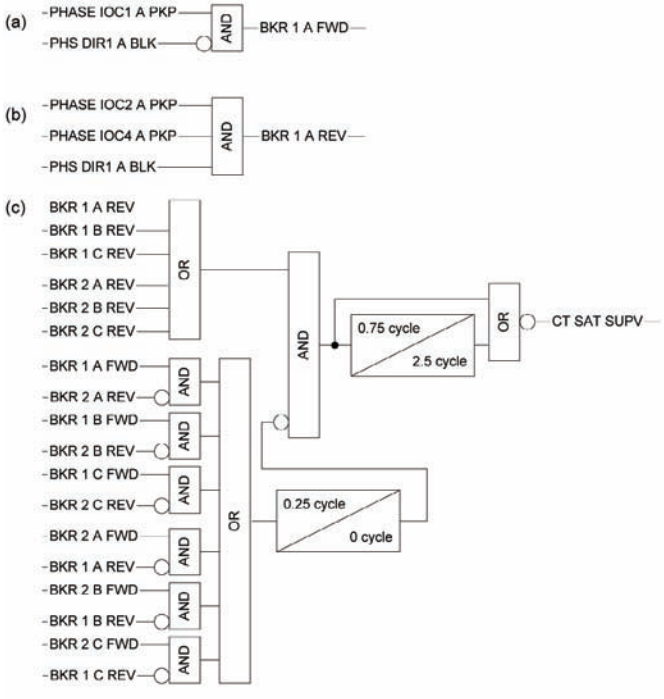

Figure 6.
Supervisory logic to cope with CT errors in the dual-breaker configuration.

A forward direction for CB-1 (Figure 6b) is declared if the current is elevated in the CB-1 leg and appears in the forward direction. Declaration of the forward direction is not impacted by the situation in the second leg of the diameter. Similar logic is implemented for CB-2, and phases B and C.

As shown in Figure 6c, the blocking action is established if any of the three phases shows a through current flowing outside of the zone, either through CB-1 or CB-2.

For security, the blocking action gets artificially extended for extra 2.5 cycles after being present for 0.75 of a cycle (switch off transient logic to cope with clearance of the external fault).

The blocking action gets cancelled if any of the currents is elevated, appears in the forward direction, and is not accompanied by the reverse direction in the other breaker in the same phase. A 0.25 cycle delay is added for security.

6.3 Performance Analysis and Explanation

During load conditions (current below some 1.5 times CT nominal) none of the IOCs is picked up and the trip permission is asserted permanently.

During internal fault conditions with very weak feed from the local terminal, the current is not elevated and may appear in the reverse direction as dominated by the load – permission is maintained as none of the IOCs picks up.

During high current internal faults, none of the directional elements operates in the re-verse direction, and the trip permission is maintained.

During external faults with one breaker opened, the blocking action is not established, but it is not needed either.

During external faults with both breakers closed, the blocking action is established as long as both the currents flowing through the diameter are above the pickup of IOC2 and IOC4.

During evolving external-to-internal faults in different phases, the blocking action is first established (phase A for example), and then canceled when the second fault appears in the forward direction in a different phase (phase B for example).

The output flag, CT SAT SUPV of Figure 6c, shall be used to supervise distance and ground directional functions of a distance relay, and the differential function of a line current differential relay, if required.

6.4. Transient Response Examples

Figure 7 presents an external fault example. The trip supervision is removed in 0.5 of a power cycle when using one particular IED [1-3] to implement the logic of Figure 6c.

Figure 8 shows an evolving fault example. The trip supervision is removed in 1 cycle after the external fault, but is re-established in 0.75 of a cycle after the fault evolves into internal.

7. Line Current Differential Solution

This section presents a description of a line current differential algorithm [5-6], but ex-tended to dual-breaker applications.

The concept [5-6] has been originally implemented for a single-breaker arrangement. In such an application, each relay [2] sends phasors of local current in all three-phases calculated using a half-cycle estimator (6 numbers) as well as dynamic terms used for adaptive restraint (3 numbers). Some extra data is appended to this core of the packet such as relay ID, virtual I/Os for teleprotection, time stamps to facilitate synchronization with the use of the ping-pong algorithm [6], GPS-driven time stamps to facilitate channel asymmetry compensation [7], CRC-check, etc.

The presented solution targets communications channels of 64kbps. The baud-rate of the channel imposes certain limitation for the packet size. Application to dual-breaker configurations calls for producing a proper restraining signal out of all the currents of the zone. For example, in three-terminal applications with each of the terminals being breaker-and-a-half or ring-bus, 6 three-phase currents surround the line differential zone. Exchanging all these currents between the terminals would increase the packet size.

The following design targets have been stated for the line current differential function capable of secure operation at multi-breaker terminals:

- The packet size should remain unchanged. A total of 9 numbers must represent currents at each terminal in terms of phasors (real, imaginary) and static and dynamic restraint factors.
- Window resizing shall be applied for fast relay operation.
- Proper restraint shall be produced to secure the differential system on external faults through the local terminal's breakers.
- Up to four currents could be used at each terminal in order to facilitate combined bus and line protection for small buses.
- Backwards compatibility of the operating principle shall be maintained if the relay is applied in a single breaker configuration.

The following subsections address the above design constraints and goals.

7.1 Phasor Estimation

The input currents are sampled at 64 samples per cycle and pre-filtered using an optimized MIMIC filter aimed at removing dc component(s) and other low-frequency oscillations. The optimized filter is a Finite Response Filter (FIR) with the window length of approximately 1/3rd of a power system cycle.

The digitally pre-filtered currents are converted into phasors by applying half-cycle Fourier algorithm. The half-cycle values are either used as calculated, or two consecutive half-cycle measurements are combined into an equivalent full-cycle measurement. The operation of switching from full- to half-cycle upon detecting disturbance in currents is referred to as "window resizing" and is implemented to speed up operation of the relay. The differential system transmits half-cycle values, and the resizing is done independently at each terminal of the line.

Half-cycle magnitudes are also calculated and transmitted in order to reflect properly through fault conditions at each terminal of the line.

In addition "a goodness of it" factor is calculated for each current in order to measure the error between the waveform and its Fourier-estimated phasor [7]. The goodness of fit factor is further used to produce an extra restraint to countermeasure the estimation error, and increase security of the relay. Conceptually, the goodness of fit factor is proportional to the following value:

$$\delta_{(k)} = \sum_{n=0}^{N-1} \left| x_{(k-n)} - X_{(k)} \cdot \cos\left(\frac{2 \cdot \pi \cdot n}{N} + \Theta_{(k)} \right) \right|^2 \qquad (1)$$

In equation (1), the present magnitude and phase estimate (X,Q) at the k-th sample is compared with the actual waveform (x) over the duration of the data window (N), and the sum of squares error measure is calculated.

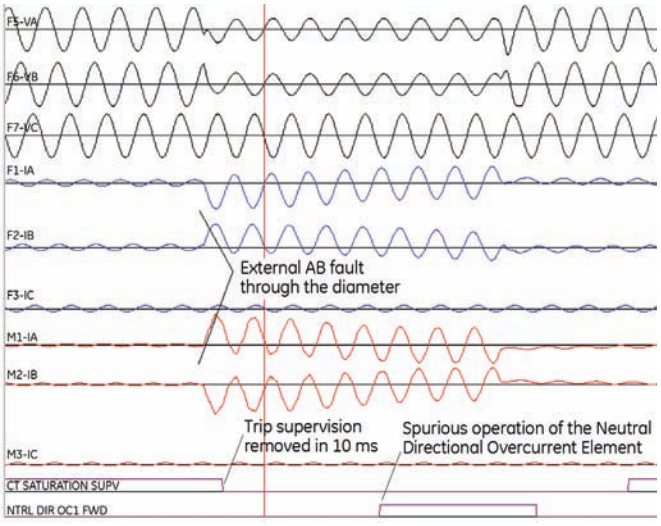

Figure 7.
External Fault. Phase-to-phase fault through the diameter causes enough CT error to operate spuriously the Neutral Directional OC function. The CT logic blocks in 0.5 cycle.

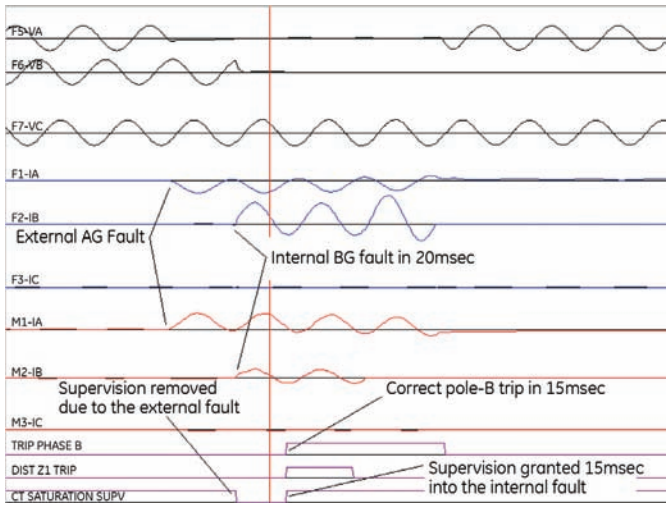

Figure 8.
External-to-Internal Evolving Fault Example. The relay trips single-pole the correct phase despite the pre-existing external fault. The CT logic unblocks in 0.75 of a cycle.

7.2. Consolidating Local Currents – the Outgoing Packet

Each terminal of the current differential system consolidates the local signals into an outgoing packet. Compression of information takes place in order to reduce the packet size and distribute the calculations between the two or three relays of the line current differential system. This is possible without compromising operating equations or accuracy if the operating equations are shaped accordingly.

First, the phasors (real, imaginary) of all the local currents are summated to give a sub-sum of the total differential current of the protected line:

$$I_{LOC\_RE\_A} = I_{1\_RE\_A} + I_{2\_RE\_A} + \ldots \quad (2)$$

Equation (2) is applies to up to four local current inputs and holds true for both real and imaginary parts, in all three phases. Equation (2) is not a differential current, but a portion of the differential current that involves the local currents only.

Second, the measure of a through fault current is estimated locally using magnitudes of all the local currents via the following equation:

$$\left(I_{LOC\_TRAD\_A}\right)^2 = \max\left(\left(I_{1\_MAG\_A}\right)^2, \left(I_{2\_MAG\_A}\right)^2, \ldots\right) \quad (3)$$

Equation (3) selects, on a per phase basis, the largest among the local currents to be a measure of the local restraint.

Figure 9 illustrates the principles behind equations (2) and (3).

Third, the protection system applies differential characteristic locally to each of the re-straining currents. The presented system does not use an explicit restraining characteristic, but the total operating and restraining value [5-6]. The latter incorporates values of the pickup, slopes (S1, S2) and breakpoint (B). The following equations are used to accommodate the characteristic:

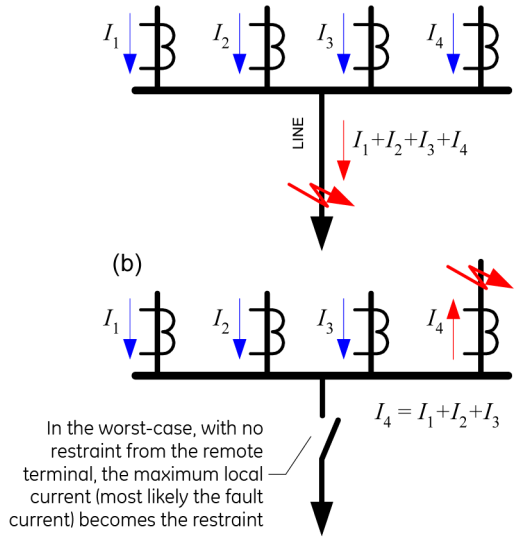

Figure 9.
The differential current is created from partial sums of all the local currents (a). The restraining current is created based on the maximum local current (b).

- In two-terminal applications:

$$\text{If } \left(I_{LOC\_TRAD\_A}\right)^2 < B^2$$

Then

$$\left(I_{LOC\_REST\_TRAD\_A}\right)^2 = 2 \cdot (S_1)^2 \cdot \left(I_{LOC\_TRAD\_A}\right)^2 \quad (4a)$$

Else

$$\left(I_{LOC\_REST\_TRAD\_A}\right)^2 = 2 \cdot \left((S_2)^2 \cdot \left(I_{LOC\_TRAD\_A}\right)^2 - (S_2 \cdot B)^2\right) + 2 \cdot (S_1 \cdot B)^2 \quad (4b)$$

- In three-terminal applications:

$$\text{If } \left(I_{LOC\_TRAD\_A}\right)^2 < B^2$$

Then

$$\left(I_{LOC\_REST\_TRAD\_A}\right)^2 = \frac{4}{3} \cdot (S_1)^2 \cdot \left(I_{LOC\_TRAD\_A}\right)^2 \quad (4c)$$

Else

$$\left(I_{LOC\_REST\_TRAD\_A}\right)^2 = \frac{4}{3} \cdot \left((S_2)^2 \cdot \left(I_{LOC\_TRAD\_A}\right)^2 - (S_2 \cdot B)^2\right) + \frac{4}{3} \cdot (S_1 \cdot B)^2 \quad (4d)$$

The adaptive portion of the restraint is a geometrical sum of errors derived from equation (1) and a measure of the clock synchronization error [5-6]. The traditional and adaptive restraints are combined geometrically using a concept of an extra arbitrary multiplier:

$$I_{LOC\_RESTRIANT\_A} = \sqrt{\left(I_{LOC\_REST\_TRAD\_A}\right)^2 + MULT_A \cdot \left(I_{LOC\_ADA\_A}\right)^2} \quad (5)$$

The multiplier increases the impact of signal distortions on the restraint, and is used to provide better restraint during CT saturation conditions on through line faults.

Values defined by equations (1-5) are based on half-cycle windows, and constitute the following outgoing packet:

$$I_{LOC\_RE\_A}, I_{LOC\_RE\_B}, I_{LOC\_RE\_C}, I_{LOC\_IM\_A}, I_{LOC\_IM\_B}, I_{LOC\_IM\_C}, \ldots$$

$$\ldots, I_{LOC\_RESTRAINT\_A}, I_{LOC\_RESTRAINT\_B}, I_{LOC\_RESTRAINT\_C} \quad (6)$$

7.3 Total Differential and Restraint Currents

The local and remote data when received are used to calculate the total differential and restraining signals for the current differential system.

Before the data is used, a decision is made to either use the full- or half-cycle measurements. The half-cycle data is used one time after detecting a fault. After such half-cycle window is used, the relay switches back to the full-cycle version when proceeding into the fault. Also, when a packet is lost, the next packet that arrives triggers window resizing. This is simply to enable protection using the latest packet even though the previous packet required to calculate the full-cycle quantities is lost due to the communication channel impairments.

The following equations are used to combine the half-cycle values into full-cycle measurements:

$$I_{LOC\_PHASOR\_RE\_A} = 0.5 \cdot \left(I_{LOC\_RE\_A(present)} + I_{LOC\_RE\_A(previous)}\right) \quad (7a)$$

$$\left(I_{LOC\_PHASOR\_RESTRAINT\_A}\right)^2 = 0.5 \cdot \left[\left(I_{LOC\_RESTRAINT\_A(present)}\right)^2 + \left(I_{LOC\_RESTRAINT\_A(previous)}\right)^2\right] \quad (7b)$$

Equation (7b) is accurate; equation (7b) is a good approximation. Equations (7) apply to both local and remote signals, all three phases, and real and imaginary parts.

Next, the relay calculates the total differential and restraint currents:

$$I_{DIFF\_RE\_A} = I_{LOC\_PHASOR\_RE\_A} + I_{REM1\_PHASOR\_RE\_A} + I_{REM2\_PHASOR\_RE\_A} \quad (8a)$$

$$\left(I_{REST\_A}\right)^2 = \left(I_{LOC\_PHASOR\_RESTRAINT\_A}\right)^2 + \left(I_{REM1\_PHASOR\_RESTRAINT\_A}\right)^2 + \left(I_{REM2\_PHASOR\_RESTRAINT\_A}\right)^2 \quad (8b)$$

And applies the so-called fault severity equation in order to decide if the line should not should not be tripped [5-6]:

$$S_A = \left(I_{DIFF\_A}\right)^2 - \left(P^2 + \left(I_{REST\_A}\right)^2\right) \quad (9)$$

The relay (87L function) operates if the fault severity, S, is positive.

P is the pickup of the characteristic (the slopes and breakpoints were already accommodated before sending the data in equations (4)).

As indicated by all the equations, the algorithm is fully phase-segregated.

7.4 CT Saturation Detection

The algorithm has a built-in immunity to saturated CTs owing to the concept of the dynamic restraint. The goodness of fit (1) becomes degraded on saturated waveforms, producing a measure of error (1), which added to the restraining signal allows for extra security.

In order to boost this natural effect, the system is using an adaptive multiplier in order to increase further the impact of the dynamic portion of the restraint (5) on the overall performance of the relay.

The multiplier is calculated adaptively per phase as follows:

$$MULT_A = \max\left(MULT_{1A}, MULT_{2A}\right) \quad (10)$$

The first component is based on local currents only, and as such is instantaneous. This component is meant to detect through fault condition on the local diameter of the breaker-and-a-half or ring-bus configuration.

The second component is based on local and remote currents, and as such is lagging the real time by the channel propagation time. This component is meant to detect through fault conditions between terminals of the line.

The first multiplier is calculated as follows:

Step 1. Select the greatest current from the local currents. The selection is based on half-cycle magnitudes: I1_MAG, I2_MAG, I3_MAG, I4_MAG. Assume the largest current is in the k-th circuit (k = 1,2,3 or 4).

Step 2. Calculate two auxiliary currents:

$$I_{X\_RE} = I_{k\_RE} \quad (11a)$$

$$I_{X\_IM} = I_{k\_IM} \quad (11b)$$

$$I_{Y\_RE} = I_{1\_RE} + I_{2\_RE} + I_{3\_RE} + I_{4\_RE} - I_{X\_RE} \quad (11c)$$

$$I_{Y\_IM} = I_{1\_IM} + I_{2\_IM} + I_{3\_IM} + I_{4\_IM} - I_{X\_IM} \quad (11d)$$

The X-current is the maximum current among the local currents. The Y-current is the sum of all the local currents but the maximum current. Note that during through faults with no feed from the remote terminals IX = -IY if no CT saturation. With CT saturation the cur-rents differ, but remain approximately out of phase.

Step 3. Calculate the multiplier as follows:

$$\text{IF } \left|I_X\right| > 3pu \quad \& \quad \left|I_Y\right| > 3pu \quad (12a)$$

$$\text{Then} \quad abs\left(angle\left(I_X, I_Y\right)\right) > 90^o \quad (12b)$$

$$\text{Then} \quad MULT := abs\left(angle\left(I_X, I_Y\right)\right) \cdot \frac{5}{180^o} \quad (12c)$$

$$\text{else} \quad MULT := 1 \quad (12d)$$

$$\text{Else} \quad MULT := 1 \quad (12e)$$

Equations (12) check if both currents (the maximum among the local currents, and the sum of all the other local currents) are large enough to cause significant CT saturation. If so, the relative direction of the two currents is checked. If the angle is less than 90 degrees, the multiplier stays at the "neutral" value of 1.00. If the angle is larger than 90 degrees, the multiplier is proportional to the angle difference and could reach the maximum value of 5.00 if the currents are exactly out of phase.

The second multiplier is calculated applying exactly the same procedure, but instead of using local currents, the procedure uses the sum of the local currents, and the remote cur-rents. In other words the currents into the line at each of up to three terminals of the line, regardless of the number of local currents at each terminal of the line. The second multiplier detects through fault conditions of the entire line.

Figure 10 illustrates operation of the presented algorithm under through fault conditions. In this example the traditional restraint of 15pu, is additionally augmented by adding the dynamic factor. The dynamic restraint is naturally increased by saturated CT, and artificially multiplied by the multiplier. In this example, the T3 terminal sees CT saturation in the circuit carrying the current out of the line toward the fault. This CT saturation will jeopardize stability of all terminals. However, all terminals will use high values of the multiplier to boost the effect of dynamic restraint, and will not misoperate.

7.5 Field Example

A permanent AG fault occurred on line L2 in the system of Figure 11. The line was tripped and reclosed from the A2 breaker. Shortly after a line current differential relay protecting the L1 line misoperated. Note that this installation used line current differential re-lays fed with externally summated currents.

Figure 11 shows traces of the phase A currents at both ends of the L1 line. The remote end current is not distorted. The local current is heavily distorted and suspicious. Detail analysis reveals that the A1 and A2 breakers carried about 22kA of fault current, or 22kA/0.8kA = 27.5 times rated when A2 closed onto the fault. The CTs saturated quickly due to a combination of large ac current, remnant flux due to the original fault, and dc off-set. The through current in the L1 circuit was only 1.36kA. Relatively minor errors of the CTs carrying 22kA augmented considerably the true "1.36kA reverse" signal causing a false operation.

The remote end relay measured 1.36kA $\angle$ -20° (correct) while the local relay measured 1.77kA $\angle$-112° (incorrect, due to CT saturation).

As a result, the differential signal appeared to be 2.19kA. The restraining signal calculated by the relays was 1.73kA (assuming a pickup of 0.16kA and a slope setting of 50%). The operating (differential) signal was far above the restraining signal, hence the spurious trip.

Should the L1 relay at the A terminal be deployed in a dual-breaker manner, and measured the A1 and A2 current separately, it would apply the restraint of:

0.16kA + 0.5*(max(23.3kA,21.9kA,1.36kA)) = 11.8kA.

The above restraint is several times higher than the operating signal resulting in no operating for this external fault case.

8. Phase Comparison Solution

As explained in section 5, phase comparison principle would face security problems when fed from externally summated currents in dual-breaker applications. In order to maintain the excellent immunity to CT saturation of the original ("single-breaker") phase comparison principle, one needs to process the two currents individually and use both the phase and magnitude information to detect the through fault condition.

The dual breaker logic consolidates two pieces of information: fault detector flags signaling the rough current levels, and the "phase" pulses signaling current direction [8].

The fault detector flags (Fault Detector Low and Fault Detector High) are OR-ed between the two breakers (breakers 1 and 2):

$$FDL = FDL_1 \ OR \ FDL_2, \ FDH = FDH_1 \ OR \ FDH_2 \quad (13)$$

The rationale behind it is that regardless which breaker, or both carry a current; the elevated current condition (FDL) shall be declared to signal permission or blocking as per the scheme type, and fault location; similarly with the trip supervision condition (FDH).

It is the "pulse" combination logic that ensures security and dependability of the 87PC function. With this respect a distinction must be made between tripping and blocking schemes.

For tripping (permissive) phase comparison schemes, a positive polarity is declared for the terminal if one breaker displays positive polarity when its FDL flag is set, while the other breaker either does not show the negative polarity or its FDL flag is dropped out (Figure 12a). This is similar to a Hybrid POTT scheme when a given terminal sends a per-missive signal unless is restrained locally by a reverse fault condition. Note that this logic displays the following desirable features:

- Under through fault conditions, when both currents are elevated and out of phase, the positive pulses in one breaker get "erased" by the negative pulses in the other breaker.
- Under reverse or forward fault with one breaker opened or its current below the lower fault detector, the logic behaves as for a single breaker. The elevated current in the closed breaker drives the response of the scheme. In this way a small out-feed can be tolerated and will not impair dependability of the scheme.
- Under forward fault with both breakers closed and both currents above the fault detection level, the two-breaker logic effectively creates a coincidence pulse out of the two individual pulses (logical AND). This corresponds to a multi-terminal phase comparison where all individual current pulses are AND-ed before feeding the trip integrators.

The above logic is used for keying in permissive schemes, and regardless of the scheme type for derivation of local pulses sent to the trip integrators of the phase comparison relay.

Transmission logic for the blocking logic follows a different reasoning (Figure 12b). Here, a blocking action must be established if any of the two breakers sees a reverse direction. It must be kept in mind that the positive and negative pulses do not necessarily complement each other, and therefore one must not substitute the "not positive polarity" by "negative polarity".

Figure 13 shows a sample response of the permissive logic to a through fault condition at a two-breaker terminal. The terminal does not produce permissive pulses and inhibits as expected.

Figure 14 shows a case of an internal fault with strong feed from both the breakers.

More information on modern implementations of the phase comparison principle, including dual-breaker applications and the CT saturation issue, can be found in [8].

9. Stub Bus Protection and Issues

In dual-breaker applications a line disconnect can be opened while the two breakers are closed to facilitate continuous service of other circuits. At the same time the line may be energized from the other end or ends, to service tapped loads or transmit power between the other two line terminals (Figure 15).

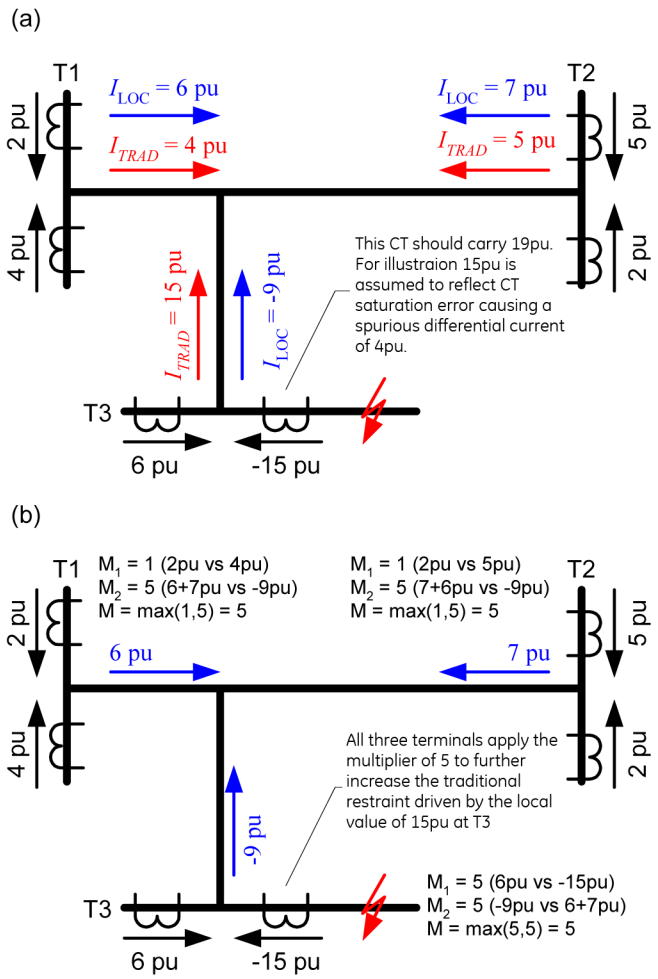

Figure 10.
An example of calculating the restraints (a) and multipliers for CT saturation algorithm (b).

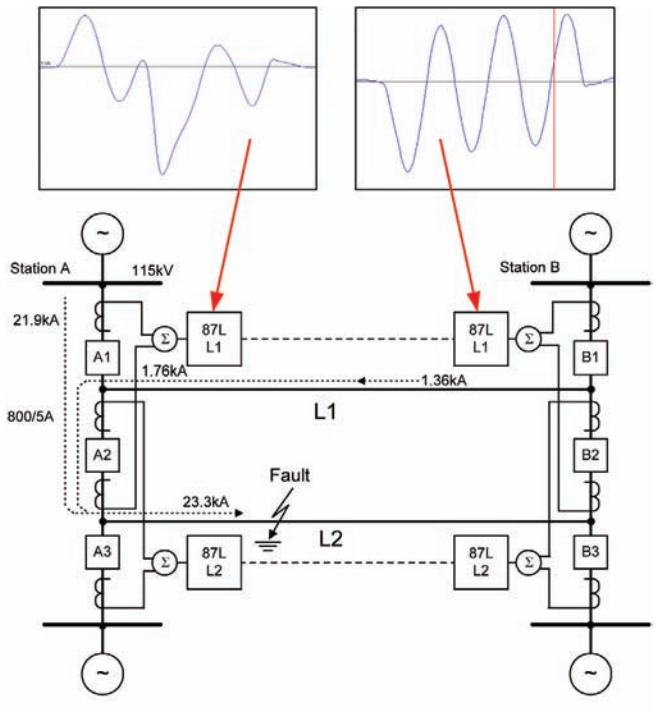

Figure 11.
System configuration for the presented filed case.

Under such circumstances the following needs to be assured:

- The stub bus zone between the two breakers and the opened disconnect is properly protected. In single-breaker application a simple overcurrent function supervised with the "disconnect opened" signal is sufficient. In dual-breaker applications such simple solution would face security problems under through fault conditions and saturated CTs as explained in section 5. Either a differential-type stub bus protection is implemented with the use of proper restraint to counterbalance the impact of saturated CTs, or the supervisory logic presented in section 6 is adopted for trip-ping.
- When tripping on stub bus faults, no DTT is to be sent to the remote end(s) as they are already isolated from the fault by the opened disconnect switch. Upon failure of one of the breakers, no BF trip is to be sent to the remote ends either.
- A fault in the stub bus zone must not result in tripping the remote line terminals. Solutions to this requirement depend on the applied protection principle, as explained below.
- Permissive directional comparison schemes typically do not have a problem. A permanent permission is keyed under the circumstances (disconnect opened while the breakers are closed); an echo scheme is used; or an overreaching zone 1 is applied at the remote end under the circumstances. In three-terminal applications or with tapped loads, it may happen that the remote end will "see" the fault in the stub bus zone despite the opened disconnect (Figure 16). This creates security problems if permanent permission or an echo scheme is used. If the fault current closes through the third line terminal, no permission will be sent from that terminal. But if the line closes via an unmonitored tapped load, the problem remains. Avoiding too sensitive overreaching functions at the remote end solves the problem.
- Under the circumstances blocking directional comparison schemes are practically equivalent to permissive schemes with permanent permission or echo as described above. Making sure the overreaching forward looking fault detectors never pickup for faults in the stub bus zone soles the problem.
- With the respect of the stub bus protection and application phase comparison relays can be dealt with as the same way as direction comparison schemes.
- Line current differential schemes require the relay under the stub bus condition to transmit zero currents regardless of its actual measurements. In this way under the stub bus fault, the 87L function will not trip the line at the remote terminal(s).

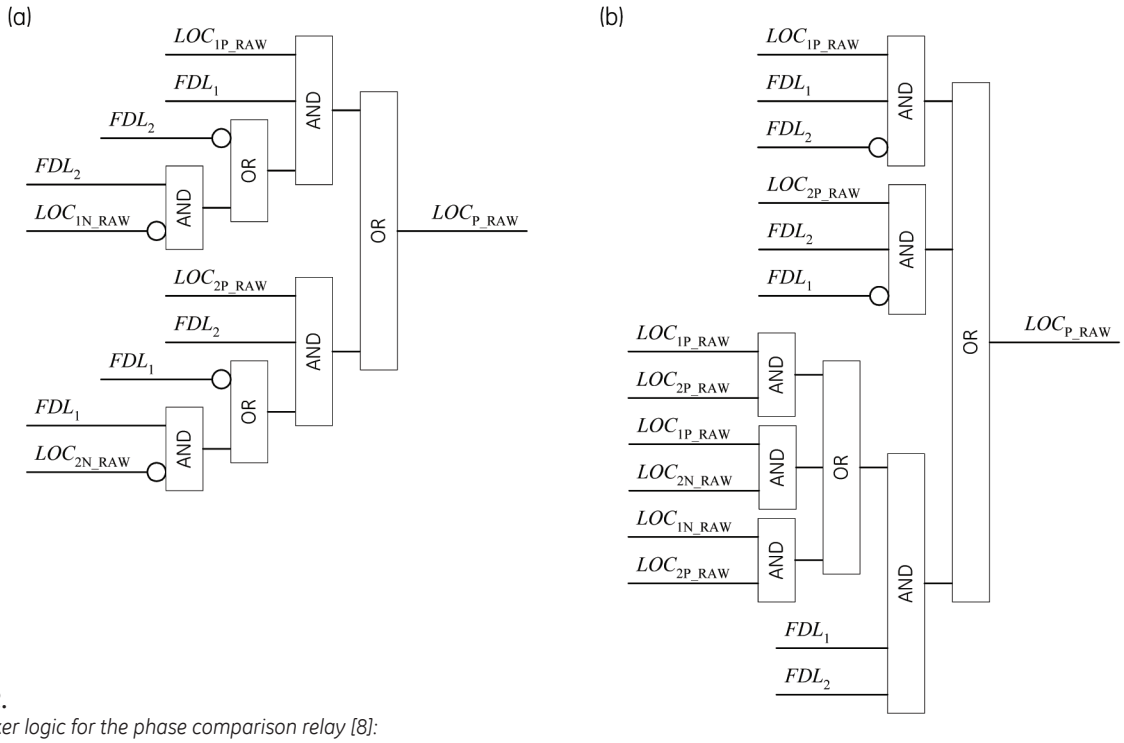

Figure 12.
Dual-breaker logic for the phase comparison relay [8]: Permissive (a) and blocking (b) transmit schemes.

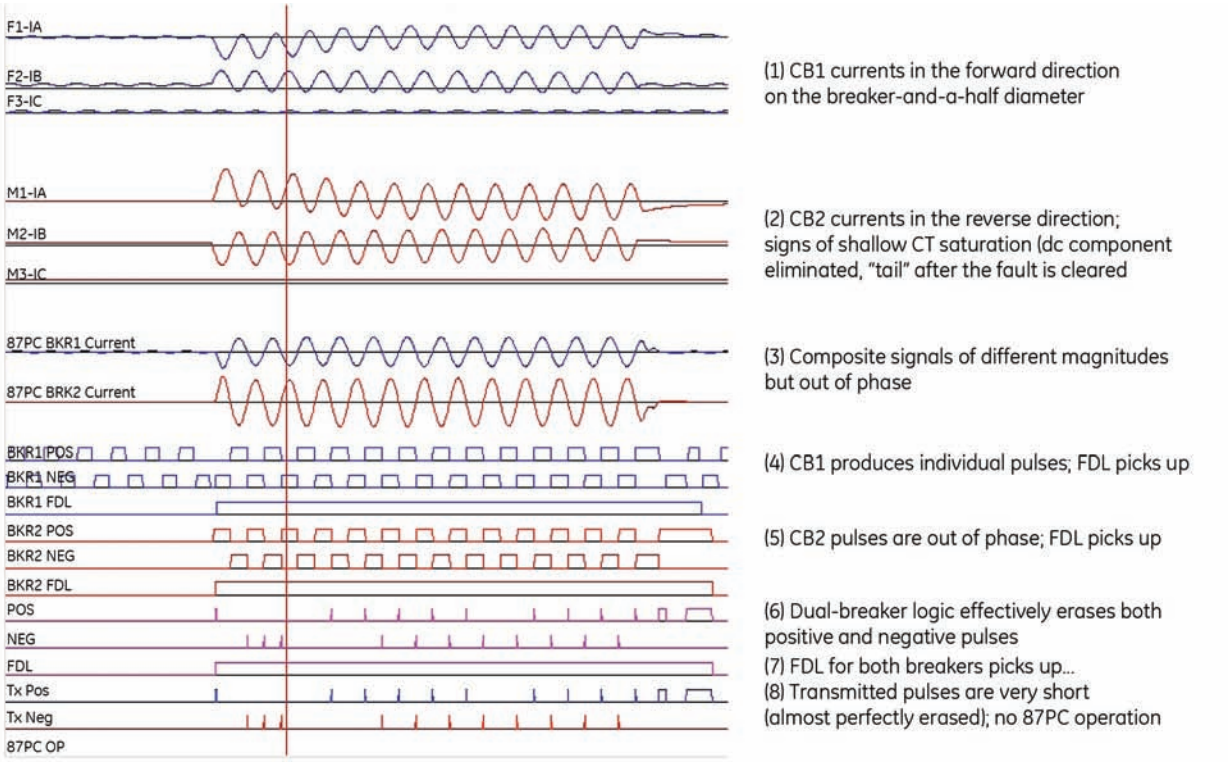

Figure 13.
Illustration of the dual-breaker logic: permissive, dual-comparison scheme, through fault condition (relay [3] COMTRADE record).

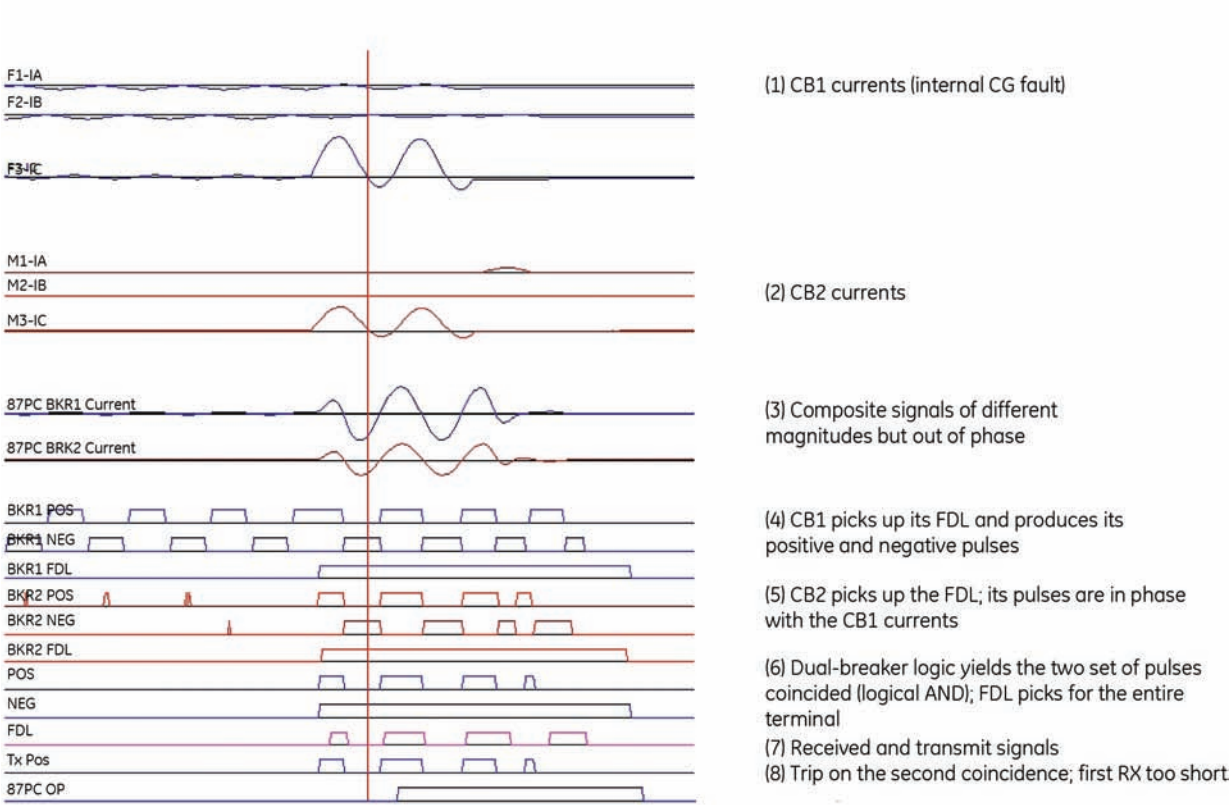

Figure 14.
Illustration of the dual-breaker logic: permissive single-comparison scheme, internal fault condition (relay [3] COMTRADE record).

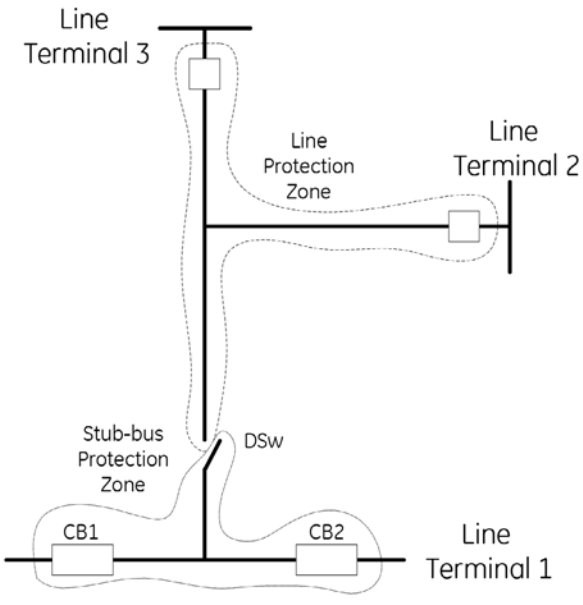

Figure 15.
Stub bus situation (three-terminal line).

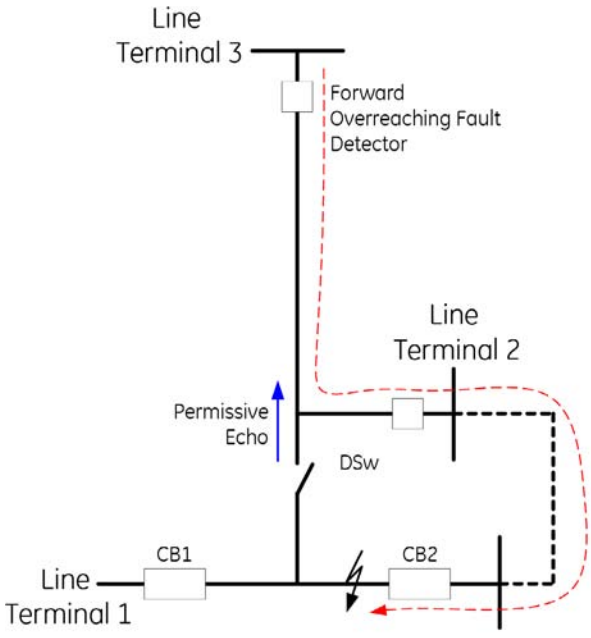

Figure 16.
Example of fault detectors too sensitive and causing problems under remote stub bus faults.

10. Conclusions

This paper presents practical application solutions for protection of lines in dual breaker applications.

Integration of breaker failure and autoreclose is discussed first.

Next a problem of stability under CT saturation when using externally summated cur-rents for protection is described.

A simple supervisory logic that could be implemented on modern line relays is presented to ensure security under CT saturation during through faults on the breaker-and-a-half or ring-bus diameter.

A novel line current differential system is described suitable not only for dual-breaker configurations, but also for applications with up to four local inputs at each of the up to three terminals of the line. The solution is designed to produce correct restraining signal as per the principle of differential protection without sending all the raw local currents between all terminals of the line.

Phase comparison algorithm addressing the security concern related to CT saturation in dual-breaker applications is also presented.

Finally notes are included on stub bus protection as related to dual-breaker applications.

Modern multi input multifunction line protection relays allow more sophisticated applications on dual-breaker line terminals.

11. References

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[3] GE Publication GEK-106412A, 2005, L60 Phase Comparison Relay, Instruction Manual.

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[8] B.Kasztenny, I.Voloh, E.A.Udren, "Rebirth of the Phase Comparison Line Protection Principle", in Proc. of the 59th Annual Conference for Protective Relay Engineers, April 4-6, 2006, College Station, Texas.