GE Vernova

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5th Generation
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CHAPTER 1

INTRODUCTION

1.1 CHAPTER OVERVIEW

This chapter provides some general information about the technical manual and an introduction to the device(s) described in this technical manual.

This chapter contains the following sections:

Chapter Overview 2
Foreword 3
Product Scope 5
Features and Functions 8
Logic Diagrams 10
Compliance 12
Functional Overview 13

1.2 FOREWORD

This technical manual provides a functional and technical description of GE Vernova's 5th Generation transformer protection IED, as well as a comprehensive set of instructions for using the device. The level at which this manual is written assumes that you are already familiar with protection engineering and have experience in this discipline. The description of principles and theory is limited to that which is necessary to understand the product. For further details on general protection engineering theory, we refer you to GE Vernova's publication, Protection and Automation Application Guide, which is available online or from our Contact Centre.

We have attempted to make this manual as accurate, comprehensive and user-friendly as possible. However we cannot guarantee that it is free from errors. Nor can we state that it cannot be improved. We would therefore be very pleased to hear from you if you discover any errors, or have any suggestions for improvement. Our policy is to provide the information necessary to help you safely specify, engineer, install, commission, maintain, and eventually dispose of this product. We consider that this manual provides the necessary information, but if you consider that more details are needed, please contact us.

All feedback should be sent to our contact centre via:

contact.centre@ge.com

1.2.1 TARGET AUDIENCE

This manual is aimed towards all professionals charged with installing, commissioning, maintaining, troubleshooting, or operating any of the products within the specified product range. This includes installation and commissioning personnel as well as engineers who will be responsible for operating the product.

The level at which this manual is written assumes that installation and commissioning engineers have knowledge of handling electronic equipment. Also, system and protection engineers have a thorough knowledge of protection systems and associated equipment.

1.2.2 TYPOGRAPHICAL CONVENTIONS

The following typographical conventions are used throughout this manual.

- The names for special keys appear in capital letters.
  For example: ENTER
- When describing software applications, menu items, buttons, labels etc as they appear on the screen are written in bold type.
  For example: Select **Save** from the file menu.
- Filenames and paths use the courier font
  For example: `Example\File.text`
- Special terminology is written with leading capitals
  For example: Sensitive Earth Fault
- If reference is made to the IED's internal settings and signals database, the menu group heading (column) text is written in upper case italics
  For example: The *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the setting cells and DDB signals are written in bold italics
  For example: The ***Language*** cell in the *SYSTEM DATA* column
- If reference is made to the IED's internal settings and signals database, the value of a cell's content is written in the Courier font
  For example: The ***Language*** cell in the *SYSTEM DATA* column contains the value `English`

1.2.3 NOMENCLATURE

Due to the technical nature of this manual, many special terms, abbreviations and acronyms are used throughout the manual. Some of these terms are well-known industry-specific terms while others may be special product-specific terms used by GE Vernova. The first instance of any acronym or term used in a particular chapter is explained. In addition, a separate glossary is available on the GE Vernova website, or from the GE Vernova contact centre.

We would like to highlight the following changes of nomenclature however:

- The word 'relay' is no longer used to describe the device itself. Instead, the device is referred to as the 'IED' (Intelligent Electronic Device), the 'device', or the 'product'. The word 'relay' is used purely to describe the electromechanical components within the device, i.e. the output relays.
- British English is used throughout this manual.
- The British term 'Earth' is used in favour of the American term 'Ground'.

1.2.4 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

1.3 PRODUCT SCOPE

The MiCOM 5th Generation range of devices preserve transformer service life by offering fast protection for transformer faults. Hosted on an advanced IED platform, the P64 products incorporate Current Differential, Restricted Earth Fault (REF),Thermal, and Overfluxing protection, plus backup protection for uncleared external faults. Further, the P64 devices provide a range of transformer condition monitoring functions such as Through-fault monitoring, loss of life statistics, RTD and CLIO protection functionality.

All devices also provide a comprehensive range of additional features to aid with power system diagnosis and fault analysis.

The P64 can be ordered in 40/60/80TE cases with several different digital input/output options also offered.

Model variants cover two and three winding power transformers, with up to five sets of 3-phase CT inputs. Backup overcurrent protection can be directionalised, if you select the optional 3-phase VT input.

The P64 range consists of three models; the P642, P643, and P645.

- The P642 provides 8 on-board CTs to support two-winding 3-phase power transformers and 1or 2 single-phase voltage transformers to support directionalisation and a range of voltage-related functions.
- The P643 provides 12 on-board CTs to support three-winding 3-phase power transformers, a single-phase voltage transformer and an optional three-phase voltage transformer to support directionalisation and a range of voltage-related functions including undervoltage, overvoltage and residual overvoltage protection.
- The P645 provides 18 on-board CTs to support three-winding 3-phase power transformers and other applications needing 5 sets of 3-phase current inputs, a single-phase voltage transformer and an optional three-phase voltage transformer to support directionalisation and a range of voltage-related functions including undervoltage, overvoltage and residual overvoltage protection.

The difference in model variants are summarised below:

Feature/Variant	P642	P643	P645
Case	40/60/80TE	60/80TE	60/80TE
Number of CT inputs	8 (6 Bias, 2 EF)	12 (9 bias, 3EF)	18 (15 Bias, 3EF)
Number of VT inputs	1 or 2	1 or 4	1 or 4
Number of bias inputs (3-phase CT sets)	2	3	5
Optically coupled digital inputs	8 - 32	16 - 48	16 - 48
Standard relay output contacts	8 - 32	16 - 32	16 - 32
Function keys	No	10	10
Undervoltage/Overvoltage/Residual voltage protection	No	Yes	Yes
Underfrequency/Overfrequency protection	No	Yes	Yes
Overfluxing protection	1-phase only	1-phase + 3-phase	1-phase + 3-phase
Programmable LEDs	23 tri-colour	23 tri-colour	23 tri-colour

1.3.1 PRODUCT VERSIONS

Since software version 2, the evolution of the P64 product family has followed two paths as shown below:

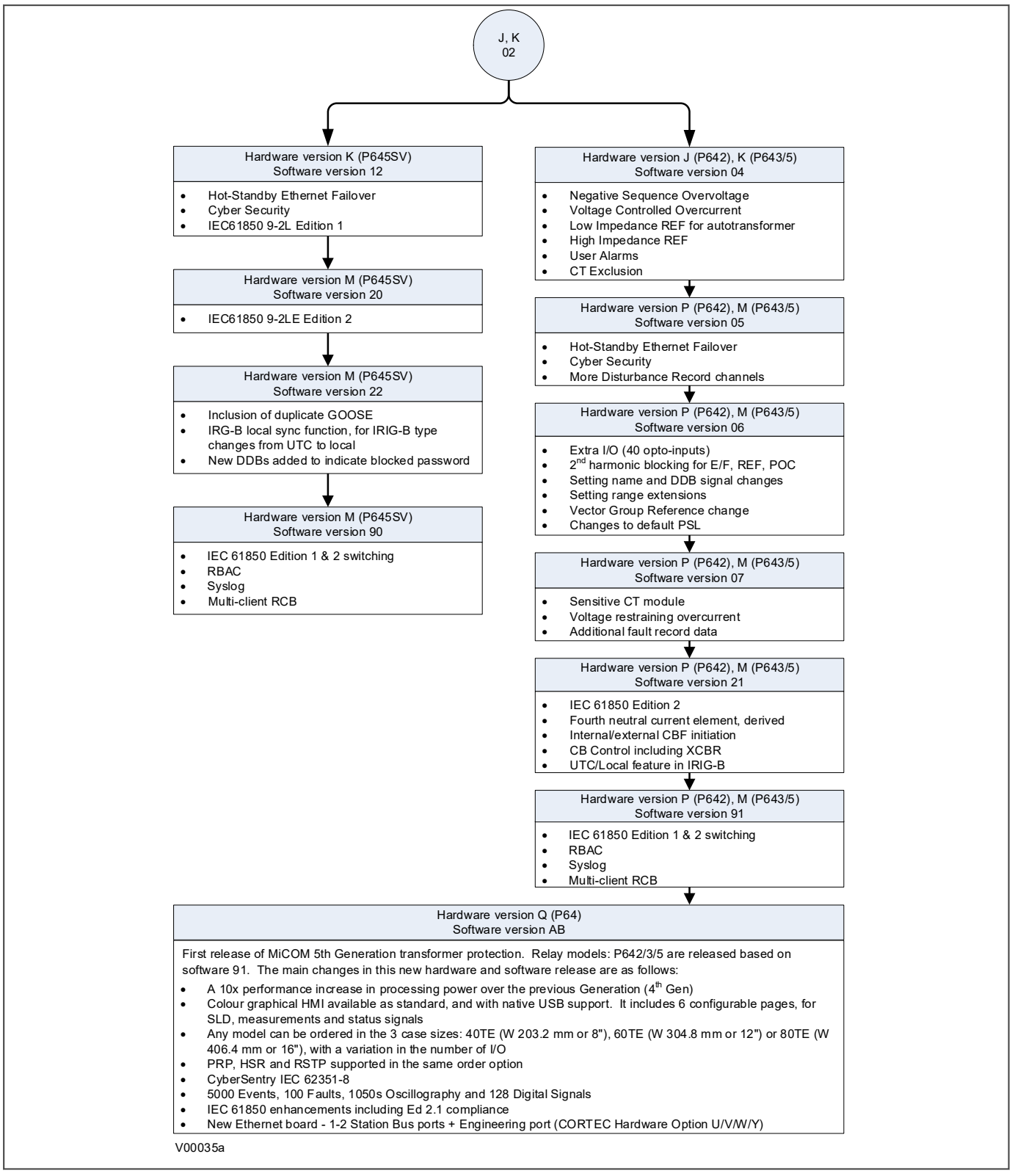


Figure 1: P64x version evolution

1.3.2 ORDERING OPTIONS

All current models and variants for this product are defined in an interactive spreadsheet called the Cortec. This is available on the company website.

Alternatively, you can obtain it via the Contact Centre at:

contact.centre@ge.com

A copy of the Cortec is also supplied as a static table in the Appendices of this document. However, it should only be used for guidance as it provides a snapshot of the interactive data taken at the time of publication.

This technical manual is applicable to the product version A<PlatformSoftwareVersion>

1.4 FEATURES AND FUNCTIONS

1.4.1 PROTECTION FUNCTIONS

The P64 range of devices provides the following protection functions:

ANSI	IEC 61850	Protection Function	P642	P643	P645
87T	LzdPDIF	Transformer biased differential protection	•	•	•
64	RefPDIF	Low Impedance and High Impedance Restricted Earth Fault protection	2	3	3
49	ThmPTTR	Thermal Overload (3 stages)	•	•	•
32	PdpPDOP/PDUP	Phase Directional Power (4 stages)	•	•	•
24	PVPH	Single-phase and three-phase V/Hz Overfluxing protection (4 stages)	1	1 (2)	1 (2)
LoL		Loss of Life	•	•	•
Thru		Through-fault monitoring	•	•	•
RTD	RtfPTTR	RTDs x 10 PT100 temperature probes	(•)	(•)	(•)
CLIO	PTUC	Current Loop transducer I/O (4 input/4 output)	(•)	(•)	(•)
50	OcpPTOC	Definite time overcurrent protection (4 stages per winding)	•	•	•
50N	EfdPTOC	Neutral/Ground Definite time overcurrent protection (4 stages per winding)	•	•	•
51	OcpPTOC	IDMT overcurrent protection (2 stages per winding)	•	•	•
51N	EfdPTOC	Neutral/Ground IDMT overcurrent protection (2 stages per winding)	•	•	•
46	NgcPTOC	Negative sequence overcurrent (4 stages per winding)	•	•	•
67	OcpPTOC	Directional Phase Overcurrent protection (4 stages per winding)	•	•	•
67N	EfdPTOC	Directional earth fault overcurrent protection (4 stages per winding)	•	•	•
50BF	RBRF	CB Failure (Breaker Fail) protection (2 stages per winding)	2	3	5
27	VtpPhsPTUV	Undervoltage protection (2 stages)		(•)	(•)
59	VtpPhsPTOV	Overvoltage protection (2 stages)		(•)	(•)
59N	VtpResPTOV	Residual Overvoltage protection (2 stages)		(•)	(•)
47	NgvPTOV	Negative sequence overvoltage protection (1 stage)	(•)	(•)	(•)
81U	FrqPTUF	Underfrequency protection (4 stages)		(•)	(•)
81O	FrqPTOF	Overfrequency protection (2 stages)		(•)	(•)

Note:
If item is enclosed in brackets, this indicates that the feature is an ordering option.

1.4.2 CONTROL FUNCTIONS

Feature	IEC 61850	ANSI
Watchdog contacts		
Read-only mode		
NERC compliant cyber-security		
Function keys (up to 10)	FnkGGIO	

Feature	IEC 61850	ANSI
Programmable LEDs (up to 23)	LedGGIO	
Programmable hotkeys (2)		
Programmable allocation of digital inputs and outputs		
Fully customizable menu texts		
Circuit breaker control, status & condition monitoring	XCBR	52
Trip circuit and coil supervision		
Control inputs	PloGGIO1	
Power-up diagnostics and continuous self-monitoring		
Dual rated 1A and 5A CT inputs		
Alternative setting groups (4)		
Graphical programmable scheme logic (PSL)		

1.4.3 MEASUREMENT FUNCTIONS

Measurement Function	IEC 61850	ANSI
Measurement of all instantaneous & integrated values (Exact range of measurements depend on the device model)		MET
Disturbance recorder for waveform capture – specified in samples per cycle	RDRE	DFR
Fault Records		
Maintenance Records		
Event Records/Event logging		Event records
Time Stamping of Opto-inputs	Yes	Yes

1.4.4 COMMUNICATION FUNCTIONS

The device offers the following communication functions:

Feature	ANSI
NERC compliant cyber-security	
Front USB communication port for configuration	
Rear serial RS485 communication port for SCADA control--Courier/DNP 3.0/IEC 60870-5-103 protocol selectable in settings	16S
Rear serial FO communication ports for SCADA control (optional) - Courier/DNP 3.0/IEC 60870-5-103 protocol selectable in settings	16S
Ethernet communication (optional)--IEC 61850	16E
Redundant Ethernet communication (optional)--IEC 61850	16E
Rear Ethernet engineering port for configuration	16E
SNMP	16E
IRIG-B modulated and unmodulated time synchronisation (optional)	CLK
IEEE 1588 PTP	

1.5 LOGIC DIAGRAMS

This technical manual contains many logic diagrams, which should help to explain the functionality of the device. Although this manual has been designed to be as specific as possible to the chosen product, it may contain diagrams, which have elements applicable to other products. If this is the case, a qualifying note will accompany the relevant part.

The logic diagrams follow a convention for the elements used, using defined colours and shapes. A key to this convention is provided below. We recommend viewing the logic diagrams in colour rather than in black and white. The electronic version of the technical manual is in colour, but the printed version may not be. If you need coloured diagrams, they can be provided on request by calling the contact centre and quoting the diagram number.

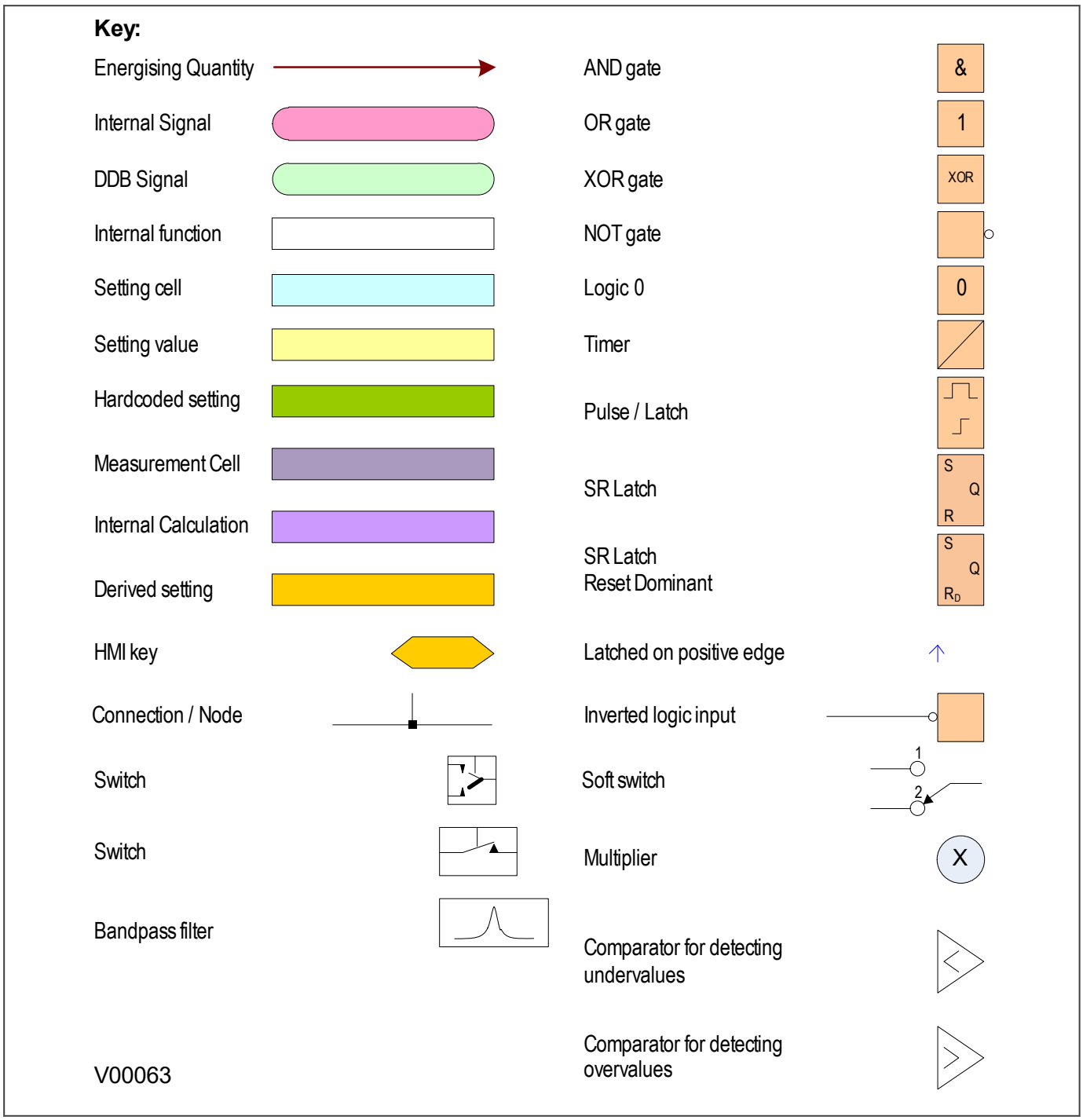
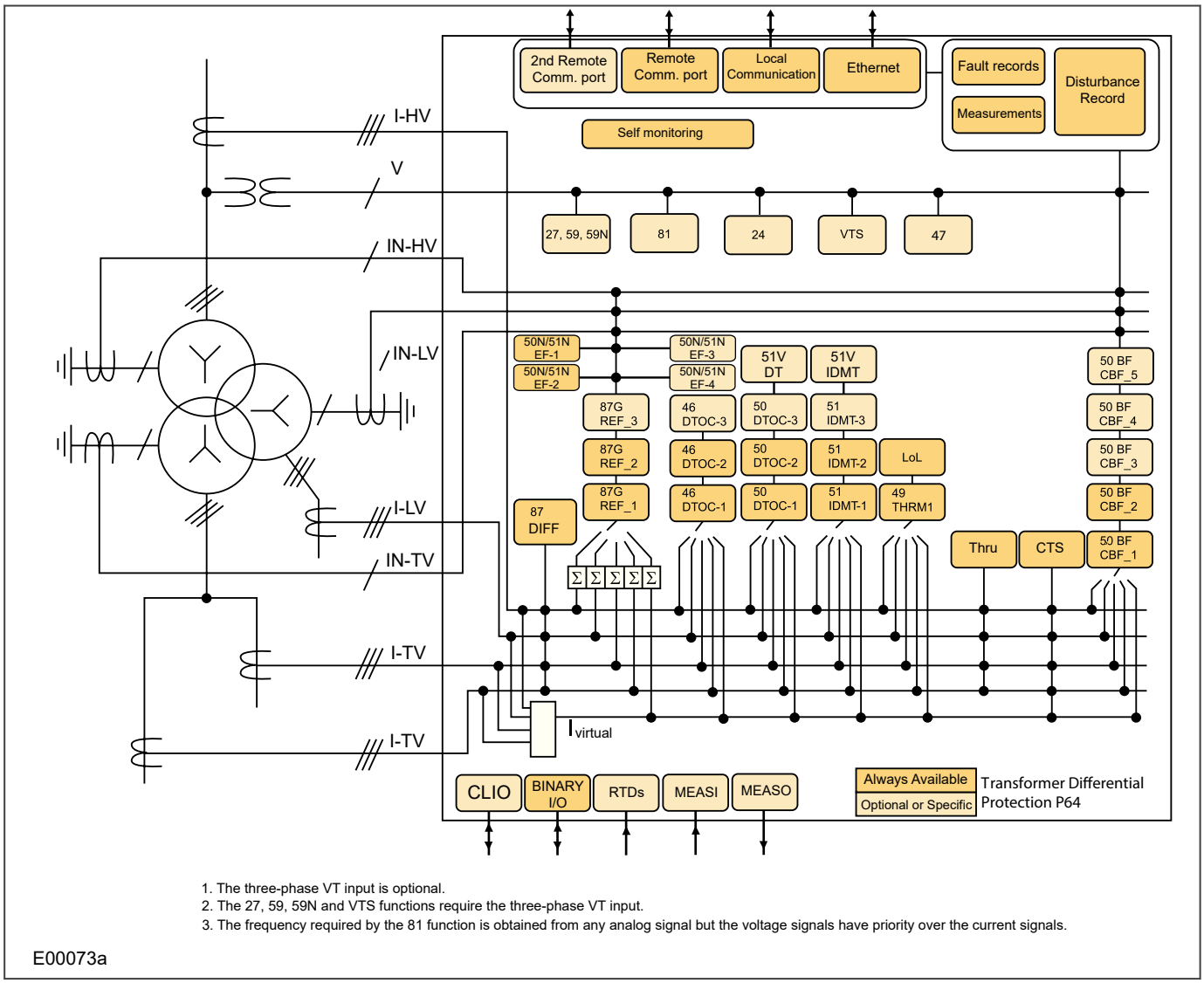


Figure 2: Key to logic diagrams

1.6 COMPLIANCE

The device has undergone a range of extensive testing and certification processes to ensure and prove compatibility with all target markets. A detailed description of these criteria can be found in the Technical Specifications chapter.

1.7 FUNCTIONAL OVERVIEW



1. The three-phase VT input is optional.
2. The 27, 59, 59N and VTS functions require the three-phase VT input.
3. The frequency required by the 81 function is obtained from any analog signal but the voltage signals have priority over the current signals.

E00073a

Figure 3: Functional overview

CHAPTER 2

SAFETY INFORMATION

2.1 CHAPTER OVERVIEW

This chapter provides information about the safe handling of the equipment. The equipment must be properly installed and handled in order to maintain it in a safe condition and to keep personnel safe at all times. You must be familiar with information contained in this chapter before unpacking, installing, commissioning, or servicing the equipment.

This chapter contains the following sections:

Chapter Overview 16

Health and Safety 17

Symbols 18

Installation, Commissioning and Servicing 19

Decommissioning and Disposal 25

Regulatory Compliance 26

2.2 HEALTH AND SAFETY

Personnel associated with the equipment must be familiar with the contents of this Safety Information.

When electrical equipment is in operation, dangerous voltages are present in certain parts of the equipment. Improper use of the equipment and failure to observe warning notices will endanger personnel.

Only qualified personnel may work on or operate the equipment. Qualified personnel are individuals who are:

- familiar with the installation, commissioning, and operation of the equipment and the system to which it is being connected.
- familiar with accepted safety engineering practises and are authorised to energise and de-energise equipment in the correct manner.
- trained in the care and use of safety apparatus in accordance with safety engineering practises
- trained in emergency procedures (first aid).

The documentation provides instructions for installing, commissioning and operating the equipment. It cannot, however cover all conceivable circumstances. In the event of questions or problems, do not take any action without proper authorisation. Please contact your local sales office and request the necessary information.

2.3 SYMBOLS

Throughout this manual you will come across the following symbols. You will also see these symbols on parts of the equipment.

Caution:
Refer to equipment documentation. Failure to do so could result in damage to the equipment

Warning:
Risk of electric shock

Warning:
Risk of damage to eyesight

Earth terminal. *Note: This symbol may also be used for a protective conductor (earth) terminal if that terminal is part of a terminal block or sub-assembly.*

Protective conductor (earth) terminal

Instructions on disposal requirements

Note:
The term 'Earth' used in this manual is the direct equivalent of the North American term 'Ground'.

2.4 INSTALLATION, COMMISSIONING AND SERVICING

2.4.1 LIFTING HAZARDS

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively

Plan carefully, identify any possible hazards and determine how best to move the product. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment (PPE) to reduce the risk of injury.

2.4.2 ELECTRICAL HAZARDS

Caution:
All personnel involved in installing, commissioning, or servicing this equipment must be familiar with the correct working procedures.

Caution:
Consult the equipment documentation before installing, commissioning, or servicing the equipment.

Caution:
Always use the equipment as specified. Failure to do so will jeopardise the protection provided by the equipment.

Warning:
Removal of equipment panels or covers may expose hazardous live parts. Do not touch until the electrical power is removed. Take care when there is unlocked access to the rear of the equipment.

Warning:
Isolate the equipment before working on the terminal strips.

Warning:
Use a suitable protective barrier for areas with restricted space, where there is a risk of electric shock due to exposed terminals.

Caution:
Disconnect power before disassembling. Disassembly of the equipment may expose sensitive electronic circuitry. Take suitable precautions against electrostatic voltage discharge (ESD) to avoid damage to the equipment.

Warning:
NEVER look into optical fibres or optical output connections. Always use optical power meters to determine operation or signal level.

Warning:
Testing may leave capacitors charged to dangerous voltage levels. Discharge capacitors by reducing test voltages to zero before disconnecting test leads.

Caution:
Operate the equipment within the specified electrical and environmental limits.

Caution:
Before cleaning the equipment, ensure that no connections are energised. Use a lint free cloth dampened with clean water.

Note:
Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

2.4.3 UL/CSA/CUL REQUIREMENTS

The information in this section is applicable only to equipment carrying UL/CSA/CUL markings.

Caution:
Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).

Caution:
To maintain compliance with UL and CSA/CUL, install the equipment using UL/CSA-recognised parts for: cables, protective fuses, fuse holders and circuit breakers, insulation crimp terminals, and replacement internal batteries.

2.4.4 FUSING REQUIREMENTS

Caution:
Where UL/CSA listing of the equipment is required for external fuse protection, a UL or CSA Listed fuse must be used for the auxiliary supply. The listed protective fuse type is: Class J time delay fuse, with a maximum current rating of 15 A and a minimum DC rating of 250 V dc (for example type AJT15).

Caution:
Where UL/CSA listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum dc rating of 250 V dc may be used for the auxiliary supply (for example Red Spot type NIT or TIA).
For P50 models, use a 1A maximum T-type fuse.
For P60 models, use a 4A maximum T-type fuse.

Caution:
Digital input circuits should be protected by a high rupture capacity NIT or TIA fuse with maximum rating of 16 A. for safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

Caution:
CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages

2.4.5 EQUIPMENT CONNECTIONS

Warning:
Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.

Caution:
Tighten M4 clamping screws of heavy duty terminal block connectors to a nominal torque of 1.3 Nm.
Tighten captive screws of terminal blocks to 0.5 Nm minimum and 0.6 Nm maximum.

Caution:
Always use insulated crimp terminations for voltage and current connections.

Caution:
Always use the correct crimp terminal and tool according to the wire size.

Caution:
Watchdog (self-monitoring) contacts are provided to indicate the health of the device on some products. We strongly recommend that you hard wire these contacts into the substation's automation system, for alarm purposes.

2.4.6 PROTECTION CLASS 1 EQUIPMENT REQUIREMENTS

Caution:
Earth the equipment with the supplied PCT (Protective Conductor Terminal).

Caution:
Do not remove the PCT.

Caution:
The PCT is sometimes used to terminate cable screens. Always check the PCT's integrity after adding or removing such earth connections.

Caution:
Use a locknut or similar mechanism to ensure the integrity of stud-connected PCTs.

Caution:
The recommended minimum PCT wire size is 2.5 mm² for countries whose mains supply is 230 V (e.g. Europe) and 3.3 mm² for countries whose mains supply is 110 V (e.g. North America). This may be superseded by local or country wiring regulations. For P60 products, the recommended minimum PCT wire size is 6 mm². See product documentation for details.

Caution:
The PCT connection must have low-inductance and be as short as possible.

Caution:
All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should be earthed, or connected to a common grouped potential.

2.4.7 PRE-ENERGISATION CHECKLIST

Caution:
Check voltage rating/polarity (rating label/equipment documentation).

Caution:
Check CT circuit rating (rating label) and integrity of connections.

Caution:
Check protective fuse or miniature circuit breaker (MCB) rating.

Caution:
Check integrity of the PCT connection.

Caution:
Check voltage and current rating of external wiring, ensuring it is appropriate for the application.

2.4.8 PERIPHERAL CIRCUITRY

Warning:
Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Short the secondary of the line CT before opening any connections to it.

Note:
For most GE Vernova equipment with ring-terminal connections, the threaded terminal block for current transformer termination is automatically shorted if the module is removed. Therefore external shorting of the CTs may not be required. Check the equipment documentation and wiring diagrams first to see if this applies.

Caution:
Where external components such as resistors or voltage dependent resistors (VDRs) are used, these may present a risk of electric shock or burns if touched.

Warning:
Take extreme care when using external test blocks and test plugs such as the MMLG, MMLB and P990, as hazardous voltages may be exposed. Ensure that CT shorting links are in place before removing test plugs, to avoid potentially lethal voltages.

Warning:
Data communication cables with accessible screens and/or screen conductors, (including optical fibre cables with metallic elements), may create an electric shock hazard in a sub-station environment if both ends of the cable screen are not connected to the same equipotential bonded earthing system.

To reduce the risk of electric shock due to transferred potential hazards:

i. The installation shall include all necessary protection measures to ensure that no fault currents can flow in the connected cable screen conductor.

ii. The connected cable shall have its screen conductor connected to the protective conductor terminal (PCT) of the connected equipment at both ends. This connection may be inherent in the connectors provided on the equipment but, if there is any doubt, this must be confirmed by a continuity test.

iii. The protective conductor terminal (PCT) of each piece of connected equipment shall be connected directly to the same equipotential bonded earthing system.

iv. If, for any reason, both ends of the cable screen are not connected to the same equipotential bonded earth system, precautions must be taken to ensure that such screen connections are made safe before work is done to, or in proximity to, any such cables.

v. No equipment shall be connected to any download or maintenance circuits or connectors of this product except temporarily and for maintenance purposes only.

vi. Equipment temporarily connected to this product for maintenance purposes shall be protectively earthed (if the temporary equipment is required to be protectively earthed), directly to the same equipotential bonded earthing system as the product.

Warning:
Small Form-factor Pluggable (SFP) modules which provide copper Ethernet connections typically do not provide any additional safety isolation. Copper Ethernet SFP modules must only be used in connector positions intended for this type of connection.

2.4.9 UPGRADING/SERVICING

Warning:
Do not insert or withdraw modules, PCBs or expansion boards from the equipment while energised, as this may result in damage to the equipment. Hazardous live voltages would also be exposed, endangering personnel.

Caution:
Internal modules and assemblies can be heavy and may have sharp edges. Take care when inserting or removing modules into or out of the IED.

2.5 DECOMMISSIONING AND DISPOSAL

Caution:
Before decommissioning, completely isolate the equipment power supplies (both poles of any dc supply). The auxiliary supply input may have capacitors in parallel, which may still be charged. To avoid electric shock, discharge the capacitors using the external terminals before decommissioning.

Caution:
Avoid incineration or disposal to water courses. Dispose of the equipment in a safe, responsible and environmentally friendly manner, and if applicable, in accordance with country-specific regulations.

2.6 REGULATORY COMPLIANCE

Compliance with the European Commission Directive on EMC and LVD is demonstrated using a technical file.

CE

2.6.1 EMC COMPLIANCE: 2014/30/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.2 LVD COMPLIANCE: 2014/35/EU

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the LVD directive.

Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

2.6.3 UL/CUL COMPLIANCE

If marked with this logo, the product is compliant with the requirements of the Canadian and USA Underwriters Laboratories.

The relevant UL file number and ID is shown on the equipment.

c UL US

2.6.4 UKCA COMPLIANCE

Compliance with the UK Directive on EMC and Safety is demonstrated using a technical file.

UK CA

2.6.5 EMC COMPLIANCE: ELECTROMAGNETIC COMPATIBILITY REGULATIONS 2016

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.6 SAFETY COMPLIANCE: ELECTRICAL EQUIPMENT (SAFETY) REGULATIONS 2016

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the Safety Regulations. Safety related information, such as the

installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

2.6.7 MOROCCO COMPLIANCE

Compliance with the Morocco Directive on EMC and Safety is demonstrated using a technical file.

2.6.8 EMC COMPLIANCE: NO. 2574-14 OF RAMADAN 1436

The product specific Declaration of Conformity (DoC) lists the relevant harmonised standard(s) or conformity assessment used to demonstrate compliance with the EMC directive.

2.6.9 SAFETY COMPLIANCE: NO. 2573-14 OF RAMADAN 1436

The product specific Declaration of Conformity (DoC) lists the relevant harmonized standard(s) or conformity assessment used to demonstrate compliance with the Safety Directive. Safety related information, such as the installation I overvoltage category, pollution degree and operating temperature ranges are specified in the Technical Data section of the relevant product documentation and/or on the product labelling.

Unless otherwise stated in the Technical Data section of the relevant product documentation, the equipment is intended for indoor use only. Where the equipment is required for use in an outdoor location, it must be mounted in a specific cabinet or housing to provide the equipment with the appropriate level of protection from the expected outdoor environment.

CHAPTER 3

HARDWARE DESIGN

3.1 CHAPTER OVERVIEW

This chapter provides information about the product's hardware design.

This chapter contains the following sections:

Chapter Overview 30
Hardware Architecture 31
Mechanical Implementation 32
Front Panel 34
Rear Panel 38
Boards and Modules 40

3.2 HARDWARE ARCHITECTURE

The main components comprising devices based on the Px4x platform are as follows:

- The housing, consisting of a front panel and connections at the rear
- The Main processor module consisting of the main CPU (Central Processing Unit), memory and an interface to the front panel HMI (Human Machine Interface)
- A selection of plug-in boards and modules with presentation at the rear for the power supply, communication functions, digital I/O, analogue inputs, and time synchronisation connectivity

All boards and modules are connected by a parallel data and address bus, which allows the processor module to send and receive information to and from the other modules as required. There is also a separate serial data bus for conveying sampled data from the input module to the CPU. These parallel and serial databuses are shown as a single interconnection module in the following figure, which shows typical modules and the flow of data between them.

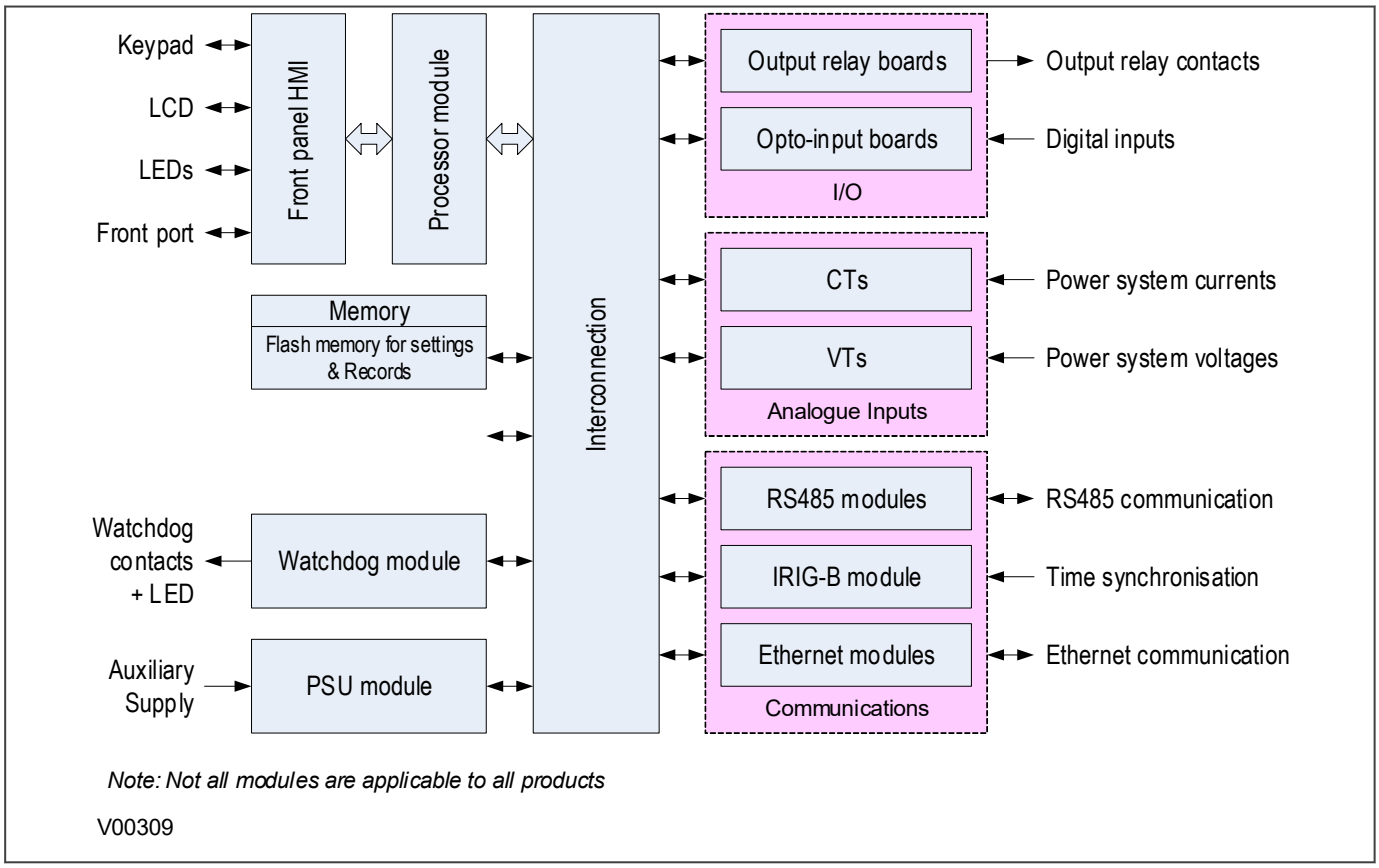


Figure 4: Hardware architecture

3.3 MECHANICAL IMPLEMENTATION

All products based on the Px4x platform have common hardware architecture. The hardware is modular and consists of the following main parts:

- Case and terminal blocks
- Boards and modules
- Front panel

The case comprises the housing metalwork and terminal blocks at the rear. The boards fasten into the terminal blocks and are connected together by a ribbon cable. This ribbon cable connects to the processor in the front panel.

The following diagram shows an exploded view of a typical product. The diagram shown does not necessarily represent exactly the product model described in this manual.

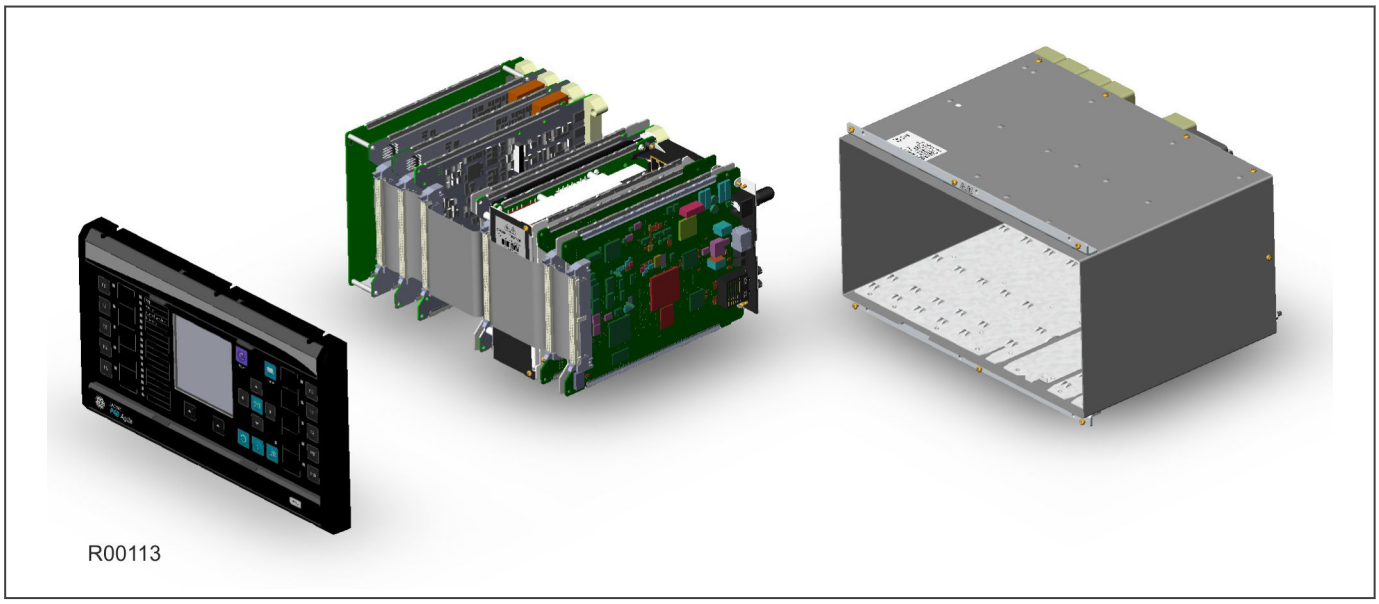


Figure 5: Exploded view of IED

3.3.1 HOUSING VARIANTS

The Px4x range of products are implemented in a range of case sizes. Case dimensions for industrial products usually follow modular measurement units based on rack sizes. These are: U for height and TE for width, where:

- 1U = 1.75 inches = 44.45 mm
- 1TE = 0.2 inches = 5.08 mm

The products are available in panel-mount or standalone versions. All products are nominally 4U high. This equates to 177.8 mm or 7 inches.

The cases are pre-finished steel with a conductive covering of aluminium and zinc. This provides good grounding at all joints, providing a low resistance path to earth that is essential for performance in the presence of external noise.

The case width depends on the product type and its hardware options. There are three different case widths for the described range of products: 40TE, 60TE and 80TE. The case dimensions and compatibility criteria are as follows:

Case width (TE)	Case width (mm)	Case width (inches)
40TE	203.2	8
60TE	304.8	12
80TE	406.4	16

3.3.2 LIST OF BOARDS

The product's hardware consists of several modules drawn from a standard range. The exact specification and number of hardware modules depends on the model number and variant. Depending on the exact model, the product in question will use a selection of the following boards.

Board	Use
Main Processor board - 40TE or smaller	Main Processor board - without support for function keys
Main Processor board - 60TE or larger	Main Processor board - with support for function keys
Power supply board - 24/54V DC	Power supply input. Accepts DC voltage between 24V and 54V
Power supply board - 48/125V DC	Power supply input. Accepts DC voltage between 48V and 125V
Power supply board - 110/250V DC	Power supply input. Accepts DC voltage between 110V and 125V
Transformer board	Contains the voltage and current transformers
Input board	Contains the A/D conversion circuitry
Input board with opto-inputs	Contains the A/D conversion circuitry + 8 digital opto-inputs
IRIG-B board - modulated input	Interface board for modulated IRIG-B timing signal
Fibre board + IRIG-B	Interface board for fibre-based RS485 connection + modulated IRIG-B
High-break output relay board	Output relay board with high breaking capacity relays
Single Ethernet, universal IRIG-B, IEEE1588, Maintenance Port	Single LC duplex Ethernet port with universal IRIG-B and IEEE1588 and 1 RJ45 Maintenance/Engineering Port
Redundant Ethernet RSTP + PRP + HSR + Failover ports, serial fibre port, universal IRIG-B	2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with IEC 60870-5-103 serial fibre ST ports with on-board universal IRIG-B and IEEE 1588 and 1 RJ45 Maintenance/engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover universal IRIG-B	2 RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B and IEEE 1588 and 1 RJ45 Maintenance/engineering port
Redundant Ethernet RSTP + PRP + HSR + Failover ports, universal IRIG-B	2 LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B and IEEE 1588 and 1 RJ45 Maintenance/engineering port
Output relay output board	Standard output relay board
RTD board	Contains 10 Resistive Temperature Device inputs
CLIO board	Contains 4 current loop inputs and 4 current loop outputs

3.4 FRONT PANEL

Depending on the exact model and chosen options, the product will be housed in either a 40TE, 60TE or 80TE case. By way of example, the following diagram shows the front panel of a typical unit. The front panels of the products based on 40TE, 60TE and 80TE cases have a lot of commonality and differ only in that the 40TE front panel does not include 10 function keys with their associated user-programmable LEDs.

Figure 6: Front panel (80TE)

The front panel consists of:

- Top and bottom compartments with hinged cover
- LCD display
- Keypad
- USB Type B port inside the bottom compartment
- Fixed function LEDs
- Function keys and LEDs (60TE and 80TE models)
- Programmable LEDs

3.4.1 FRONT PANEL COMPARTMENTS

The top compartment contains labels for the:

- Serial number
- Current and voltage ratings.

The bottom compartment contains:

- USB type B port

3.4.2 HMI PANEL

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the colour LCD display.

The colour LCD display is an active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit and back-light unit. The resolution of the 4.0” TFT-LCD is 480x480 pixels and it can display up to 16.7M colours.

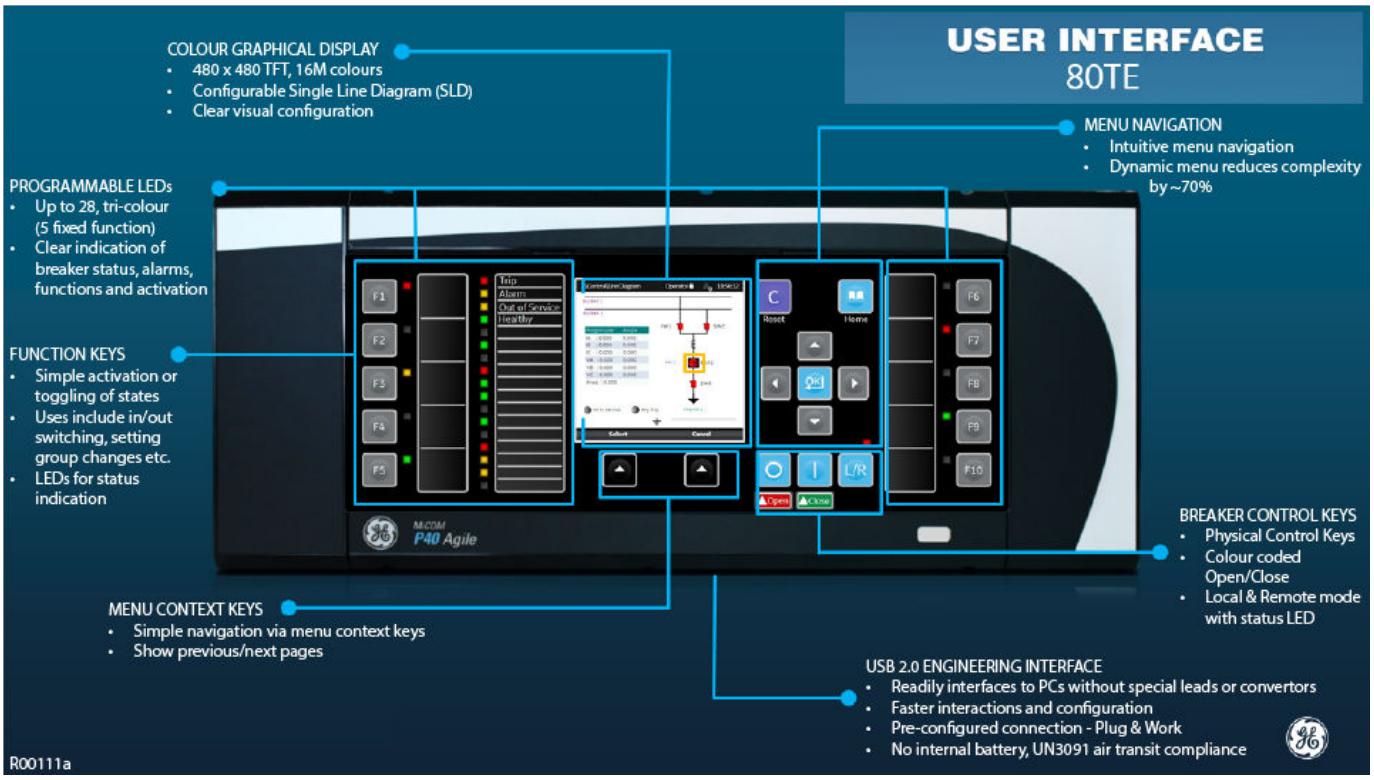
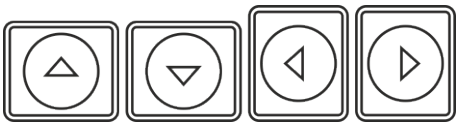
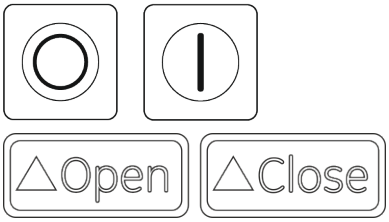


Figure 7: HMI panel

3.4.3 KEYPAD

The keypad consists of the following keys:

4 arrow keys to navigate the menus, changing values within the cell or to select the next item on the SLD (organised around the Enter key).	
An enter key for changing and executing settings. When a bottom banner menu context key label is selected, the OK key can also be used to navigate between pages.	
A clear/reset key for clearing the current setting dialogue or to navigate to the top menu.	
A home key for navigating to the default menu view.	
2 menu context keys used to navigate between pages.	

Open/Close keys (colour coded) **Note:** Colour coding is selectable via labels and configuration of PSL/ SLD.	
Local/remote key to select between local or remote modes.	

3.4.4 USB PORT

The USB port is situated inside the bottom compartment, and is used to communicate with a locally connected PC. It has two main purposes:

- To transfer settings between the PC and the device.
- For downloading firmware updates and menu text editing.

The port is intended for temporary connection during testing, installation and commissioning. It is not intended to be used for permanent SCADA communications. This port supports the Courier communication protocol only. Courier is a proprietary communication protocol to allow communication with a range of protection equipment, and between the device and the Windows-based support software package.

You can connect the unit to a PC with a USB cable up to 5 m in length.

The inactivity timer for the front port is set to 15 minutes. This controls how long the unit maintains its level of password access on the front port. If no messages are received on the front port for 15 minutes, any password access level that has been enabled is cancelled.

Note:
The front USB port does not support automatic extraction of event and disturbance records, although this data can be accessed manually.

Caution:
When not in use, always close the cover of the USB port to prevent contamination.

3.4.5 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

3.4.6 FUNCTION KEYS

The programmable function keys are available for custom use for some models.

Factory default settings associate specific functions to these keys, but by using programmable scheme logic, you can change the default functions of these keys to fit specific needs. Adjacent to these function keys are programmable LEDs, which are usually set to be associated with their respective function keys. The device has 10 function keys in the 60TE and 80TE case size models and no function keys in the 40TE case size model.

3.4.7 PROGRAMABLE LEDS

The device has 13 of programmable LEDs, which can be associated with PSL-generated signals. The programmable LEDs are tri-colour and can be set to RED, YELLOW or GREEN.

3.5 REAR PANEL

The MiCOM Px40 series uses a modular construction. Most of the internal structure consists of boards and modules that fit into slots. Some of the boards plug into terminal blocks, which are bolted onto the rear of the unit. However, some boards such as the communications boards have their own connectors. The rear panel consists of these terminal blocks plus the rears of the communications boards.

The back panel cut-outs and slot allocations vary. This depends on the product, the type of boards and the terminal blocks needed to populate the case. The following diagram shows a typical rear view of a case populated with various boards.

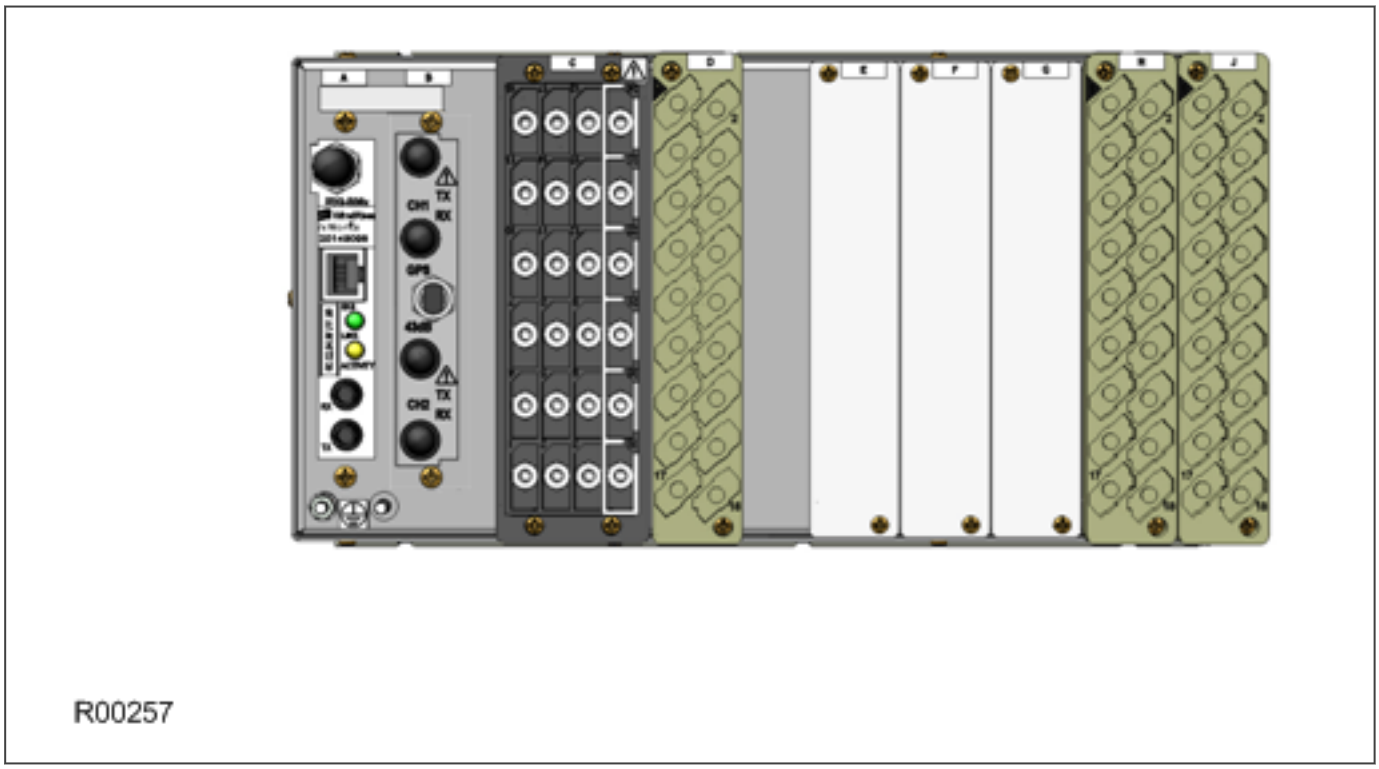


Figure 8: Rear view of populated case

Note:
This diagram is just an example and may not show the exact product described in this manual. It also does not show the full range of available boards, just a typical arrangement.

Not all slots are the same size. The slot width depends on the type of board or terminal block. For example, HD (heavy duty) terminal blocks, as required for the analogue inputs, require a wider slot size than MD (medium duty) terminal blocks. The board positions are not generally interchangeable. Each slot is designed to house a particular type of board. Again this is model-dependent.

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, opto-inputs, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

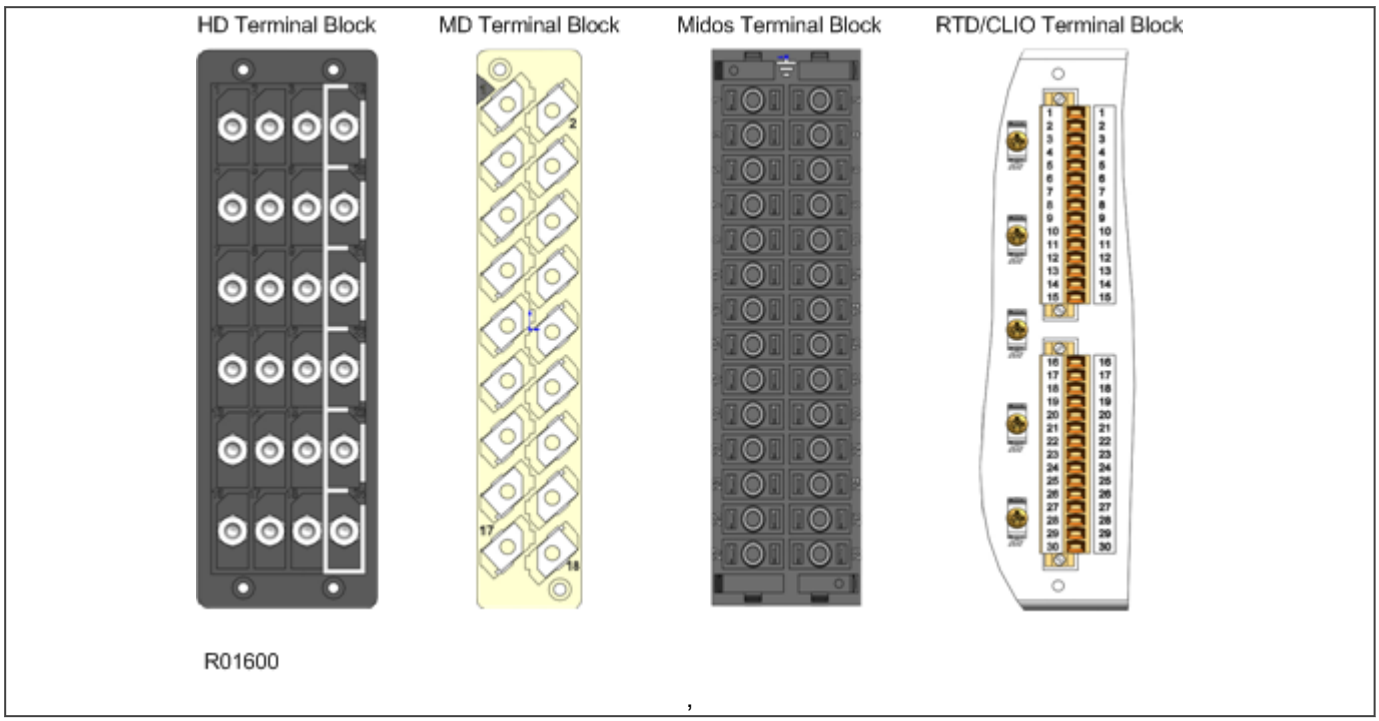


Figure 9: Terminal block types

Note:
Not all products use all types of terminal blocks. The product described in this manual may use one or more of the above types.

3.5.1 TERMINAL BLOCK INGRESS PROTECTION

IP2x shields and side cover panels are designed to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers may be attached during installation or retrofitted to upgrade existing installations - see figure below. For more information, contact your local sales office or our worldwide Contact Centre.

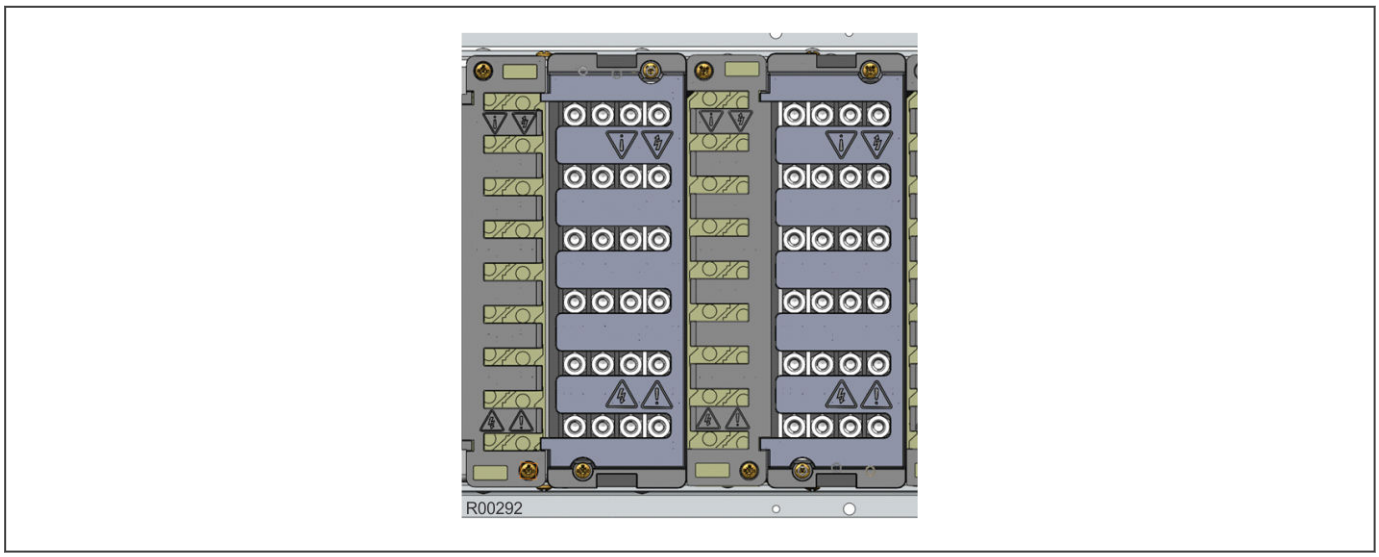


Figure 10: Example - fitted IP2x shields (cabling omitted for clarity)

3.6 BOARDS AND MODULES

Each product comprises a selection of PCBs (Printed Circuit Boards) and subassemblies, depending on the chosen configuration.

3.6.1 PCBS

A PCB typically consists of the components, a front connector for connecting into the main system parallel bus via a ribbon cable, and an interface to the rear. This rear interface may be:

- Directly presented to the outside world (as is the case for communication boards such as Ethernet Boards)
- Presented to a connector, which in turn connects into a terminal block bolted onto the rear of the case (as is the case for most of the other board types)

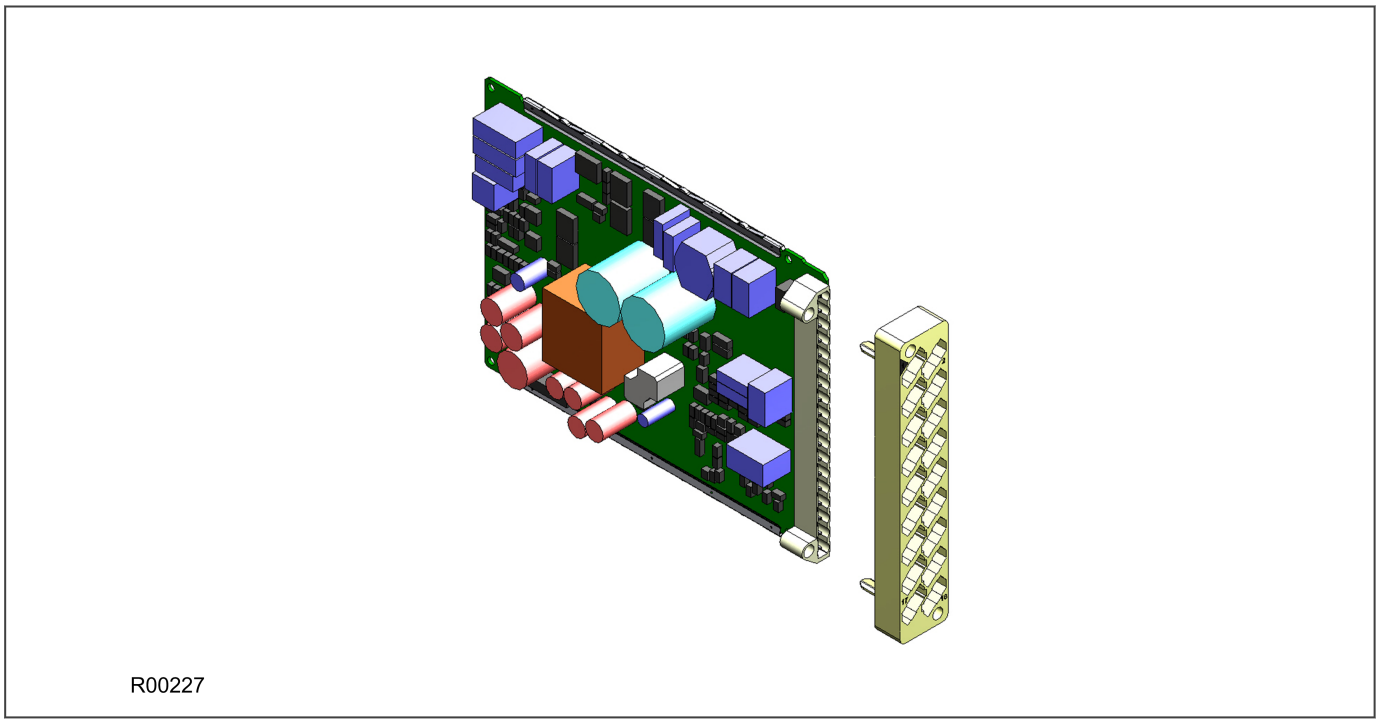


Figure 11: Rear connection to terminal block

3.6.2 SUBASSEMBLIES

A sub-assembly consists of two or more boards bolted together with spacers and connected with electrical connectors. It may also have other special requirements such as being encased in a metal housing for shielding against electromagnetic radiation.

Boards are designated by a part number beginning with ZN, whereas pre-assembled sub-assemblies are designated with a part number beginning with GN. Sub-assemblies, which are put together at the production stage, do not have a separate part number.

The products in the Px40 series typically contain two sub-assemblies:

- The power supply assembly comprising:
  - A power supply board
  - An output relay board
- The input module comprising:
  - One or more transformer boards, which contains the voltage and current transformers (partially or fully populated)
  - One or more input boards
  - Metal protective covers for EM (electromagnetic) shielding

The input module is pre-assembled and is therefore assigned a GN number, whereas the power supply module is assembled at production stage and does not therefore have an individual part number.

3.6.3 MAIN PROCESSOR BOARD

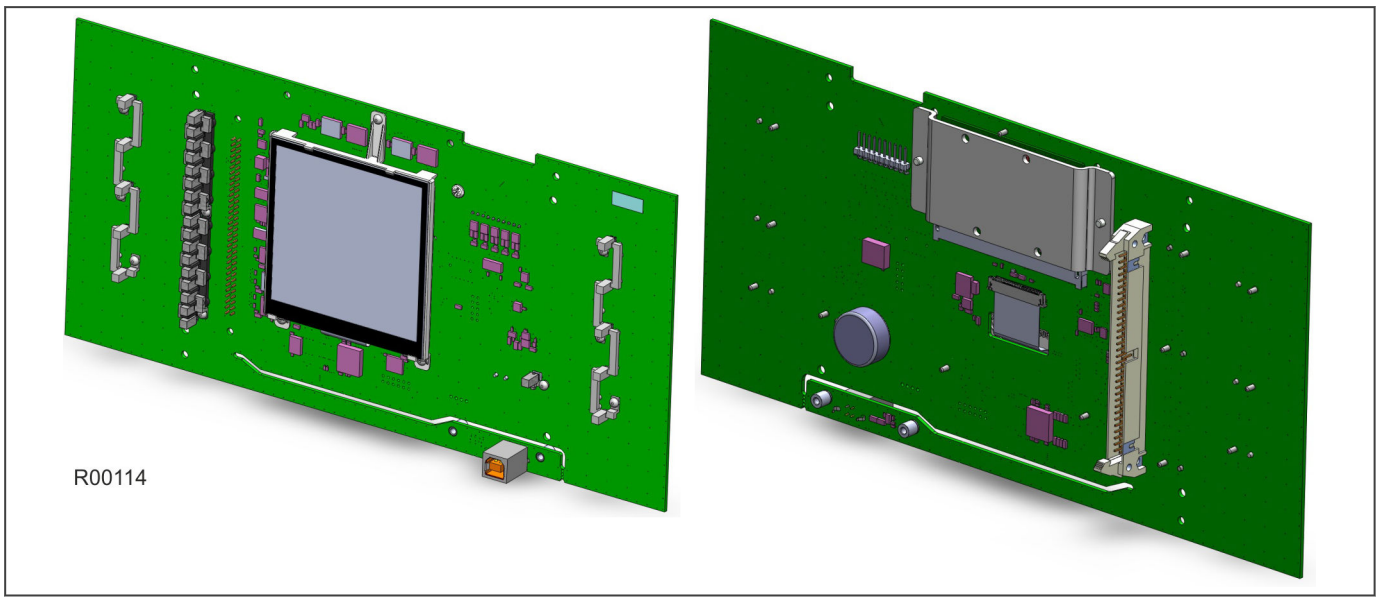


Figure 12: Main processor board

The main processor board performs all calculations and controls the operation of all other modules in the IED, including the data communication and user interfaces. This is the only board that does not fit into one of the slots. It resides in the front panel and connects to the rest of the system using an internal ribbon cable.

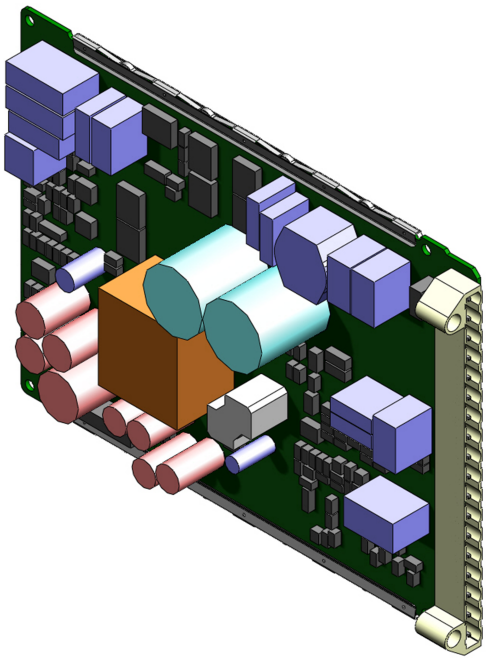
The LCD and LEDs are mounted on the processor board along with the front panel communication ports.

The memory on the main processor board is split into two categories: volatile and non-volatile. The volatile memory is DRAM, used by the processor to run the software and store data during calculations. The non-volatile memory is Flash memory and is used to store Product Firmware, text and configuration data including the present setting values, disturbance records, events, fault and maintenance record data.

There are two board types available depending on the size of the case:

- For models in 40TE cases
- For models in 60TE cases and larger

3.6.4 POWER SUPPLY BOARD



R00228

Figure 13: Power supply board

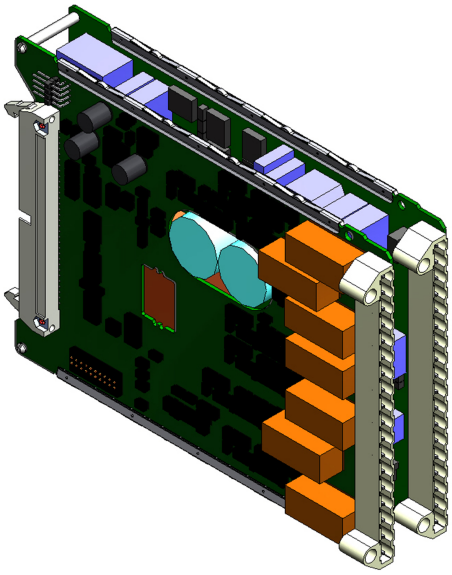
The power supply board provides power to the unit. One of three different configurations of the power supply board can be fitted to the unit. This is specified at the time of order and depends on the magnitude of the supply voltage that will be connected to it.

There are three board types, which support the following voltage ranges:

- 24/54 V DC
- 48/125 V DC or 40-100V AC
- 110/250 V DC or 100-240V AC

The power supply board connector plugs into a medium duty terminal block. This terminal block is always positioned on the right hand side of the unit looking from the rear.

The power supply board is usually assembled together with a relay output board to form a complete subassembly, as shown in the following diagram.



R00229

Figure 14: Power supply assembly

The power supply outputs are used to provide isolated power supply rails to the various modules within the unit. Three voltage levels are used by the unit's modules:

- 5.1 V for all of the digital circuits
- +/- 16 V for the analogue electronics such as on the input board
- 22 V for driving the output relay coils.

All power supply voltages, including the 0 V earth line, are distributed around the unit by the 64-way ribbon cable.

The power supply board incorporates inrush current limiting. This limits the peak inrush current to approximately 10 A.

Power is applied to pins 1 and 2 of the terminal block, where pin 1 is negative and pin 2 is positive. The pin numbers are clearly marked on the terminal block as shown in the following diagram.

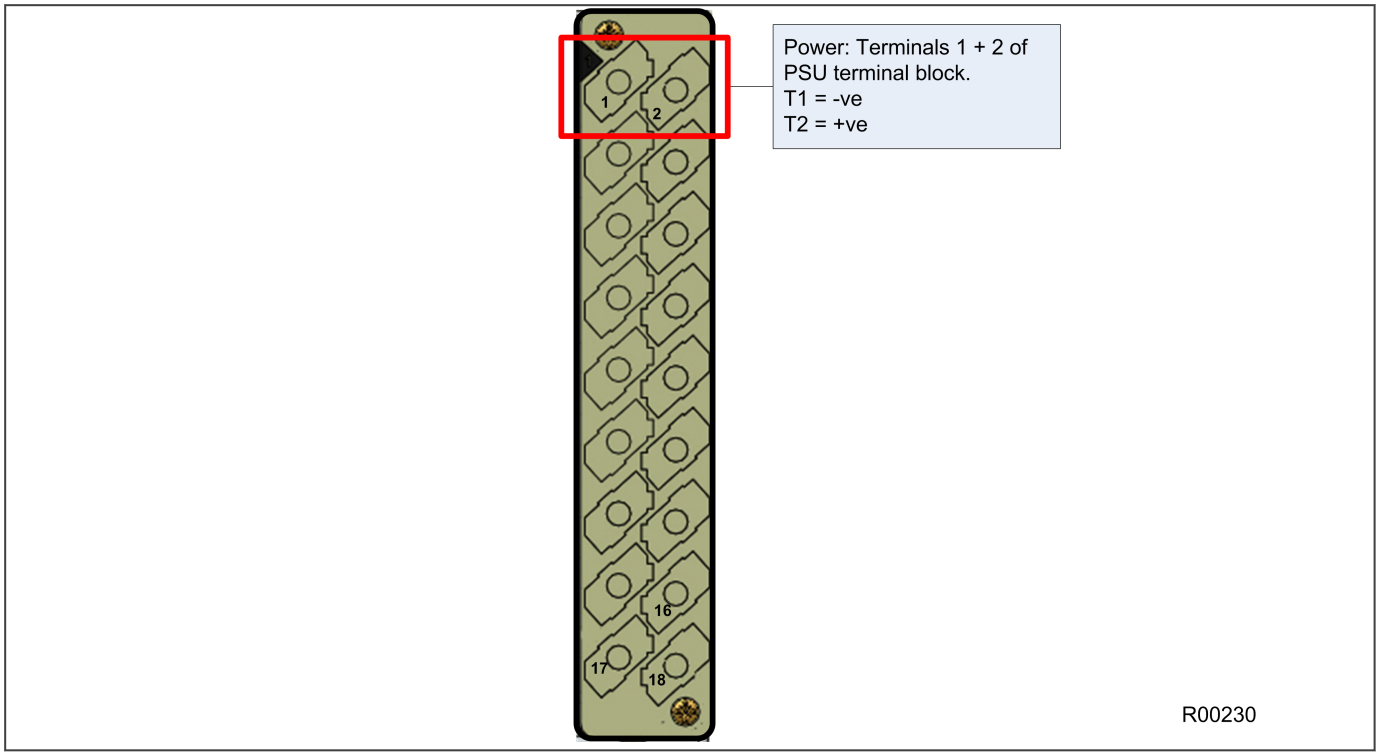


Figure 15: Power supply terminals

3.6.4.1 WATCHDOG

The Watchdog contacts are also hosted on the power supply board. The Watchdog facility provides two output relay contacts, one normally open and one normally closed. These are used to indicate the health of the device and are driven by the main processor board, which continually monitors the hardware and software when the device is in service.

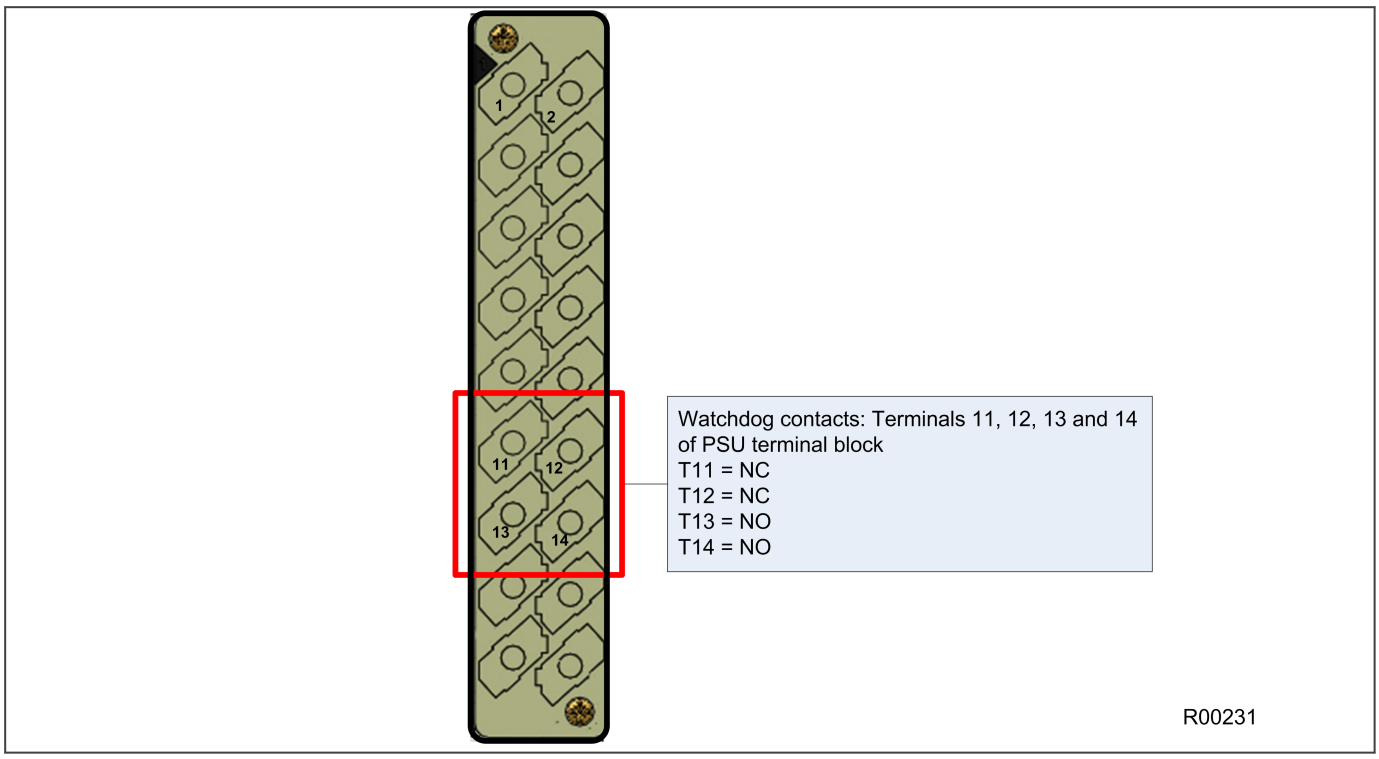


Figure 16: Watchdog contact terminals

3.6.4.2 REAR SERIAL PORT

The rear serial port (RP1) is housed on the power supply board. This is a three-terminal EIA(RS)485 serial communications port and is intended for use with a permanently wired connection to a remote control centre for SCADA communication. The interface supports half-duplex communication and provides optical isolation for the serial data being transmitted and received.

The physical connectivity is achieved using three screw terminals; two for the signal connection, and the third for the earth shield of the cable. These are located on pins 16, 17 and 18 of the power supply terminal block, which is on the far right looking from the rear. The interface can be selected between RS485 and K-bus. When the K-Bus option is selected, the two signal connections are not polarity conscious.

The polarity independent K-bus can only be used for the Courier data protocol. The polarity conscious MODBUS, IEC 60870-5-103 and DNP3.0 protocols need RS485.

The following diagram shows the rear serial port. The pin assignments are as follows:

- Pin 16: Earth shield
- Pin 17: Negative signal
- Pin 18: Positive signal

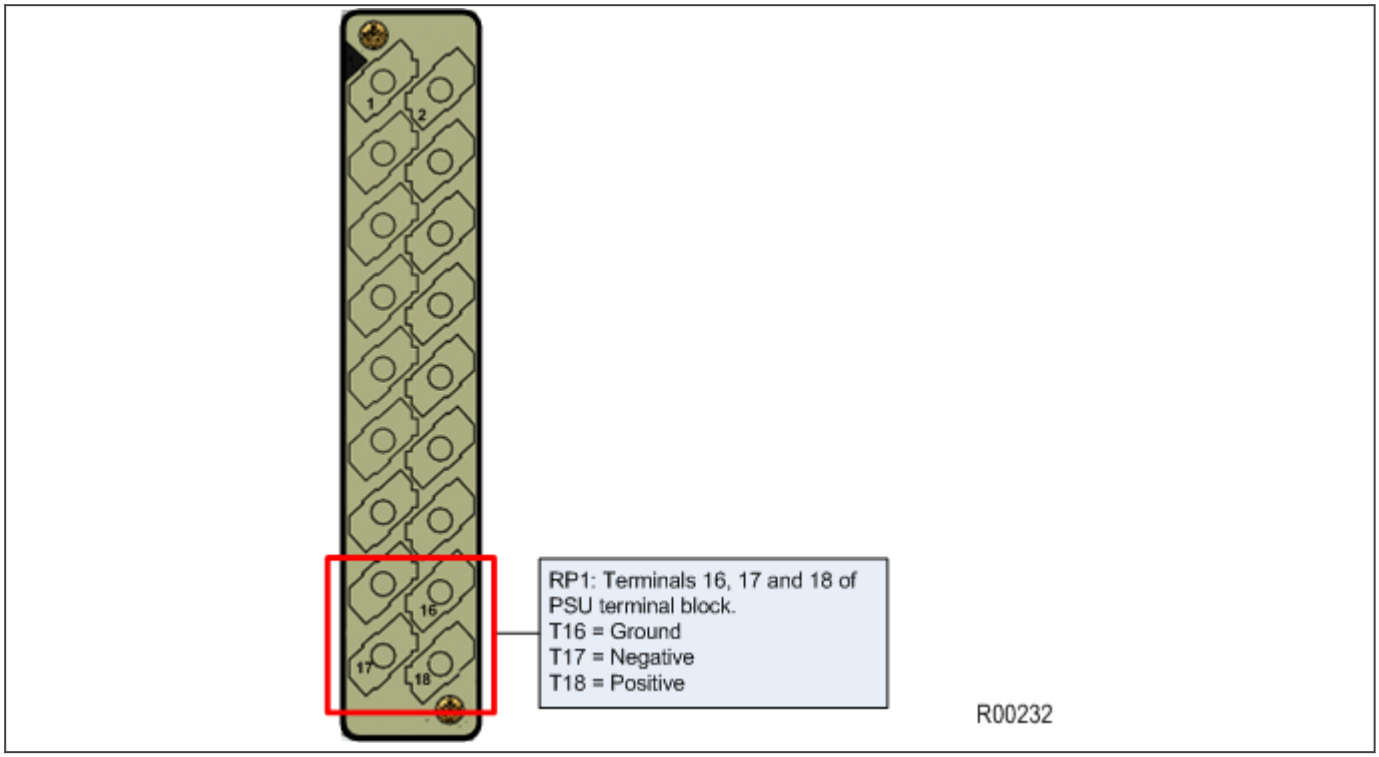


Figure 17: Rear serial port terminals

An additional serial port with D-type presentation is available as an optional board, if required.

3.6.5 INPUT MODULE - 1 TRANSFORMER BOARD

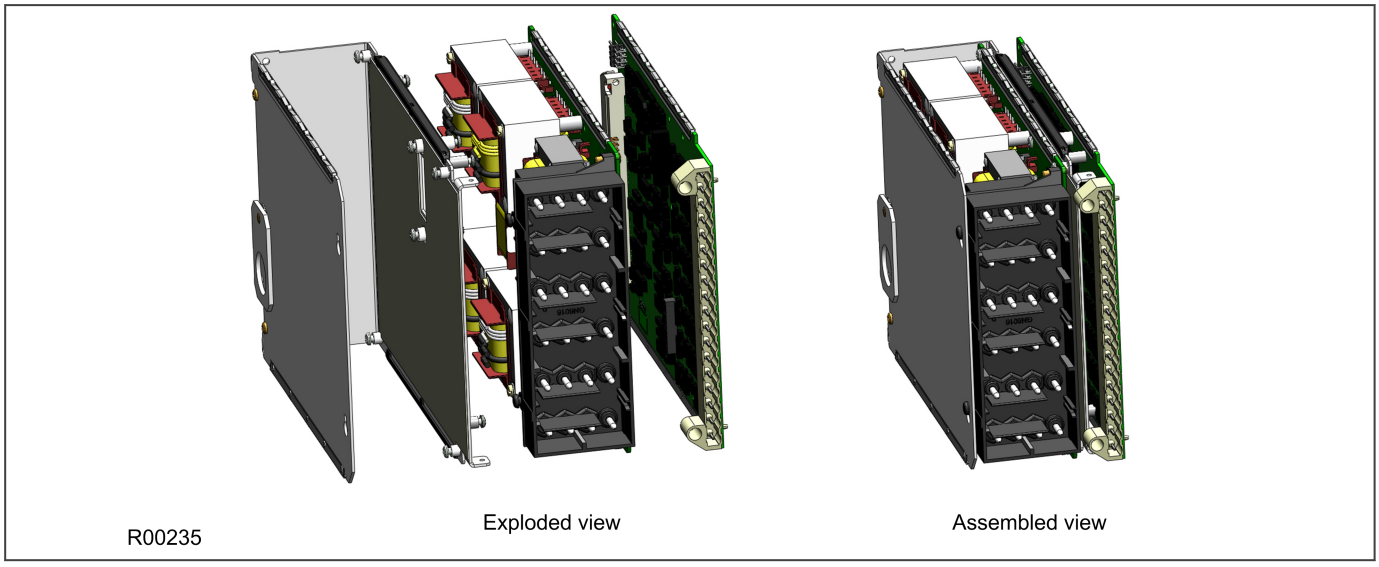


Figure 18: Input module - 1 transformer board

The input module consists of the main input board coupled together with an instrument transformer board. The instrument transformer board contains the voltage and current transformers, which isolate and scale the analogue input signals delivered by the system transformers. The input board contains the A/D conversion and digital processing circuitry, as well as eight digital isolated inputs (opto-inputs).

The boards are connected together physically and electrically. The module is encased in a metal housing for shielding against electromagnetic interference.

3.6.5.1 INPUT MODULE CIRCUIT DESCRIPTION

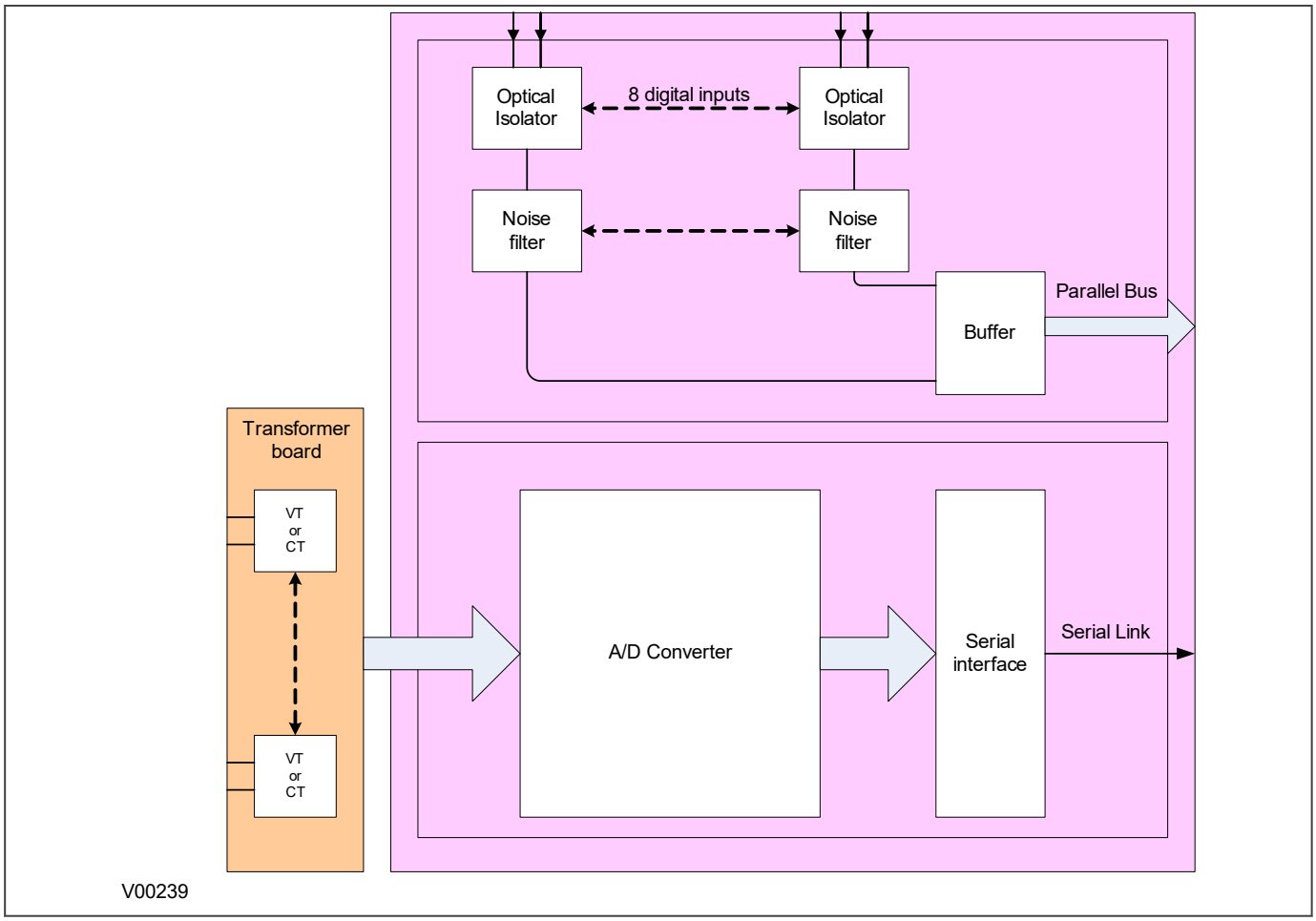


Figure 19: Input module schematic

A/D Conversion

The differential analogue inputs from the CT and VT transformers are presented to the main input board as shown. Each differential input is first converted to a single input quantity referenced to the input board's earth potential. The analogue inputs are sampled and converted to digital, then filtered to remove unwanted properties. The samples are then passed through a serial interface module which outputs data on the serial sample data bus.

The calibration coefficients are stored in non-volatile memory. These are used by the processor board to correct for any amplitude or phase errors introduced by the transformers and analogue circuitry.

Opto-isolated inputs

The other function of the input board is to read in the state of the digital inputs. As with the analogue inputs, the digital inputs must be electrically isolated from the power system. This is achieved by means of the 8 on-board optical isolators for connection of up to 8 digital signals. The digital signals are passed through an optional noise filter before being buffered and presented to the unit's processing boards in the form of a parallel data bus.

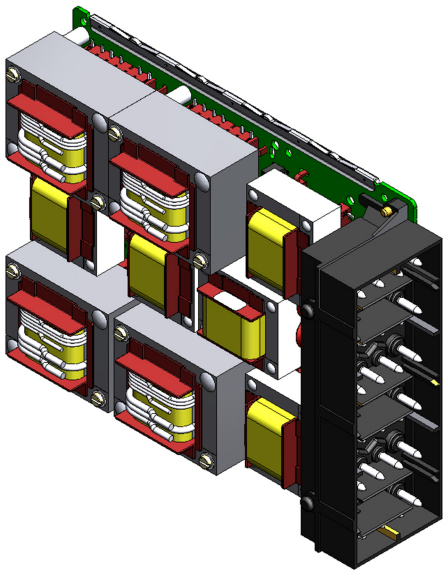
This selectable filtering allows the use of a pre-set filter of ½ cycle which renders the input immune to induced power-system noise on the wiring. Although this method is secure it can be slow, particularly for inter-tripping. This can be improved by switching off the ½ cycle filter, in which case one of the following methods to reduce ac noise should be considered.

- Use double pole switching on the input
- Use screened twisted cable on the input circuit

The opto-isolated logic inputs can be configured for the nominal battery voltage of the circuit for which they are a part, allowing different voltages for different circuits such as signalling and tripping.

Note:
The opto-input circuitry can be provided without the A/D circuitry as a separate board, which can provide supplementary opto-inputs.

3.6.5.2 TRANSFORMER BOARD



R00237

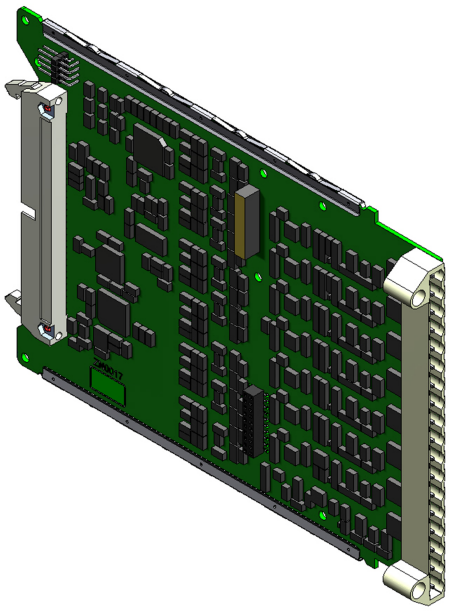
Figure 20: Transformer board

The transformer board hosts the current and voltage transformers. These are used to step down the currents and voltages originating from the power systems' current and voltage transformers to levels that can be used by the devices' electronic circuitry. In addition to this, the on-board CT and VT transformers provide electrical isolation between the unit and the power system.

The transformer board is connected physically and electrically to the input board to form a complete input module.

For terminal connections, please refer to the wiring diagrams.

3.6.5.3 INPUT BOARD



R00238

Figure 21: Input board

The input board is used to convert the analogue signals delivered by the current and voltage transformers into digital quantities used by the IED. This input board also has on-board opto-input circuitry, providing eight optically-isolated digital inputs and associated noise filtering and buffering. These opto-inputs are presented to the user by means of an MD terminal block, which sits adjacent to the analogue inputs HD terminal block.

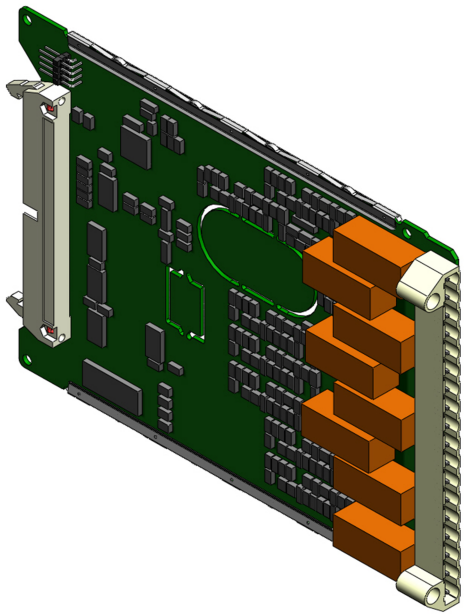
The input board is connected physically and electrically to the transformer board to form a complete input module.

The terminal numbers of the opto-inputs are as follows:

Terminal Number	Opto-input
Terminal 1	Opto 1 -ve
Terminal 2	Opto 1 +ve
Terminal 3	Opto 2 -ve
Terminal 4	Opto 2 +ve
Terminal 5	Opto 3 -ve
Terminal 6	Opto 3 +ve
Terminal 7	Opto 4 -ve
Terminal 8	Opto 4 +ve
Terminal 9	Opto 5 -ve
Terminal 10	Opto 5 +ve
Terminal 11	Opto 6 -ve
Terminal 12	Opto 6 +ve
Terminal 13	Opto 7 –ve
Terminal 14	Opto 7 +ve

Terminal Number	Opto-input
Terminal 15	Opto 8 –ve
Terminal 16	Opto 8 +ve
Terminal 17	Common
Terminal 18	Common

3.6.6 STANDARD OUTPUT RELAY BOARD



R00234

Figure 22: Standard relay output board - 8 contacts

This output relay board has 8 relays with 6 Normally Open contacts and 2 Changeover contacts.

The output relay board is provided together with the power supply board as a complete assembly, or independently for the purposes of relay output expansion.

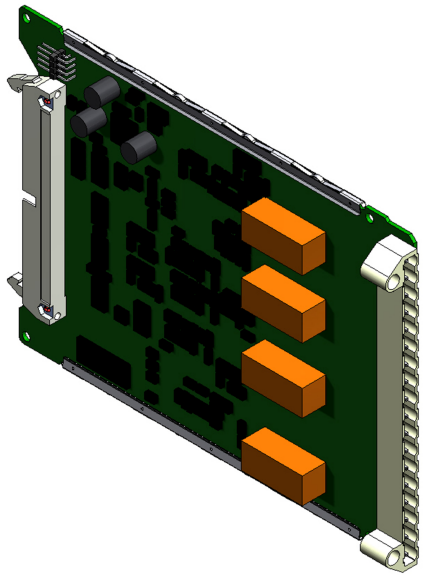
There are two cut-out locations in the board. These can be removed to allow power supply components to protrude when coupling the output relay board to the power supply board. If the output relay board is to be used independently, these cut-out locations remain intact.

The terminal numbers are as follows:

Terminal Number	Output Relay
Terminal 1	Relay 1 NO
Terminal 2	Relay 1 NO
Terminal 3	Relay 2 NO
Terminal 4	Relay 2 NO
Terminal 5	Relay 3 NO
Terminal 6	Relay 3 NO

Terminal Number	Output Relay
Terminal 7	Relay 4 NO
Terminal 8	Relay 4 NO
Terminal 9	Relay 5 NO
Terminal 10	Relay 5 NO
Terminal 11	Relay 6 NO
Terminal 12	Relay 6 NO
Terminal 13	Relay 7 changeover
Terminal 14	Relay 7 changeover
Terminal 15	Relay 7 common
Terminal 16	Relay 8 changeover
Terminal 17	Relay 8 changeover
Terminal 18	Relay 8 common

3.6.7 HIGH BREAK OUTPUT RELAY BOARD



R00245

Figure 23: High Break relay output board

A High Break output relay board is available as an option. It comprises four normally open output contacts, which are suitable for high breaking loads.

A High Break contact consists of a high capacity relay with a MOSFET in parallel with it. The MOSFET has a varistor placed across it to provide protection, which is required when switching off inductive loads. This is because the stored energy in the inductor causes a high reverse voltage that could damage the MOSFET, if not protected.

When there is a control input command to operate an output contact the miniature relay is operated at the same time as the MOSFET. The miniature relay contact closes in nominally 3.5 ms and is used to carry the continuous load current. The MOSFET operates in less than 0.2 ms, but is switched off after 7.5 ms.

When the control input is reset, the MOSFET is again turned on for 7.5 mS. The miniature relay resets in nominally 3.5 ms before the MOSFET. This means the MOSFET is used to break the load. The MOSFET absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching DC circuits only.

The board number is:

- ZN0042 001

High Break Contact Operation

The following figure shows the timing diagram for High Break contact operation.

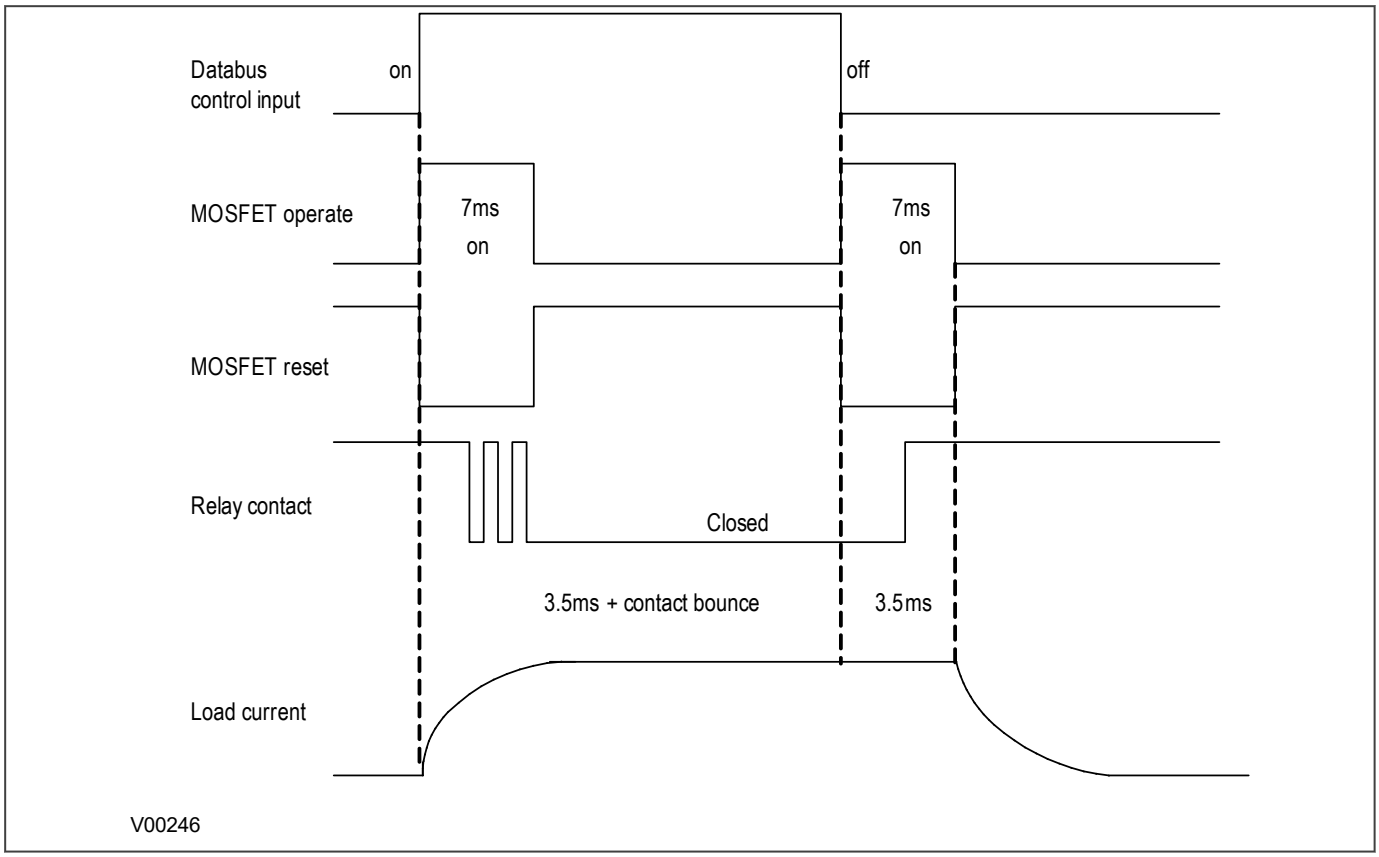


Figure 24: High Break contact operation

High Break Contact Applications

- Efficient scheme engineering

  In traditional hard wired scheme designs, High Break capability could only be achieved using external electromechanical trip relays. Instead, these internal High Break contacts can be used thus reducing space requirements.

- Accessibility of CB auxiliary contacts

  It is common practise to use circuit breaker 52a (CB Closed) auxiliary contacts to break the trip coil current on breaker opening, thereby easing the duty on the protection contacts. In some cases (such as operation of disconnectors, or retrofitting), it may be that 52a contacts are either unavailable or unreliable. In such cases, High Break contacts can be used to break the trip coil current in these applications.

- Breaker fail

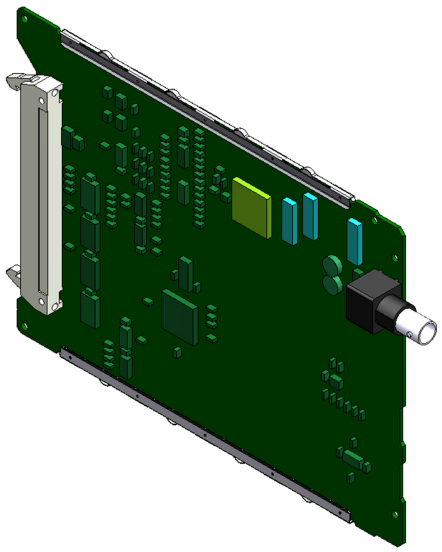
  In the event of failure of the local circuit breaker (stuck breaker), or defective auxiliary contacts (stuck contacts), it is incorrect to use 52a contact action. The interrupting duty at the local breaker then falls on the relay output contacts, which may not be rated to perform this duty. High Break contacts should be used in this case to avoid the risk of burning out relay contacts.

- Initiation of teleprotection

  The High Break contacts also offer fast making, which results in faster tripping. In addition, fast keying of teleprotection is a benefit. Fast keying bypasses the usual contact operation time, such that permissive, blocking and intertrip commands can be routed faster.

Warning:
These relay contacts are POLARITY SENSITIVE. External wiring must comply with the polarity requirements described in the external connection diagram to ensure correct operation.

3.6.8 IRIG-B BOARD



R00240

Figure 25: IRIG-B board

The IRIG-B board can be fitted to provide an accurate timing reference for the device. The IRIG-B signal is connected to the board via an BNC connector. The timing information is used to synchronise the IED's internal real-time clock to an accuracy of 1 ms. The internal clock is then used for time tagging events, fault, maintenance and disturbance records.

IRIG-B interface is available in modulated or demodulated formats.

The IRIG-B facility is provided in combination with other functionality on a number of additional boards, such as:

- Fibre board with IRIG-B
- Second rear communications board with IRIG-B
- Ethernet board with IRIG-B
- Redundant Ethernet board with IRIG-B

There are three types of each of these boards; one type which accepts a modulated IRIG-B input, one type which accepts a demodulated IRIG-B input and one type which accepts a universal IRIG-B input. The order code will indicate which variant it supports.

3.6.9 FIBRE OPTIC BOARD

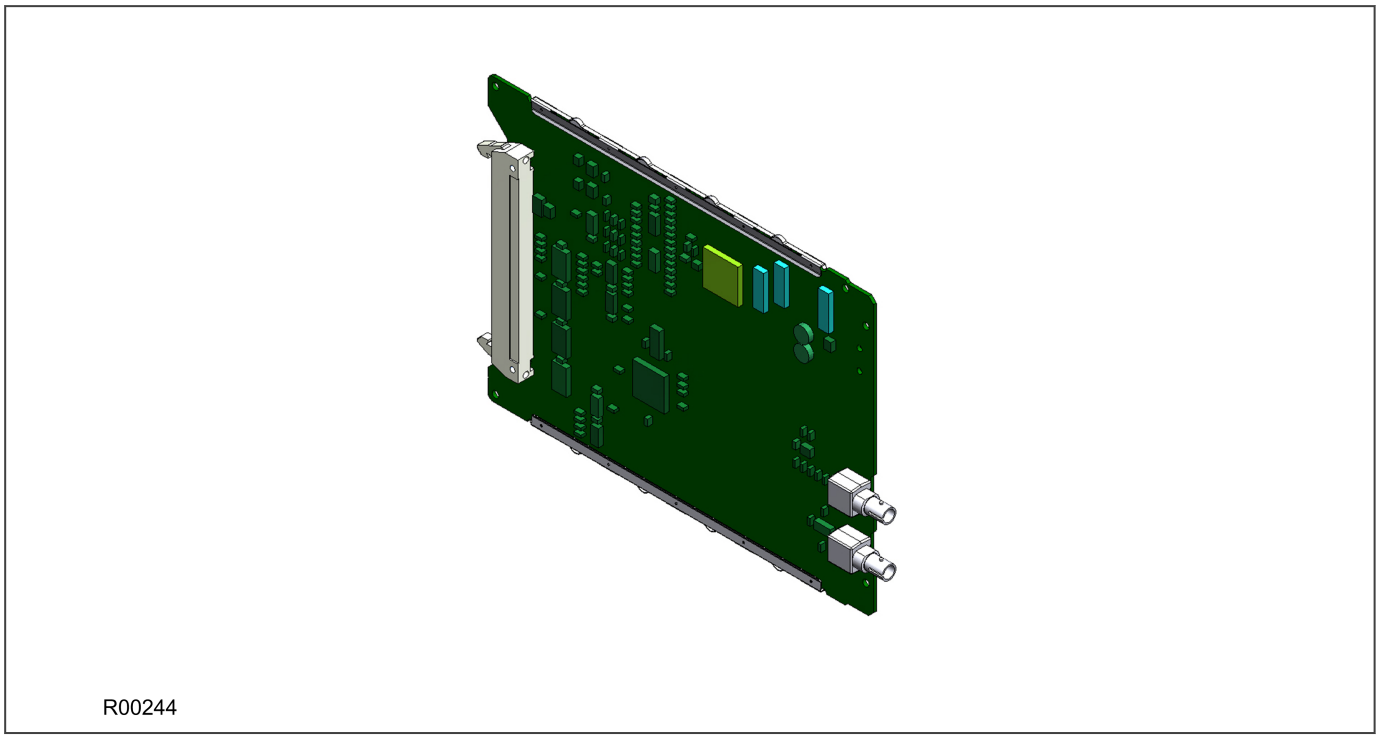


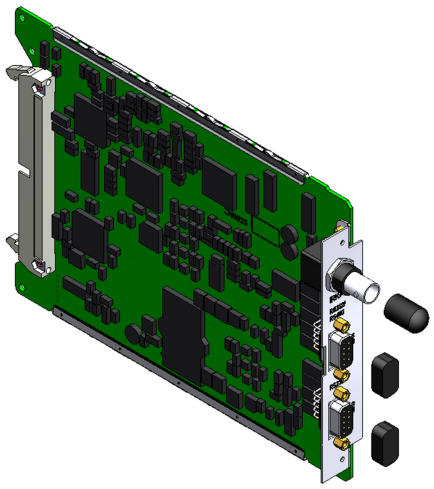
Figure 26: Fibre optic board

This board provides an interface for communicating with a master station. This communication link can use all compatible protocols (Courier, IEC 60870-5-103, MODBUS and DNP 3.0). It is a fibre-optic alternative to the metallic RS485 port presented on the power supply terminal block. The metallic and fibre optic ports are mutually exclusive.

The fibre optic port uses BFOC 2.5 ST connectors.

The board comes in two varieties; one with an IRIG-B input and one without:

3.6.10 REAR COMMUNICATION BOARD



R00243

Figure 27: Rear communication board

The optional communications board containing the secondary communication ports provide two serial interfaces presented on 9 pin D-type connectors. These interfaces are known as SK4 and SK5. Both connectors are female connectors, but are configured as DTE ports. This means pin 2 is used to transmit information and pin 3 to receive.

SK4 can be used with RS232, RS485 and K-bus. SK5 can only be used with RS232 and is used for electrical teleprotection. The optional rear communications board and IRIG-B board are mutually exclusive since they use the same hardware slot. However, the board comes in two varieties; one with an IRIG-B input and one without.

3.6.11 SINGLE ETHERNET BOARD

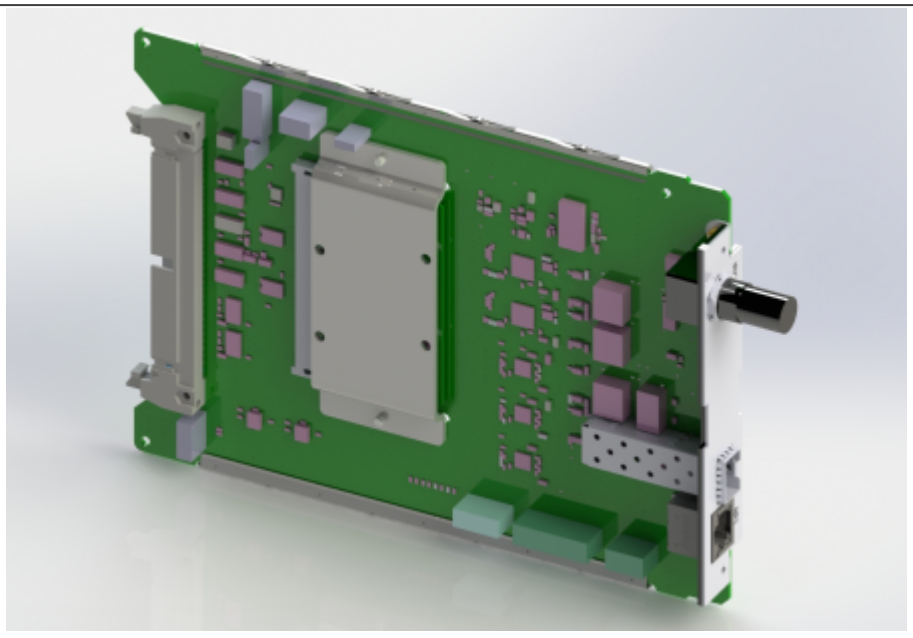


Figure 28: Ethernet board

This board provides one optical 100Mbps LC duplex Ethernet port (NP2A) for station bus communications, with a universal IRIG-B interface for time synchronisation, and a separate 10/100Mbps RJ45 Ethernet maintenance/ engineering interface (NP1) for monitoring and configuration purposes.

The Ethernet and other connection details are described below:

RJ45 Connector (NP1 only)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

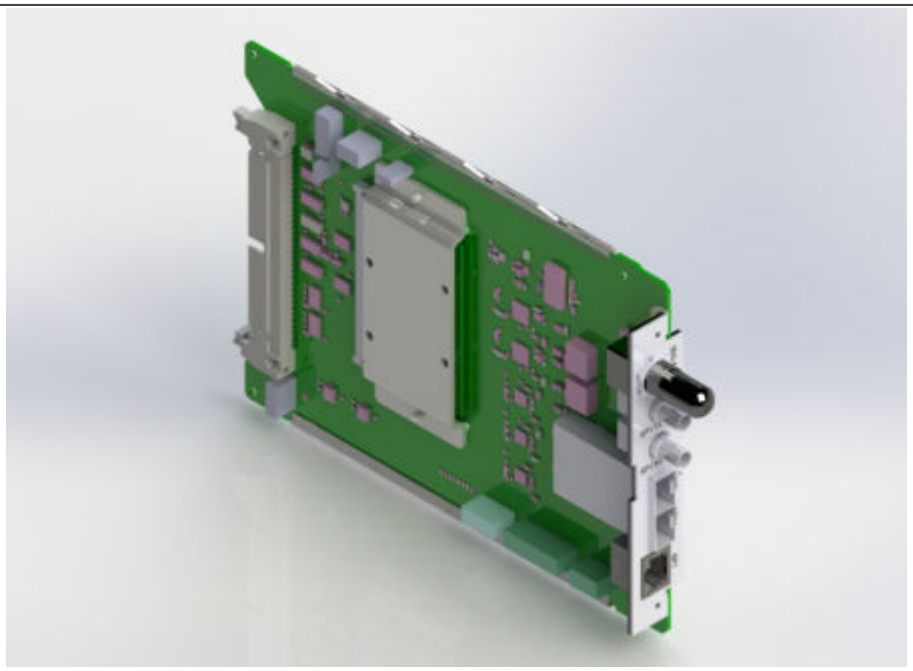
UNIVERSAL IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

LC Optical Fibre Connector (NP2A only)

Connector	SFP
A	TX
B	RX

3.6.12 REDUNDANT ETHERNET BOARD



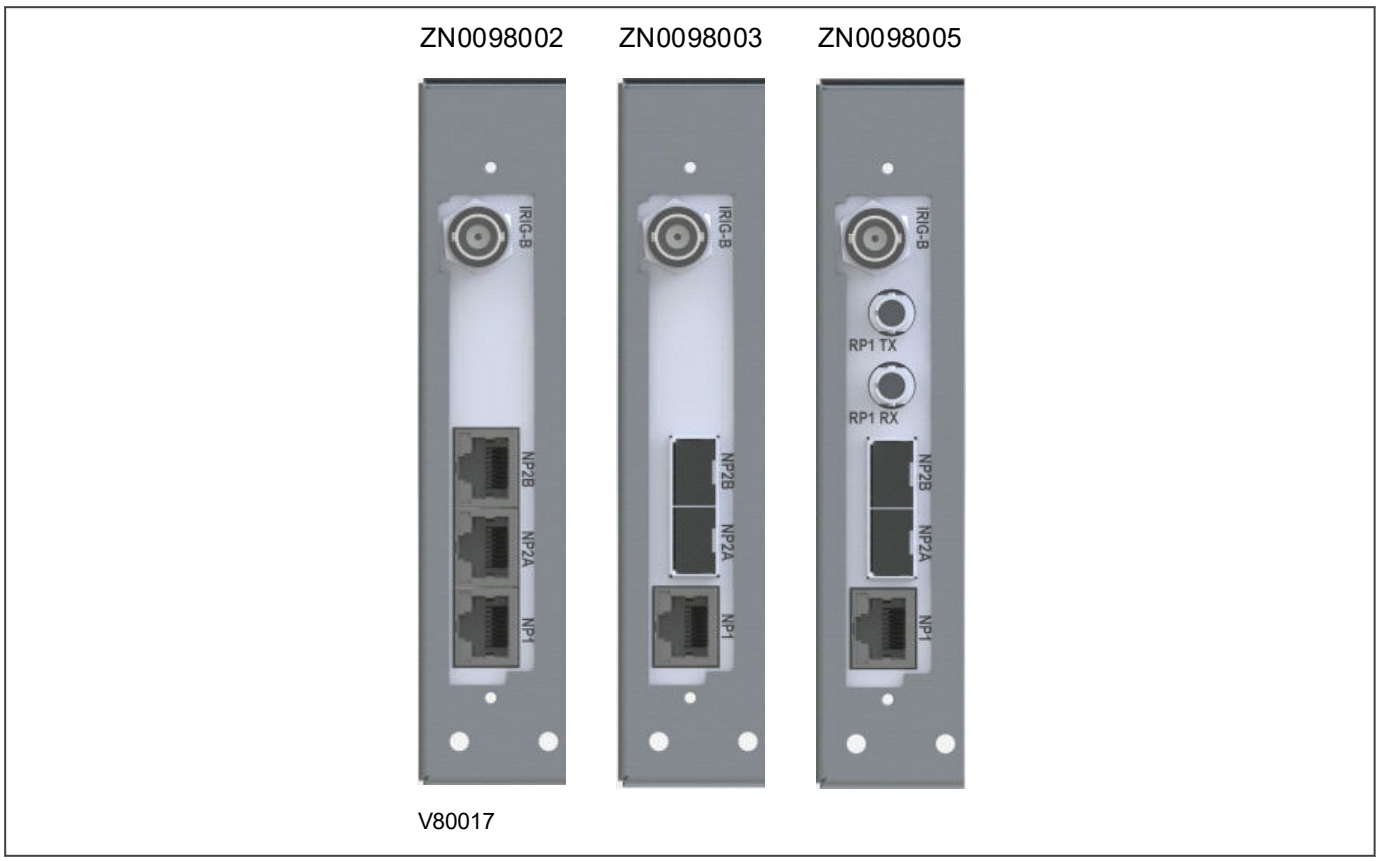


Figure 29: Redundant Ethernet board

This board provides dual redundant Ethernet (NP2A and NP2B) for station bus communications. A universal IRIG-B interface for time synchronisation and a separate Ethernet interface (NP1) for monitoring two variants. A new variant also provides serial protocol support on fiber optics (RP1).

The available redundancy protocols are:

- RSTP (Rapid Spanning Tree Protocol)
- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- Failover

There are several variants for this board as follows:

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with a serial protocol communications ST fibre port with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

Two RJ45 duplex redundant 10/100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

Two LC duplex redundant 100Mbps Ethernet ports running RSTP + PRP + HSR + Failover, with on-board universal IRIG-B and one 10/100Mbps RJ45 maintenance/engineering port.

The Ethernet and other connection details are described below:

UNIVERSAL IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

LC Optical Fibre Connector (only for NP2A or NP2B when ordering fibre ports on station bus ports)

Connector	SFP
A	TX
B	RX

ST Optical Fibre Connector (only for RP1 serial communications)

Connector	Communications
RP1	TX
RP2	RX

RJ45 Connector (NP1 or NP2A/NP2B when ordering two copper ports on station bus ports only)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

3.6.13 RTD BOARD

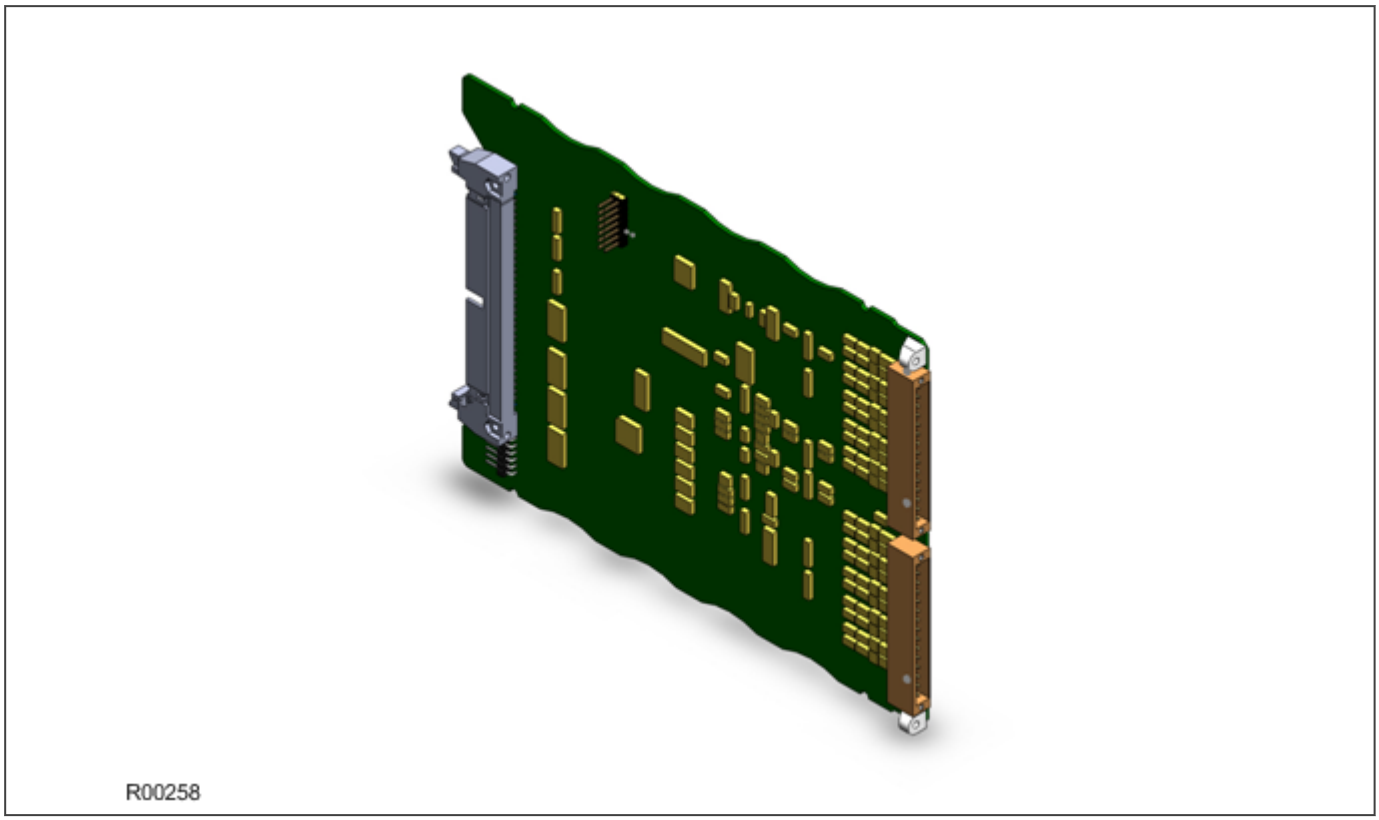


Figure 30: RTD board

The RTD board provides two banks of 15 terminals to support ten RTD inputs, of the type PT100, Ni100, or Ni120, depending on the product. There are three terminals for each RTD, therefore 30 terminals altogether. The RTD board fits into slot B or slot C, depending on the model variant.

The terminal numbers of the RTDs are as follows:

Terminal Number	RTD Connection
Terminal 1	RTD1 wire 1
Terminal 2	RTD1 wire 2
Terminal 3	RTD1 wire 3
Terminal 4	RTD2 wire 1
Terminal 5	RTD2 wire 2
Terminal 6	RTD2 wire 3
Terminal 7	RTD3 wire 1
Terminal 8	RTD3 wire 2
Terminal 9	RTD3 wire 3
Terminal 10	RTD4 wire 1
Terminal 11	RTD4 wire 2
Terminal 12	RTD4 wire 3

Terminal Number	RTD Connection
Terminal 13	RTD5 wire 1
Terminal 14	RTD5 wire 2
Terminal 15	RTD5 wire 3
Terminal 16	RTD6 wire 1
Terminal 17	RTD6 wire 2
Terminal 18	RTD6 wire 3
Terminal 19	RTD7 wire 1
Terminal 20	RTD7 wire 2
Terminal 21	RTD7 wire 3
Terminal 22	RTD8 wire 1
Terminal 23	RTD8 wire 2
Terminal 24	RTD8 wire 3
Terminal 25	RTD9 wire 1
Terminal 26	RTD9 wire 2
Terminal 27	RTD9 wire 3
Terminal 28	RTD10 wire 1
Terminal 29	RTD10 wire 2
Terminal 30	RTD10 wire 3

3.6.14 CLIO BOARD

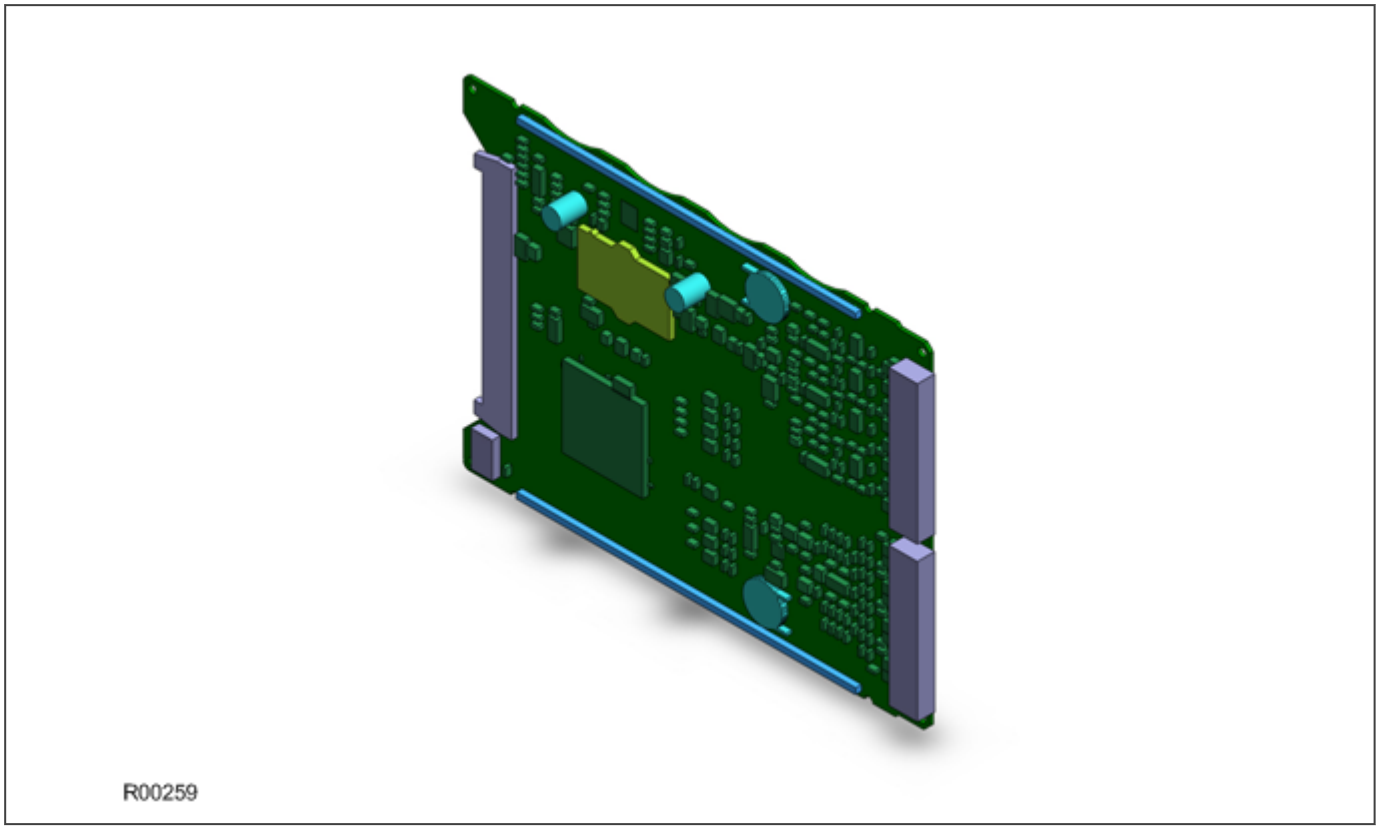


Figure 31: CLIO board

The CLIO board provides two banks of 15 terminals to support four current loop inputs and four current loop outputs. There are three terminals for each input and three for each output, therefore 24 of the terminals are used altogether. The CLIO board fits into slot B or slot C, depending on the model variant.

The terminal numbers of the current loop inputs and outputs are as follows:

Terminal Number	Current Loop Connection
Terminal 1	CLO1 - 20 mA input
Terminal 2	CLO1 - 1 mA input
Terminal 3	CLO1 - common input
Terminal 4	Not used
Terminal 5	CLO2 - 20 mA input
Terminal 6	CLO2 - 1 mA input
Terminal 7	CLO2 - common input
Terminal 8	Not used
Terminal 9	CLO3 - 20 mA input
Terminal 10	CLO3 - 1 mA input
Terminal 11	CLO3 - common input
Terminal 12	Not used
Terminal 13	CLO4 - 20 mA input

Terminal Number	Current Loop Connection
Terminal 14	CLO4 - 1 mA input
Terminal 15	CLO4 - common input
Terminal 16	CLI1 - 20 mA input
Terminal 17	CLI1 - 1 mA input
Terminal 18	CLI1 - common input
Terminal 19	Not used
Terminal 20	CLI2 - 20 mA input
Terminal 21	CLI2 - 1 mA input
Terminal 22	CLI2 - common input
Terminal 23	Not used
Terminal 24	CLI3 - 20 mA input
Terminal 25	CLI3 - 1 mA input
Terminal 26	CLI3 - common input
Terminal 27	Not used
Terminal 28	CLI4 - 20 mA input
Terminal 29	CLI4 - 1 mA input
Terminal 30	CLI4 - common input

CHAPTER 4

SOFTWARE DESIGN

4.1 CHAPTER OVERVIEW

This chapter describes the software design of the IED.

This chapter contains the following sections:

Chapter Overview 66
Sofware Design Overview 67
System Level Software 68
Platform Software 71
Protection and Control Functions 72

4.2 SOFWARE DESIGN OVERVIEW

The device software can be conceptually categorized into several elements as follows:

- The system level software
- The platform software
- The protection and control software

These elements are not distinguishable to the user, and the distinction is made purely for the purposes of explanation. The following figure shows the software architecture.

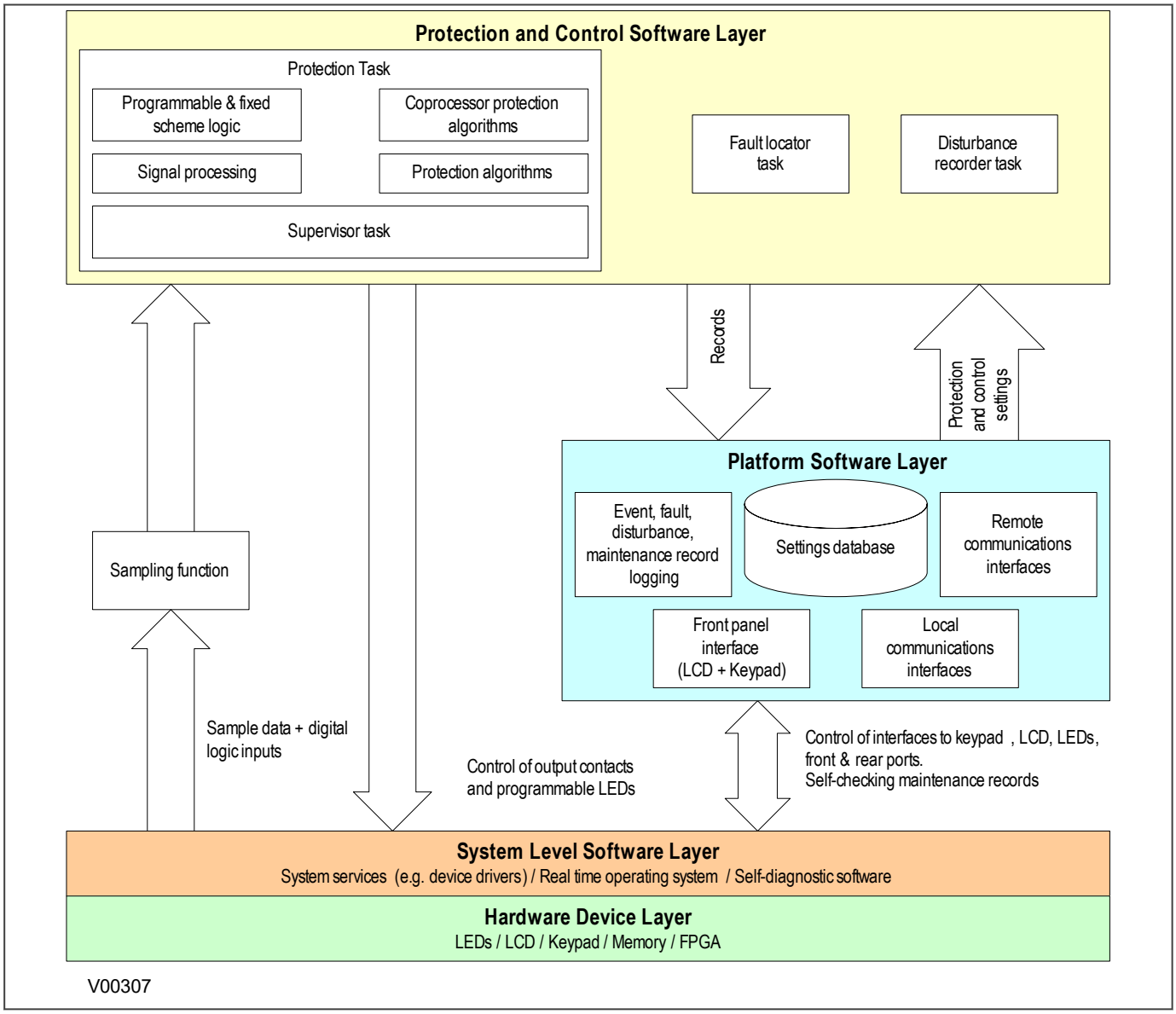


Figure 32: Software Architecture

The software, which executes on the main processor, can be divided into a number of functions as illustrated above. Each function is further broken down into a number of separate tasks. These tasks are then run according to a scheduler. They are run at either a fixed rate or they are event driven. The tasks communicate with each other as and when required.

4.3 SYSTEM LEVEL SOFTWARE

4.3.1 REAL TIME OPERATING SYSTEM

The real-time operating system is used to schedule the processing of the various tasks. This ensures that they are processed in the time available and in the desired order of priority. The operating system also plays a part in controlling the communication between the software tasks, through the use of operating system messages.

4.3.2 SYSTEM SERVICES SOFTWARE

The system services software provides the layer between the hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports. It also controls things like the booting of the processor and the downloading of the processor code into DRAM at startup.

4.3.3 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the ‘Healthy’ LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the ‘Healthy’ LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

4.3.4 STARTUP SELF-TESTING

The self-testing takes a few seconds to complete, during which time the IEDs measurement, recording, control, and protection functions are unavailable. On a successful start-up and self-test, the ‘Healthy' state LED on the front of the device is switched on. If a problem is detected during the start-up testing, the device remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

1. System boot
2. System software initialisation
3. Platform software initialisation and monitoring

4.3.4.1 SYSTEM BOOT

The integrity of the Flash memory is verified using a checksum before the program code and stored data is loaded into DRAM for execution by the processor. When the loading has been completed, the data held in DRAM is compared to that held in the Flash memory to ensure that no errors have occurred in the data transfer and that the two are the same. The entry point of the software code in DRAM is then called. This is the IED's initialisation code.

4.3.4.2 SYSTEM LEVEL SOFTWARE INITIALISATION

The initialization process initializes the processor registers and interrupts, starts the watchdog timers (used by the hardware to determine whether the software is still running), starts the real-time operating system and creates and starts the supervisor task. In the initialization process the device checks the following:

- The status of the supercapacitor to maintain the real time clock
- The operation of the LCD controller
- The watchdog operation

At the conclusion of the initialization software the supervisor task begins the process of starting the platform software. Coprocessor board checks are also made as follows:

- A check is made for the presence of the coprocessor board
- The DRAM on the coprocessor board is checked

If any of these checks produces an error, the coprocessor board is left out of service. The other protection functions provided by the main processor board are left in service.

4.3.4.3 PLATFORM SOFTWARE INITIALISATION AND MONITORING

When starting the platform software, the IED checks the following:

- The integrity of the data held in non-volatile memory (using a checksum)
- The operation of the real-time clock
- The optional IRIG-B function (if applicable)
- The presence and condition of the input board
- The analog data acquisition system (it does this by sampling the reference voltage)

At the successful conclusion of all of these tests the unit is entered into service and the application software is started up.

4.3.5 CONTINUOUS SELF TESTING

When the IED is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software and the results are reported to the platform software. The functions that are checked are as follows:

- The Flash memory containing all program code and language text is verified by a checksum.
- The code and constant data held in system memory is checked against the corresponding data in Flash memory to check for data corruption.
- The system memory containing all data other than the code and constant data is verified with a checksum.
- The integrity of the digital signal I/O data from the opto-inputs and the output relay coils is checked by the data acquisition function every time it is executed.
- The operation of the analog data acquisition system is continuously checked by the acquisition function every time it is executed. This is done by sampling the reference voltages.
- The operation of the optional Ethernet board is checked by the software on the main processor board. If the Ethernet board fails to respond an alarm is raised and the board is reset in an attempt to resolve the problem.
- The operation of the optional IRIG-B function is checked by the software that reads the time and date from the board.
- Where fitted, the operation of the RTD board is checked by reading the temperature indicated by the reference resistors on the two spare RTD channels.
- Where fitted, the operation of the CLIO board is checked.

In the event that one of the checks detects an error in any of the subsystems, the platform software is notified and it attempts to log a maintenance record.

If the problem is with the IRIG-B board, the device continues in operation. For problems detected in any other area, the device initiates a shutdown and re-boot, resulting in a period of up to 10 seconds when the functionality is unavailable.

A restart should clear most problems that may occur. If, however, the diagnostic self-check detects the same problem that caused the IED to restart, it is clear that the restart has not cleared the problem, and the device takes itself permanently out of service. This is indicated by the ‘’health-state’ LED on the front of the device, which switches OFF, and the watchdog contact which switches ON.

4.4 PLATFORM SOFTWARE

The platform software has three main functions:

- To control the logging of records generated by the protection software, including alarms, events, faults, and maintenance records
- To store and maintain a database of all of the settings in non-volatile memory
- To provide the internal interface between the settings database and the user interfaces, using the front panel interface and the front and rear communication ports

4.4.1 RECORD LOGGING

The logging function is used to store all alarms, events, faults and maintenance records. The records are stored in non-volatile memory to provide a log of what has happened. The IED maintains four types of log on a first in first out basis (FIFO). These are:

- Alarms
- Event records
- Fault records
- Maintenance records

The logs are maintained such that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software. The platform software is responsible for logging a maintenance record in the event of an IED failure. This includes errors that have been detected by the platform software itself or errors that are detected by either the system services or the protection software function. See the Monitoring and Control chapter for further details on record logging.

4.4.2 SETTINGS DATABASE

The settings database contains all the settings and data, which are stored in non-volatile memory. The platform software manages the settings database and ensures that only one user interface can modify the settings at any one time. This is a necessary restriction to avoid conflict between different parts of the software during a setting change. Changes to protection settings and disturbance recorder settings, are first written to a temporary location DRAM memory. This is sometimes called 'Scratchpad' memory. These settings are not written into non-volatile memory immediately. This is because a batch of such changes should not be activated one by one, but as part of a complete scheme. Once the complete scheme has been stored in DRAM, the batch of settings can be committed to the non-volatile memory where they will become active.

4.4.3 INTERFACES

The settings and measurements database must be accessible from all of the interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each of the interfaces (LCD display, keypad and all the communications interfaces).

4.5 PROTECTION AND CONTROL FUNCTIONS

The protection and control software processes all of the protection elements and measurement functions. To achieve this it has to communicate with the system services software, the platform software as well as organise its own operations.

The protection task software has the highest priority of any of the software tasks in the main processor board. This ensures the fastest possible protection response.

The protection and control software provides a supervisory task, which controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

4.5.1 ACQUISITION OF SAMPLES

After initialization, the protection and control task waits until there are enough samples to process. The acquisition of samples on the main processor board is controlled by a ‘sampling function’ which is called by the system services software.

This sampling function takes samples from the input module and stores them in a two-cycle FIFO buffer. The sample rate is 24 samples per cycle. This results in a nominal sample rate of 1,200 samples per second for a 50 hz system and 1,440 samples per second for a 60 Hz system. However the sample rate is not fixed. It tracks the power system frequency as described in the next section.

4.5.2 FREQUENCY TRACKING

The device provides a frequency tracking algorithm so that there are always 24 samples per cycle irrespective of frequency drift. The frequency range in which 48 samples per second are provided is between 45 Hz and 66 Hz. If the frequency falls outside this range, the sample rate reverts to its default rate of 1,200 Hz for 50 Hz or 1,440 Hz for 60 Hz.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals. It works by detecting a change in the signal’s measured phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module, in order to achieve a constant sample rate per cycle of the power waveform. The value of the tracked frequency is also stored for use by the protection and control task.

The frequency tracks off any voltage or current in the order VA, VB, VC, IA, IB, IC, down to 10%Vn for voltage and 5%In for current.

4.5.3 DIRECT USE OF SAMPLED VALUES

Most of the IED’s protection functionality uses the Fourier components calculated by the device’s signal processing software. However RMS measurements and some special protection algorithms available in some products use the sampled values directly.

The disturbance recorder also uses the samples from the input module, in an unprocessed form. This is for waveform recording and the calculation of true RMS values of current, voltage and power for metering purposes.

In the case of special protection algorithms, using the sampled values directly provides exceptionally fast response because you do not have to wait for the signal processing task to calculate the fundamental. You can act on the sampled values immediately.

4.5.4 SYSTEM LEVEL SOFTWARE INITIALISATION

The differential protection requires that the devices at the line ends exchange data messages four times per cycle. To achieve this the coprocessor retrieves the frequency-tracked samples at 48 samples per cycle from the input board and converts these to 8 samples per cycle based on the nominal frequency. The coprocessor calculates the Fourier transform of the fixed rate samples after every sample, using a one-cycle window. This generates current

measurements eight times per cycle which are used for the differential protection algorithm. These are transmitted to the remote device(s) using the HDLC (high-level data link control) communication protocol.

The coprocessor is also responsible for managing intertripping commands via the communication link, as well as re-configuration instigated from the remote device(s).

Data exchange between the coprocessor board and the main processor board is achieved through the use of shared memory on the coprocessor board. When the main processor accesses this memory, the coprocessor is temporarily halted. After the coprocessor code has been copied onto the board at initialization, the main traffic between the two boards consists of setting change information, commands from the main processor, differential protection measurements and output data.

4.5.5 FOURIER SIGNAL PROCESSING

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. Although some protection algorithms use some Fourier-derived harmonics (e.g. second harmonic for magnetizing inrush), most protection functions are based on the Fourier-derived fundamental components of the measured analog signals. The Fourier components of the input current and voltage signals are stored in memory so that they can be accessed by all of the protection elements' algorithms.

The Fourier components are calculated using single-cycle Fourier algorithm. This Fourier algorithm always uses the most recent 24 samples from the 2-cycle buffer.

Most protection algorithms use the fundamental component. In this case, the Fourier algorithm extracts the power frequency fundamental component from the signal to produce its magnitude and phase angle. This can be represented in either polar format or rectangular format, depending on the functions and algorithms using it.

The Fourier function acts as a filter, with zero gain at DC and unity gain at the fundamental, but with good harmonic rejection for all harmonic frequencies up to the nyquist frequency. Frequencies beyond this nyquist frequency are known as alias frequencies, which are introduced when the sampling frequency becomes less than twice the frequency component being sampled. However, the Alias frequencies are significantly attenuated by an anti-aliasing filter (low pass filter), which acts on the analog signals before they are sampled. The ideal cut-off point of an anti-aliasing low pass filter would be set at:

$$(\text{samples per cycle}) \times (\text{fundamental frequency})/2$$

At 24 samples per cycle, this would be nominally 600 Hz for a 50 Hz system, or 720 Hz for a 60 Hz system.

The following figure shows the nominal frequency response of the anti-alias filter and the Fourier filter for a 24-sample single cycle fourier algorithm acting on the fundamental component:

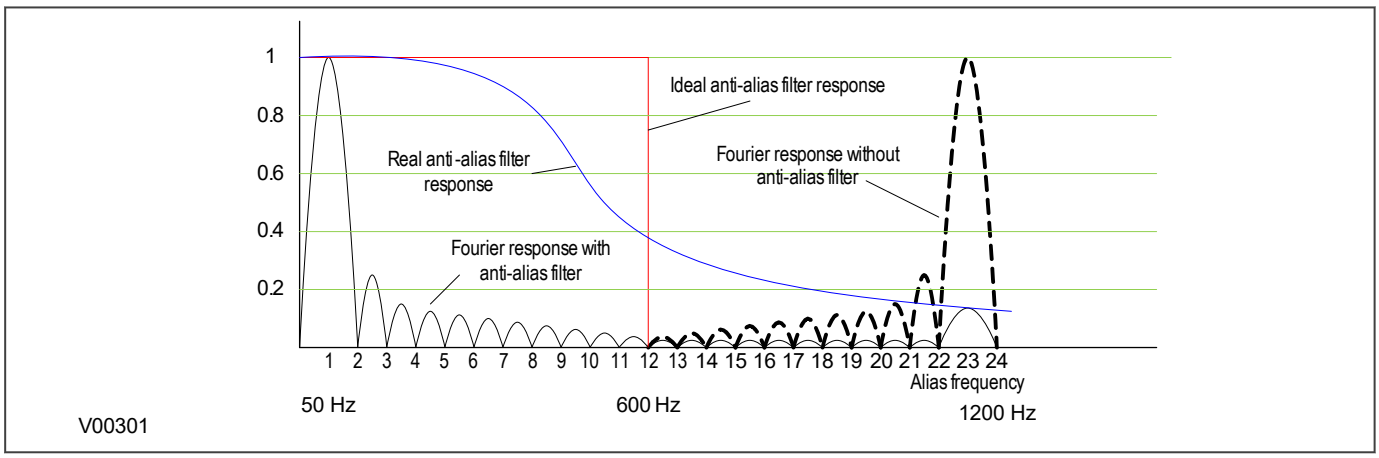


Figure 33: Frequency Response (indicative only)

4.5.6 PROGRAMMABLE SCHEME LOGIC

The purpose of the programmable scheme logic (PSL) is to allow you to configure your own protection schemes to suit your particular application. This is done with programmable logic gates and delay timers. To allow greater flexibility, different PSL is allowed for each of the four setting groups.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed protection scheme logic (FSL). The fixed scheme logic provides the standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay, and/or to condition the logic outputs, such as to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven. The logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection & control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

The PSL can be configured to create very complex schemes. Because of this PSL design is achieved by means of a PC support package called the PSL Editor. This is available as part of the settings application software MiCOM S1 Agile.

4.5.7 EVENT RECORDING

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to indicate that an event is available to be processed and writes the event data to a fast buffer controlled by the supervisor task. Up to 5000 time-tagged event records can be stored.

When the supervisor task receives an event record, it instructs the platform software to create the appropriate log in non-volatile memory (DRAM). The operation of the record logging to Flash is slower than the supervisor buffer. This means that the protection software is not delayed waiting for the records to be logged by the platform software. However, in the rare case when a large number of records to be logged are created in a short period of time, it is possible that some will be lost, if the supervisor buffer is full before the platform software is able to create a new log in Flash memory. If this occurs then an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner, with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem.

For more information, see the Monitoring and Control chapter.

4.5.8 DISTURBANCE RECORDER

The disturbance recorder operates as a separate task from the protection and control task. It can record the waveforms for up to 30 calibrated analogue channels and values of up to 32 digital signals all at a high resolution of 24 samples/cycle. The recording time is user selectable. Typically, 100 waveforms of 10.5 seconds duration can be stored. The disturbance recorder is supplied with data by the protection and control task once per cycle. The disturbance recorder collates the data that it receives into the required length disturbance record. The disturbance records can be extracted by settings application software such as S1 Agile, which can also store the data in COMTRADE format, therefore allowing the use of other packages to view the recorded data.

For more information, see the Monitoring and Control chapter.

4.5.9 FUNCTION KEY INTERFACE

The function keys interface directly into the PSL as digital input signals. A change of state is only recognized when a key press is executed on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed. It can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up thus allowing the function key state to be reinstated after power-up, should power be inadvertently lost.

CHAPTER 5

CONFIGURATION

5.1 CHAPTER OVERVIEW

Each product has different configuration parameters according to the functions it has been designed to perform. There is, however, a common methodology used across the entire product series to set these parameters.

Some of the communications setup cannot be carried out using the settings applications software, it can only be carried out using the HMI. This chapter includes concise instructions on how to configure the device, as well as a description of the common methodology used to configure the device in general.

This chapter contains the following sections:

Chapter Overview 78

Settings Application Software 79

Using the HMI Panel 80

5.2 SETTINGS APPLICATION SOFTWARE

To configure this device, you will need to use the Settings Application Software. The settings application software used in this range of IEDs is called MiCOM S1 Agile. It is a collection of software tools, which is used for setting up and managing the IEDs.

Although you can change many settings using the front panel HMI, some of the features cannot be configured without the Settings Application Software. For example, the programmable scheme logic, or the IEC 61850 communications or the SLD.

If you do not already have a copy of the Settings Application Software, you can obtain it from GE Vernova contact centre.

To configure your product, you will need a data model that matches your product. When you launch the Settings Application Software, you will be presented with a panel that allows you to invoke the “Data Model Manager”. This will close the other aspects of the software to allow an efficient import of the chosen data model. If you don’t have, or can’t find, the data model relating to your product, please call the GE Vernova contact centre.

When you have loaded all the data models you need, you should restart the Settings Application Software and start to create a model of your system using the “System Explorer” panel.

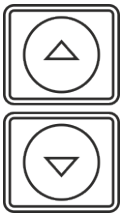
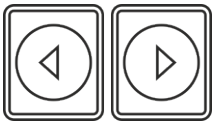
The software is designed to be intuitive, but help is available in an online help system and in the Settings Application Software user guide P40-M&CR-SAS-UG-EN-n, where 'Language' is a 2-letter code designating the language version of the user guide and 'n' is the latest version of the settings application software.

5.3 USING THE HMI PANEL

Using the Graphical HMI, you can:

- Display and modify settings
- Display measurements
- Display fault records
- Display the Single Line Diagram (SLD)
- View the digital I/O signal status
- Reset fault and alarm indications

The keypad provides full access to the device functionality using a range of menu options. The information is displayed on the screen.

Keys	Description	Function
	Up and down cursor keys	To change between settings in a particular column, changing values within a cell or to select the next item on the SLD
	Left and right cursor keys	To change between settings in a particular column, change values within a cell or to select the next item on the SLD
	ENTER/OK key	For changing and executing settings. When a bottom banner Menu context key label is selected, the OK key can also be used to navigate between pages.
	Menu context keys	Menu context keys situated directly below the graphical HMI are used to navigate between pages.
	Cancel/Reset key	To return to the menu header from any menu cell, or to cancel a setting input.
	Read/Home key	To navigate to the default Home page from anywhere in the menu.
	Function keys (not all models)	For executing user programmable functions

Keys	Description	Function
	Control key OPEN	Control key OPEN used to open the CB/Switch. **Note:** Colour coding is selectable via labels and configuration of PSL/SLD.
	Control key CLOSE	Control key CLOSE used to close the CB/Switch. **Note:** Colour coding is selectable via labels and configuration of PSL/SLD.
	Local/Remote key	To select between local and remote operating modes.

5.3.1 NAVIGATING THE HMI PANEL

The cursor keys are used to navigate the menu. To navigate between different menus, use the Menu context keys, which are located below the graphical display.

The cursor keys have an auto-repeat function if held down continuously. This can be used to speed up both setting value changes and menu navigation. The longer the key is held down, the faster the rate of change or movement.

5.3.2 GETTING STARTED

When you first start the IED, it will go through its power up procedure. After a few seconds it will settle down into the default display. If there are alarms present, the yellow Alarms LED will be flashing and the alarm counter on the top banner will show the number of alarms that are active.

The device should be in full working order when you first start it, but an alarm could still be present. For example, if there is no network connection for a device fitted with a network board. If this is the case, you can read the alarm by selecting the Alarm counter on the top banner of the display.

If the device is fitted with an Ethernet board, you will need to connect the device to an active Ethernet network to clear the alarm.

5.3.3 DEFAULT DISPLAY

The graphical HMI default display contains shortcuts to various sections of the menu, as well as a snapshot of the current device status.

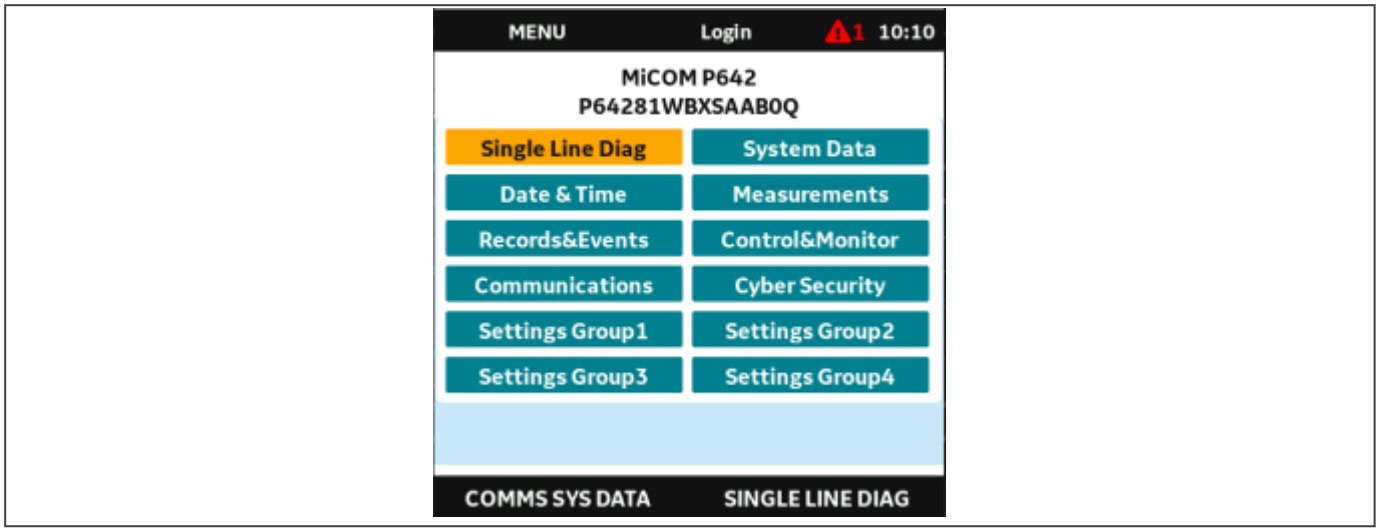


Figure 34: HMI default display

The graphical display screen consists of three main areas, which can be selected using the navigation keypad.

1. The top banner displays information left to right and includes the menu label for the current display, the user access level, the number of active alarms and the time.
2. The content area displays information related to the chosen area of navigation. For example, settings, measurements or SLD.
3. The bottom banner displays labels for the two Menu context keys, which are used for navigating between the menus.

Note:
After a period defined by the "LCD screen saver" , setting the HMI will enter rest mode. This allows the HMI to reduce power consumption and will dim the LCD backlight. The HMI may be woken from rest mode by pressing any front panel key. This mode has no effect on IED functional performance.

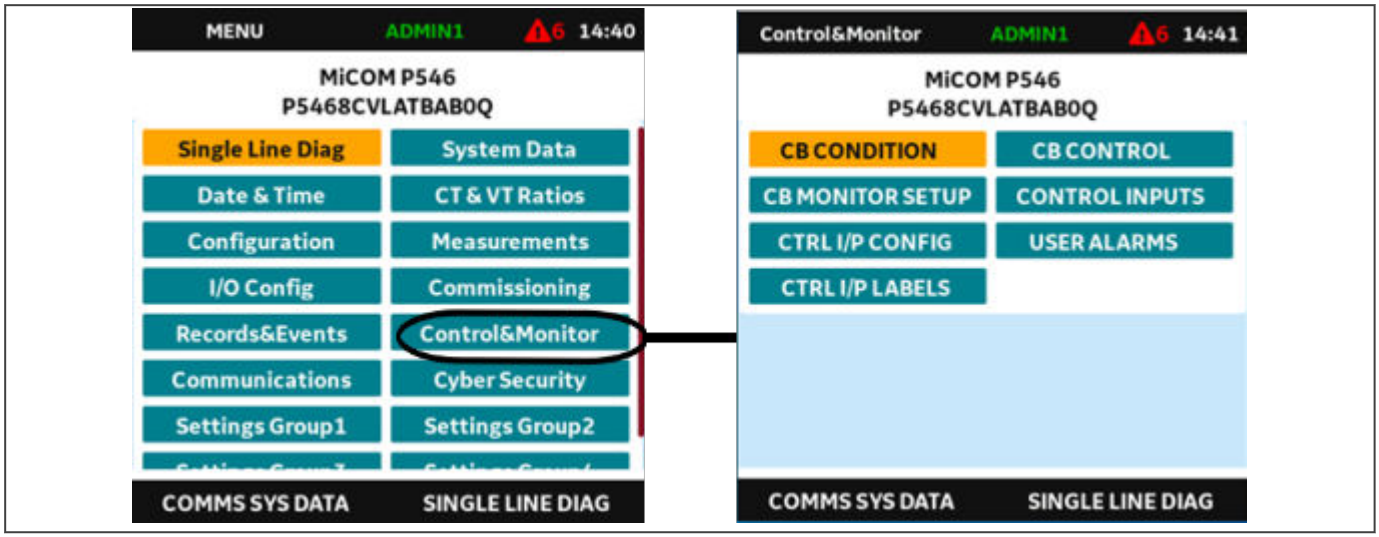
5.3.4 DEFAULT DISPLAY NAVIGATION

The default display provides quick and simple navigation of the complete menu database. Use the navigation keypad to change the highlighted cell. The highlighted entry can be selected using the Enter/OK Key. When the bottom of the screen is reached, the selected area moves to the Bottom Banner. From here the OK key can also be used to navigate between the pages.

The Menu view can be directly navigated to by long pressing the "Read/Home" key.

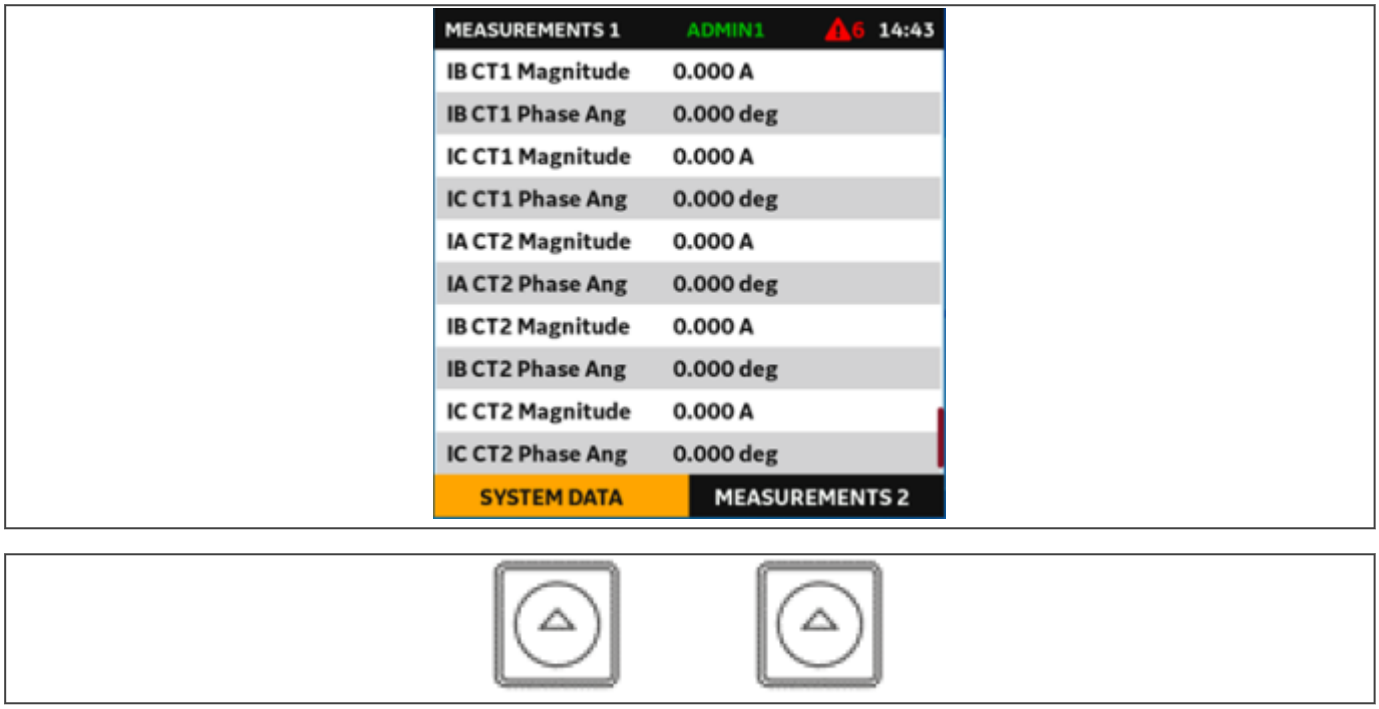
Previous level in the navigation hierarchy may be reached by pressing the "Cancel/Reset" key.

From the HMI Default Display, you can navigate to the required view or open up a Submenu using hierarchical navigation. For example, by selecting Controls & Monitor, a Submenu is opened.



As an alternative to hierarchical navigation, the views may be navigated to in sequence by using the hot keys as “Next” and “Previous” buttons, and is referred as horizontal navigation.

For example, you can move to either ***SYSTEM DATA*** or ***MEASUREMENTS 2*** Views using the horizontal navigation, menu contexts hot keys situated directly under the screen.



5.3.5 PROCESSING ALARMS AND RECORDS

When there are no alarms, the Alarm Icon on the top banner is shown as:

While there are any standing alarms, the standing alarm count will be highlighted in red in the top HMI banner and the yellow alarm LED will flash.

To launch the alarm list view, select the alarm counter in the HMI top banner and press the **OK** key. The alarm view list may be scrolled to view all alarms.

New standing and fleeting alarms may be accepted by selecting the alarm and pressing the **Ack/Clear** menu context key. Rescinded alarms may also be cleared by selecting the alarm and pressing the **Ack/Clear** menu context key.

All visible alarms may be selected by pressing the **Select All** menu context key.

The "*reset indication*" command may be issued to reset latched alarms and accept the flashing led notification. A "*reset indication*" may be issued from the "*View Records*" HMI settings view or by pressing **Ack/Clear** alarm context key.

"*Ack/Clear*" and "*reset indication*" commands are available to users with ENGINEER or OPERATOR or INSTALLER roles.

To return to the launch view from the alarm view press the **Cancel** key.

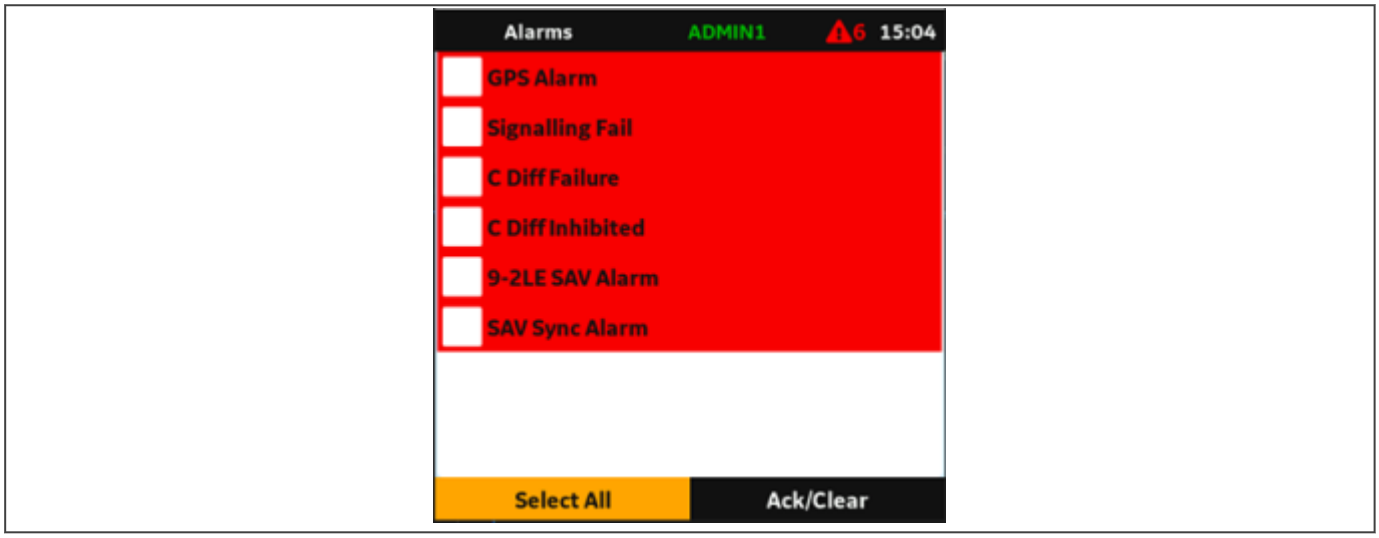


Figure 35: HMI Alarms Display

5.3.6 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

5.3.6.1 CIRCUIT BREAKER CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the circuit breaker selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the ***CB Control by*** setting is selected, to option 1 *Local*, option 3 *Local+Remote*, option 5 *Opto+local*, option 7 *Opto+Rem+local* or option 8 *L/R Key* in the *CB CONTROL* column users are allowed to use the Trip and Close Key on the front panel to operate the CB.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***CB control by*** setting to *L/R Key*
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R

Key LED is green and the REMOTE mode is selected. ***The L/R Key Status*** DDB status is stored in non-volatile memory, so that it's status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant which you require to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the Open or Close key to operate

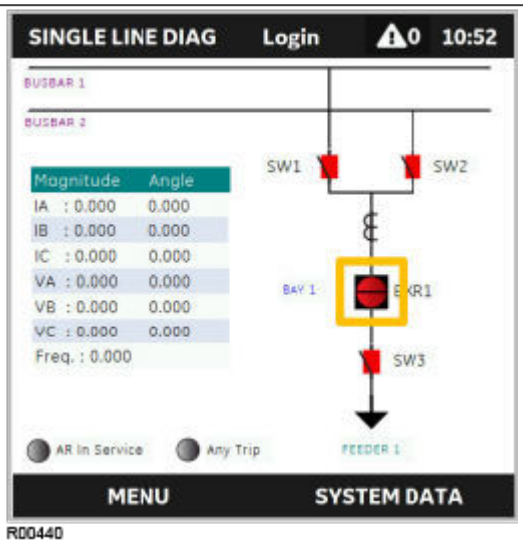


Figure 36: HMI SLD Display

For the Circuit Breaker Commands from HMI, additional checks are done:

If the CB is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "Control by" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "Control by" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "Control by" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - In Remote Control".

If the associated local DDB is set to local, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

5.3.6.2 SWITCH CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the switches selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the Switch Control by setting is selected to option 1 *LOCAL*, option 3 `Local+Remote` or option 4 `L/R Key` in the SWITCH CONTROL column, users are allowed to use the Open and Close Key on the front panel to operate the SWITCH.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***Switch Control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R

Key LED is green and the REMOTE mode is selected. The **L/R Key Status** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant you want to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the OPEN or CLOSE key to operate

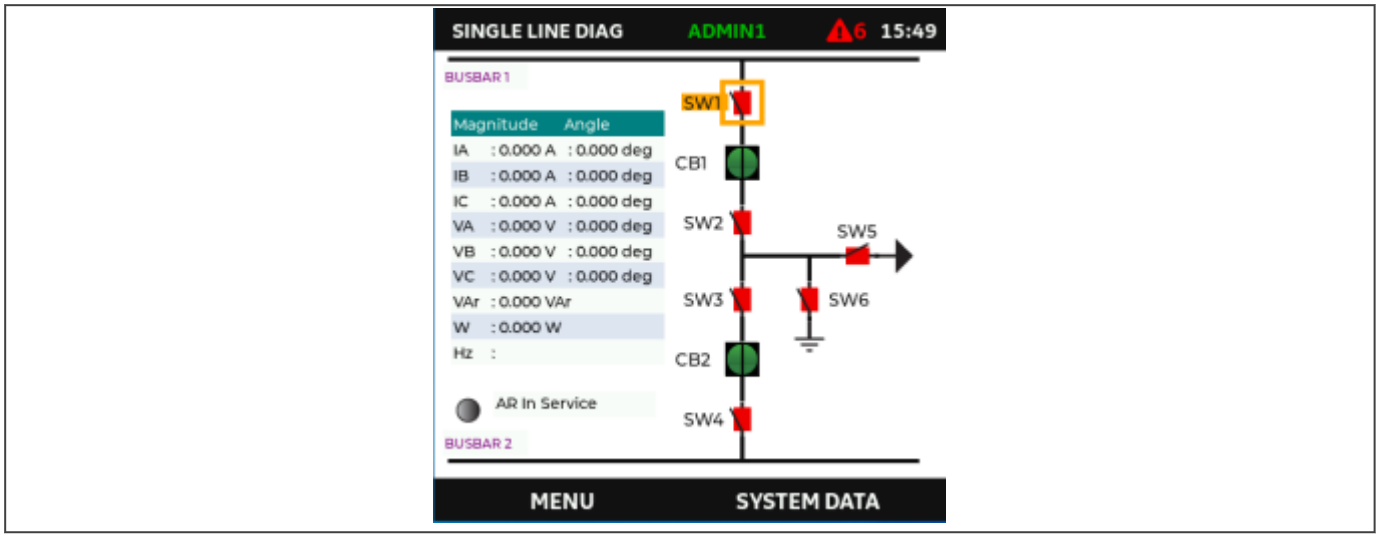


Figure 37: HMI SLD display

Figure 38: For the Switch Commands from HMI, these additional checks are done:

If the Switch is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "***Control by***" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - In Remote Control."

If the associated local DDB is set to local, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

5.3.7 MENU STRUCTURE

Settings, commands, records and measurements are stored in a local database inside the IED. When using the Human Machine Interface (HMI) it is convenient to visualise the menu navigation system as a table. Each item in the menu is known as a cell, which is accessed by reference to a column and row address. Each column and row is assigned 2-digit hexadecimal numbers, resulting in a unique 4-digit cell address for every cell in the database. The main menu groups are allocated columns and the items within the groups are allocated rows, meaning a particular item within a particular group is a cell.

You do not need to scroll through each of the columns horizontally to access a specific setting view. The ‘Home Page’ can be used to quickly access the required column/setting view. Each column contains all related items, for example all of the disturbance recorder settings and records are in the same column.

There are three types of cell:

- Settings: this is for parameters that can be set to different values
- Commands: this is for commands to be executed
- Data: this is for measurements and records to be viewed, which are not settable

Note:
Sometimes the term "Setting" is used generically to describe all of the three types.

The table below, provides an example of the menu structure:

SYSTEM DATA (Col 00)	VIEW RECORDS (Col 01)	MEASUREMENTS 1 (Col 02)	…
Language (Row 01)	"Select Event [0...n]" (Row 01)	IA Magnitude (Row 01)	…
Password (Row 02)	Menu Cell Ref (Row 02)	IA Phase Angle (Row 02)	…
Sys Fn Links (Row 03)	Time & Date (Row 03)	IB Magnitude (Row 03)	…
…	…	…	…

It is convenient to specify all the settings in a single column, detailing the complete Courier address for each setting. The above table may therefore be represented as follows:

Setting	Column	Row	Description
SYSTEM DATA	**00**	**00**	**First Column definition**
Language (Row 01)	00	01	First setting within first column
Password (Row 02)	00	02	Second setting within first column
Sys Fn Links (Row 03)	00	03	Third setting within first column
…	…	…	
VIEW RECORDS	**01**	**00**	**Second Column definition**
Select Event [0...n]	01	01	First setting within second column
Menu Cell Ref	01	02	Second setting within second column
Time & Date	01	03	Third setting within second column
…	…	…	
MEASUREMENTS 1	**02**	**00**	**Third Column definition**
IA Magnitude	02	01	First setting within third column
IA Phase Angle	02	02	Second setting within third column
IB Magnitude	02	03	Third setting within third column
…	…	…	

The first three column headers are common throughout much of the product ranges. However, the rows within each of these column headers may differ according to the product type. Many of the column headers are the same for all products within the series. However, there is no guarantee that the addresses will be the same for a particular column header. Therefore, you should always refer to the product settings documentation and not make any assumptions.

5.3.8 DIRECT ACCESS (MENU CONTEXT KEYS)

The IED provides a pair of menu context keys directly below the LCD display, which allows scrolling between column headings (navigation between menu screens). These keys can be pressed at any time during menu navigation to quickly access the menu label displayed in the bottom banner of the graphical HMI.

5.3.8.1 CONTROL INPUTS

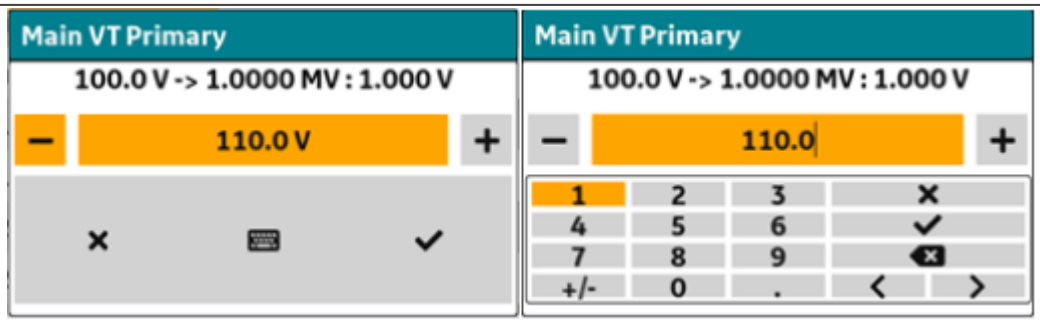
Control inputs cannot be operated through the Menu context keys. To operate control inputs, navigate to the Control Inputs settings view on the front graphical HMI screen, select the relevant control input and Set/Reset as required. RBAC is now applied to access control inputs for operation.

5.3.9 CHANGING THE SETTINGS

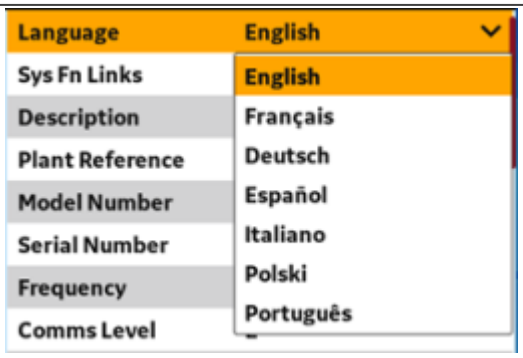
Appropriate user authority or bypass access is required to change the Settings. Please refer to the Cyber Security chapter for user authority details.

- Starting at the default display, highlight the required settings column/menu
- Use the OK key to enter the highlighted settings menu.
- To change the value of a setting, highlight the relevant cell in the menu, then press the **Enter** key to change the cell value. A settings screen will appear next to the cell. If the currently logged in user does not have the level of access required for changing the setting, a pop-up dialog box will inform the user and prevent the settings from being changed. Acknowledge the pop-up message, then navigate to the 'user accounts' section to the top of the screen (top banner) to enter the password for the required access level to change settings.
- To change the value on the settings screen, use the cursor keys to change the desired settings. When more settings are available than can fit on the screen, a scroll bar on the right-hand side appears. In some cases, a virtual keyboard is provided to enter complex characters. The IED maintains dependencies between various settings, and only the applicable settings are displayed for changing.

For Analog Value update, the new analogue value may be entered by selecting the +ve and -ve step buttons or free-form numerals entered by virtual keyboard.

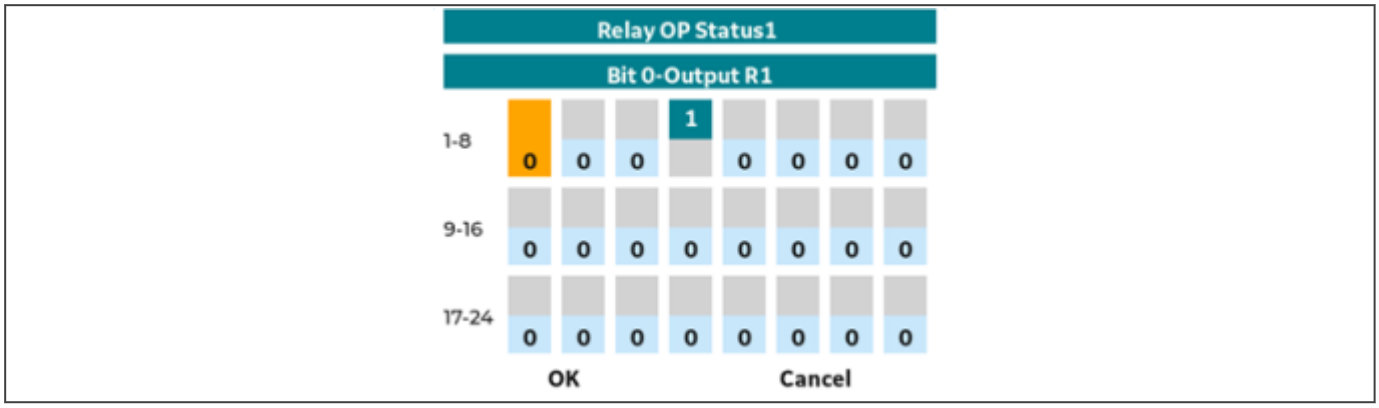


If the setting cell has the facility of drop down, the required setting can be selected from the drop down list.

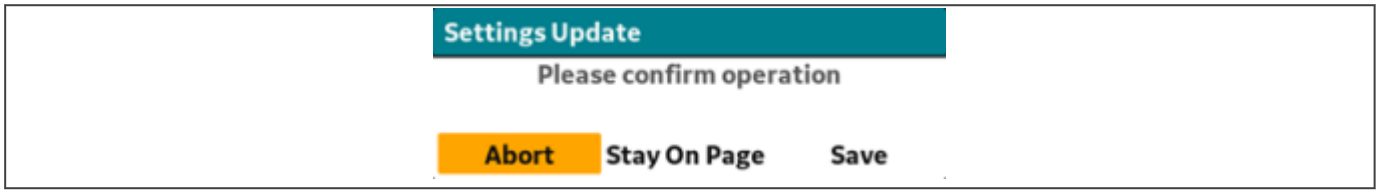


Some of the settings are in the form of Binary Data Bits update. By selecting each of the Bit position the data can be toggled.

Note:
Binary Data Bits can also be used to verify the present data of each bits for monitoring purpose.



- Press the **Enter** key to confirm the new setting value or the **Clear** key or the on-screen 'x' to discard it.
- To confirm the new settings, press the **Enter** key. Navigate away from the currently active group settings or press the **Home** key. A Settings update confirmation dialogue box will appear that requires choosing of one of the following options:
- Save - accept all settings including the recently changed settings
- Abort - discard recent changes and keep existing settings
- Stay on page - return to the active settings page without saving recent changes



- To return to the top of the menu, hold down the **Up** cursor key for a second or so, or press the **Clear** key once. It is possible to move across columns from anywhere in the menu by using the Menu context keys at the bottom of the display.
- To return to the default display, press the **Home** key at any time.
- Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.
- The Date and time can be adjusted by navigating to the top banner and selecting the displayed time. Press the **Enter** key to adjust the date and time using the calendar/clock widget that pops up.

Note:
For the protection group and disturbance recorder settings, the changes are not saved unless confirmed using the Settings update confirmation prompt.

Note:
All other Control and support settings (such as Communications and Control inputs), however, are updated immediately after they are entered on the front HMI without the need to confirm using the Settings update confirmation prompt.

5.3.10 FUNCTION KEYS

Most products have a number of function keys for programming control functionality using the programmable scheme logic (PSL).

Each function key has an associated programmable tri-colour LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are in the *FUNCTION KEYS* column.

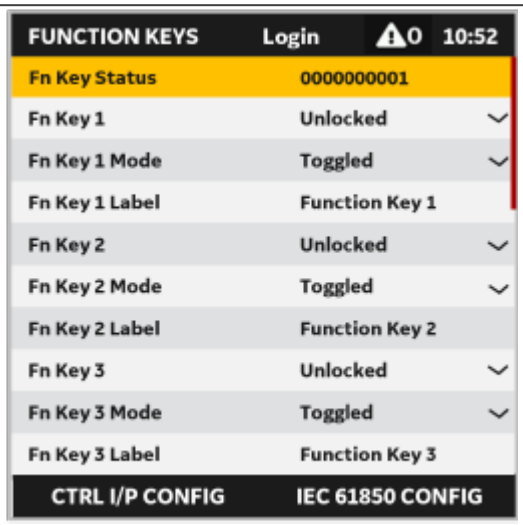


Figure 39: HMI Function Keys Display

The first cell down in the *FUNCTION KEYS* column is the ***Fn Key Status*** cell. This contains a binary string, which represents the function key commands. Their status can be read from the binary string.

The next cell down (***Fn Key 1***) allows you to activate or disable the first function key (1). The ***Lock*** setting allows a function key to be locked. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state, preventing any further key presses from deactivating the associated function. Locking a function key that is set to the Normal mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

The next cell down (***Fn Key 1 Mode***) allows you to set the function key to `Normal` or `Toggled`. In the Toggle mode the function key DDB signal output stays in the set state until a reset command is given, by activating the function key on the next key press. In the Normal mode, the function key DDB signal stays energised for as long as the function key is pressed then resets automatically. If required, a minimum pulse width can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The next cell down (***Fn Key 1 Label***) allows you to change the label assigned to the function. The default label is `Function key 1` in this case. To change the label you need to press the enter key and then change the text on the bottom line, character by character. This text is displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

Subsequent cells allow you to carry out the same procedure as above for the other function keys.

The status of the function keys is stored in non-volatile memory. If the auxiliary supply is interrupted, the status of all the function keys is restored. The IED only recognises a single function key press at a time and a minimum key press duration of approximately 200 ms is required before the key press is recognised. This feature avoids accidental double presses.

The function keys needs operator permissions to operate. If operator permissions are not held by the present user an information dialogue is raised to inform the operation has failed.

5.3.10.1 VISUALISATION OF PROTECTION OPERATION

Where there is a protection operation/trip, in addition to the front panel LED indications, the standing trip is indicated on the LCD screen by a red trim around the top banner. Additionally, the LCD backlight becomes lit and a dialogue is presented with three options:

- “OK” - close the dialogue
- “View” - Navigate to the “record” data view and open the latest fault record
- “Reset Ind” - Attempt to reset the trip indication

CHAPTER 6

TRANSFORMER DIFFERENTIAL PROTECTION

6.1 CHAPTER OVERVIEW

This chapter contains the following sections:

Chapter Overview 94
Transformer Differential Protection Principles 95
Implementation 103
Harmonic Blocking 115
Application Notes 119

6.2 TRANSFORMER DIFFERENTIAL PROTECTION PRINCIPLES

Transformer Differential Protection (87T) uses the well-known current differential principle where current entering the protected equipment is compared with the current leaving the protected equipment. If there is no fault, the current entering the transformer will be equal to the current leaving the transformer multiplied by the inverse of the turns ratio. If there is a fault in the transformer zone, the currents will not be equal, which results in a differential current. This differential current is proportional to the fault current for internal faults, but approaches zero for any other operating conditions. The IED trips the circuit breakers protecting the transformer when it detects a minimum level of differential current.

The differential scheme creates a well-defined protection zone between the CT sets protecting the transformer. Any fault within the differential protection zone is called an internal fault, while any fault outside the differential protection zone is called an external fault. The protection should operate only for internal faults and be sensitive to low fault currents. It should also restrain on the highest prospective external faults, providing the CTS accurately reproduce the primary currents. This is difficult to achieve in practice because the CTs never have identical saturation characteristics. This will result in a differential current, which could cause undesirable operation.

An external fault, which causes a high current to flow through the transformer, is called a through fault. The through-fault current will usually be high enough to saturate the CTs. The differences in the saturation characteristics of the CTs will cause a differential current, which could cause the device to trip unless it is restrained. The term used to specify the IED's ability to cope with these imperfections is called Through Fault Stability.

CT saturation is not the only cause of undesirable differential current. Other aspects which need to be considered by the transformer differential element to avoid maloperation are:

- Phase shift between the transformer primary and secondary currents depending on the vector group
- Transformation ratio
- The zero-sequence current, which flows in the grounded star transformer winding or the grounding transformer within the differential protection zone
- Tap changer operation to adjust the voltage
- Magnetising inrush current that flows immediately after the transformer energisation or during a voltage recovery after the clearance of an external fault or when a second transformer is paralleled with the already energised transformer
- Over excitation of the transformer

6.2.1 THROUGH FAULT STABILITY

In an ideal world, the CTs either side of a differentially protected system would be identical with identical characteristics to avoid creating a differential current. However, in reality CTs can never be identical, therefore a certain amount of differential current is inevitable. As the through-fault current in the primary increases, the discrepancies introduced by imperfectly matched CTs is magnified, causing the differential current to build up. Eventually, the value of the differential current reaches the pickup current threshold, causing the protection element to trip. In such cases, the differential scheme is said to have lost stability. To specify a differential scheme’s ability to restrain from tripping on external faults, we define a parameter called ‘through-fault stability limit’, which is the maximum through-fault current a system can handle without losing stability.

6.2.2 BIAS CURRENT COMPENSATION

To prevent maloperation, compensation is needed for the protection to remain sensitive to internal faults but to ignore through faults. This is achieved by applying a proportion of the scalar sum of all the currents entering and exiting the zone. This scalar sum is called bias current.

The bias characteristic changes the operating point of the IED depending on the fault current. At low through-fault currents, the CT performance is more reliable so a low bias current is needed. Less differential current is then needed to trip the circuit breakers, allowing greater sensitivity to internal faults. At high through-fault currents, the

CTs may be close to saturation so a high bias current is needed. More differential current is then needed to trip the circuit breakers, allowing greater security from external faults and less risk of maloperation.

This is achieved by defining an operating current characteristic. Often a triple slope characteristic is used as shown below.

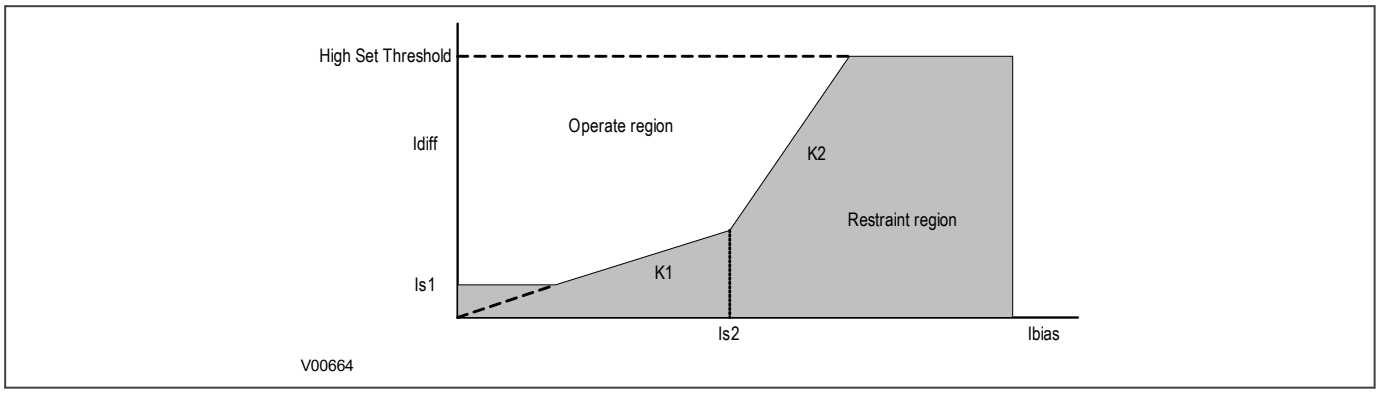


Figure 40: Compensation using biased differential characteristic

Idiff is the differential current, which is the vector sum of all the current inputs. Ibias is a current which is proportional to the scalar sum of all currents entering and leaving the zone. The bias current is used to calculate an operating current. If the differential current calculated by the IED is above the operation current, then the device will trip (providing no blocking signals are asserted).

The characteristic can be defined by setting certain parameters such as the minimum operating current Is1 (Iset 1), Is2 (Iset 2), K1 and K2. Is1 sets the minimum operating current. Is2 sets the level of bias current at which the steeper slope sets in. Constants K1 and K2 define the slopes. A High Set Threshold is usually defined, which ensures the device will operate for very high currents, even if blocking signals are present.

The slope parts of the characteristic curve provide stability for external faults that cause CT saturation. The high bias current region of the characteristic curve has a steeper slope than the low bias current region in order to improve the stability even further for high-current external faults. The first slope, K1, compensates for CT errors and tap changer errors. The second slope, K2, compensates for CT saturation. Is1 should be set above transient overfluxing and Is2 should be considered as the transformer full load current. The CTs are sized according to the transformer full load current.

6.2.3 THREE-PHASE TRANSFORMER CONNECTION TYPES

There are two ways of connecting a three-phase transformer winding:

- Star-connected (sometimes known as Y, or Wye)
- Delta-connected (sometimes known as Δ or D)

In some transformers, the windings are split at the centre point and terminals are brought out so that they can also be interconnected. These windings can be zig-zag connected (Z-connected).

The more common connection types are:

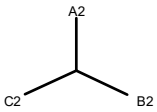
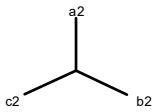
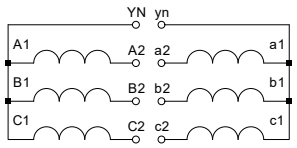
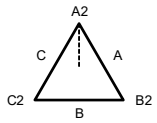
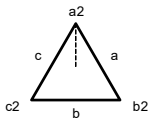
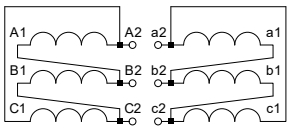
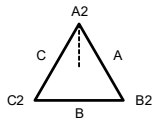
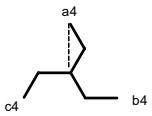
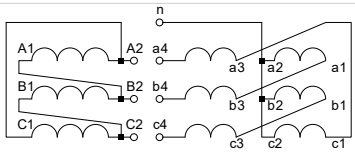
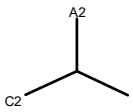
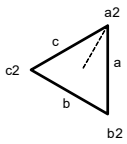
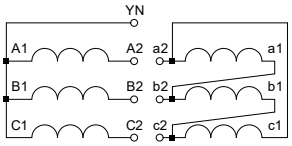
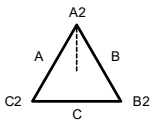
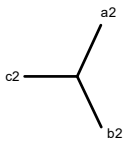
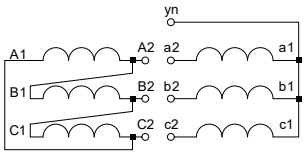
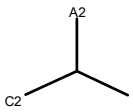
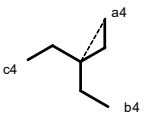
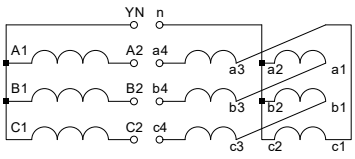
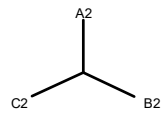
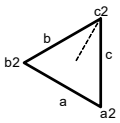
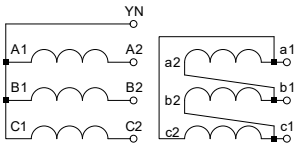
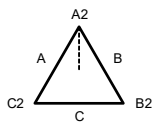
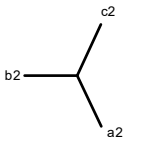
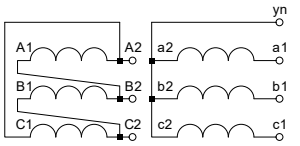
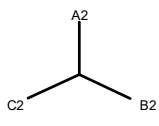
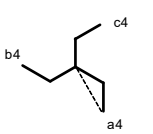
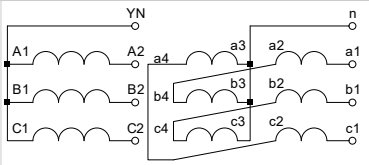
- Y-y
- Y-d
- Y-z
- D-d
- D-y
- D-z

To differentiate between the low and high voltage sides of the transformer, a standard convention has been adopted whereby lower case is used for the low voltage side and upper case is used for the high voltage side.

Not only can the primary and secondary be connected as a star or a delta, each phase can also be reversed resulting in a large choice of possible connections. In reality, however, only a few of these are used, because we generally require that the phase shifts between the primary windings and their secondary counterparts be consistent. This reduces the common connection types to those shown in the table below.

You will notice that the naming convention specifying the connection type in the first column also has a number appended to it. This number, called the clock face vector, or vector group number represents the phase shift between the current in a low voltage winding with respect to its counterpart on the high voltage winding. This corresponds to the position of the number of a standard clock face. The table and diagram below shows examples of connections with the clock vectors Midnight, 1 o' clock, 6 o' clock and 11 o'clock, which is equivalent to a phase shift of 0°, -30°, -180° and +30° respectively.

Vector Group	Phase Shift
Yy0	0°
Dd0	0°
Dz0	0°
Yd1	-30°
Dy1	-30°
Dz1	-30°
Yd5	-150°
Dy5	-150°
Dz5	-150°
Yy6	180°
Dd6	180°
Dz6	180°
Yd11	+30°
Dy11	+30°
Dz11	+30°

Type	HV winding	LV winding	Winding Connection	Phase Shift
Yy0				**0°**
Dd0				**0°**
Dz0				**0°**
Yd1				**-30°**
Dy1				**-30°**
Yz1				**-30°**
Yd5				**-150°**
Dy5				**-150°**
Yz5				**-150°**

V03125

Figure 41: Transformer winding connections - part 1

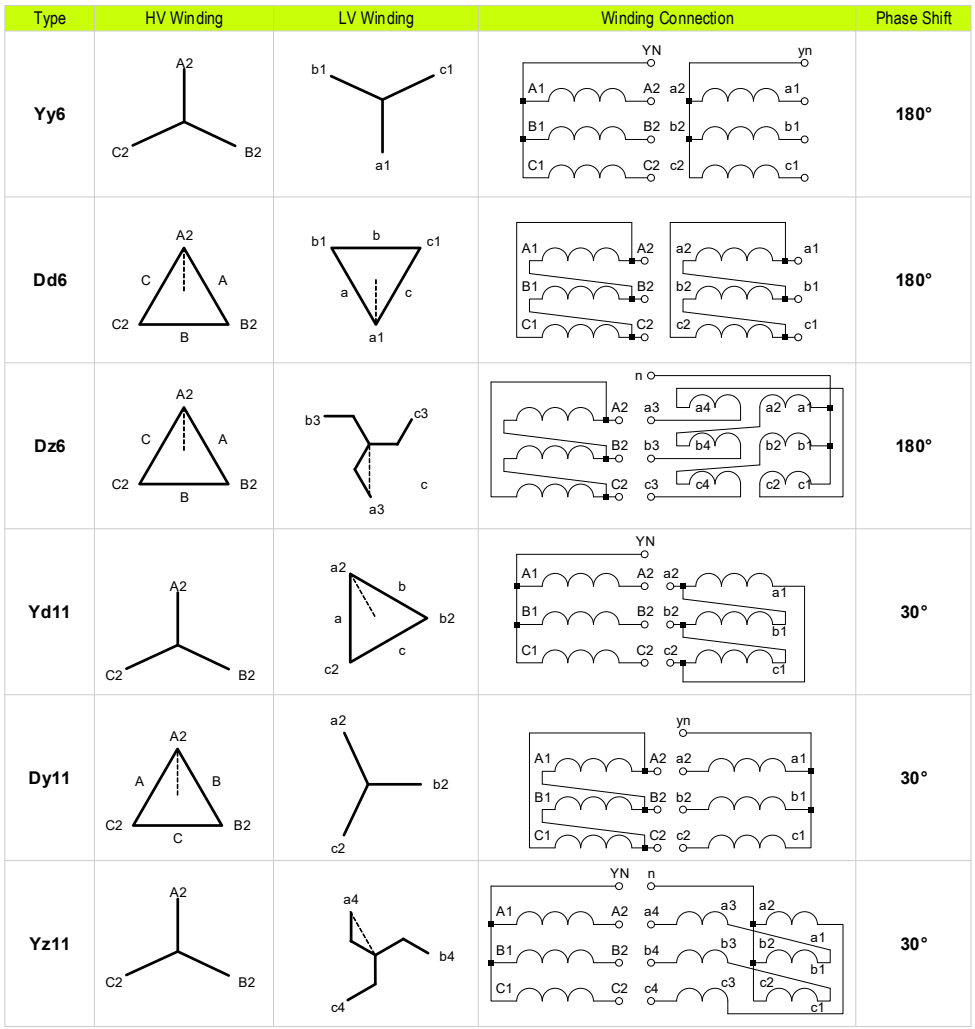


Figure 42: Transformer winding connections - part 2

6.2.4 PHASE AND AMPLITUDE COMPENSATION

A power transformer is designed to convert voltages. This means the line currents either side of the transformer are different in magnitude. If identical CTs were used on both sides of the transformer, the differential protection circuit would be unbalanced, causing a differential current. Obviously, this has to be compensated for. Amplitude compensation is theoretically arranged by having a suitable turns ratio on the secondary CT. Ideally, selecting CT ratios that exactly match the inverse of the transformer turns ratio would compensate for the difference in the transformer current magnitudes. However, the CT ratios associated with available CTs typically do not provide exact ratio matching. Also for Y-delta or delta-Y connected transformers, the voltage and current magnitudes used are changed by a factor of $\sqrt{3}$. Further, a phase shift is introduced, meaning the secondary side is out of phase with the primary side. So further amplitude compensation, as well as phase compensation is required.

Before the advent of numerical IEDs, this compensation was achieved by choosing CTs with appropriate turns ratios and connection types, and introducing interposing CTs with appropriate connection types. Of course, having CTs with different turns ratios and connection types on each side of the protected zone exacerbates the CT errors, therefore increasing the need for good through-fault compensation.

With modern IEDs, it is possible to do a great deal of the compensation in software, so simple Y-connected CTs can be used on both sides of the transformer irrespective of the connection types. The CTs are chosen such that their respective turns ratios provide a nominal current usable by the IED (1A or 5A). This in itself provides a certain amount of amplitude compensation, but there will invariably be a CT ratio mismatch. This mismatch is compensated

for by software in the IED. The device calculates suitable values based on the reference power rating, transformer voltage ratings, CT ratios and connection type (star or delta) to scale the secondary currents to a common base.

6.2.5 ZERO SEQUENCE FILTERING

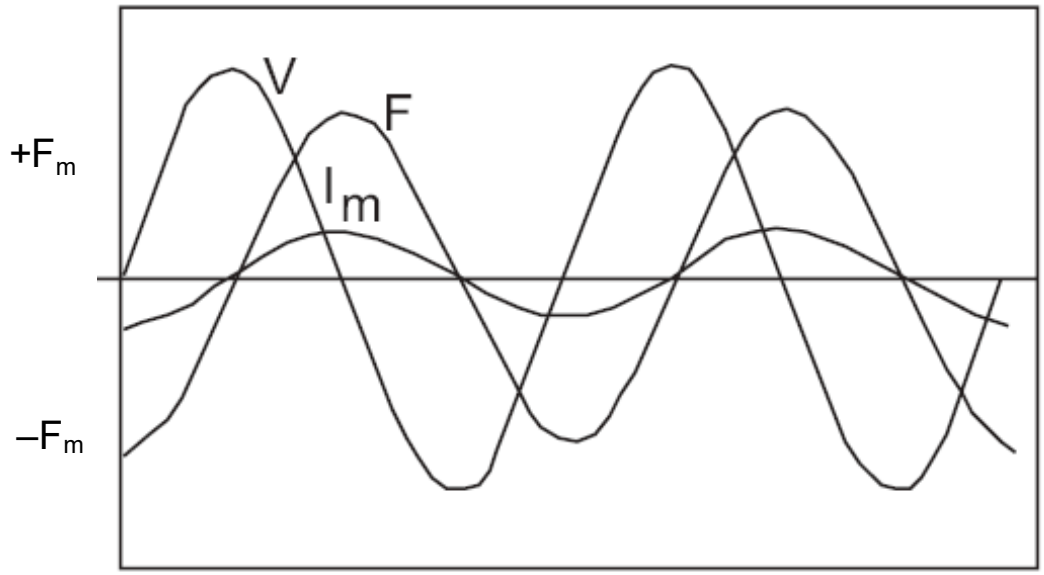
An earth fault in a three-phase system will always produce a zero sequence current component. With earthed Y-connected windings, this zero sequence current flows through the neutral conductor to earth. With delta-connected windings, this zero sequence current component just circulates around the delta connected windings (unless an earthing transformer is used). So in the case of a Y-delta transformer, an external fault will cause zero sequence current to be measured by the Y-side CTs. However, because this zero sequence current is trapped on the delta side, it is not measured by the delta-side CTs. This could cause maloperation if not compensated for. Before the advent of numerical IEDs, this was handled by a configuration involving interposing CTs. Numerical IEDs, however, can do this by filtering out the zero sequence component in software.

6.2.6 MAGNETISING INRUSH RESTRAINT

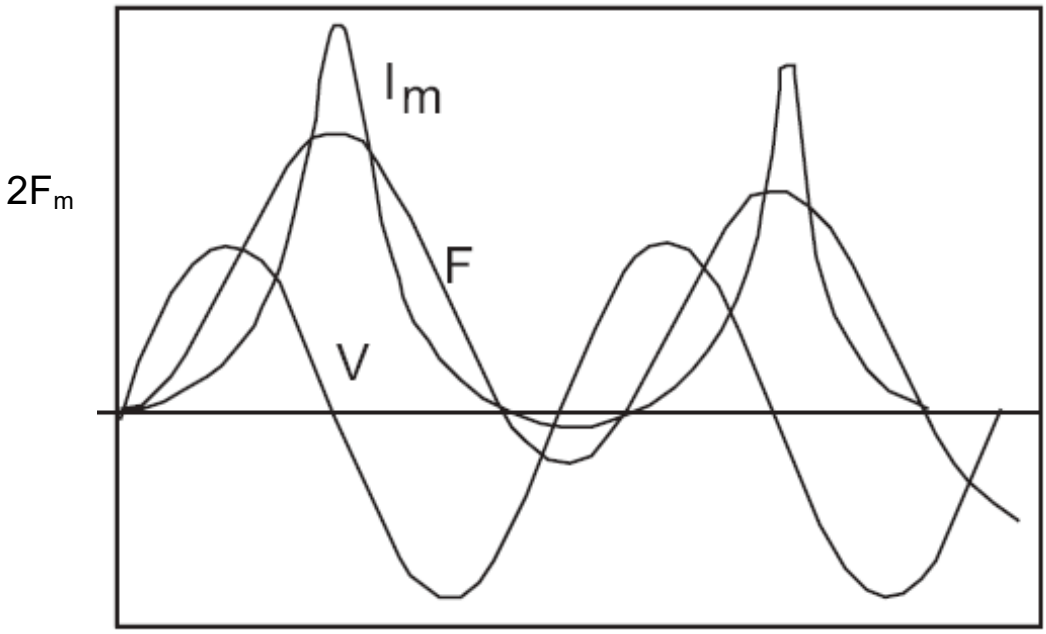
Whenever there is an abrupt change of magnetising voltage (e.g. when a transformer is initially connected to a source of AC voltage), there may be a substantial surge of current through the primary winding called inrush current.

In an ideal transformer, the magnetizing current would rise to approximately twice its normal peak value as well, generating the necessary MMF to create this higher-than-normal flux. However, most transformers are not designed with enough of a margin between normal flux peaks and the saturation limits to avoid saturating in a condition like this, and so the core will almost certainly saturate during this first half-cycle of voltage. During saturation, disproportionate amounts of MMF are needed to generate magnetic flux. This means that winding current, which creates the MMF to cause flux in the core, could rise to a value way in excess of its steady state peak value. Furthermore, if the transformer happens to have some residual magnetism in its core at the moment of connection to the source, the problem could be further exacerbated.

The following figure shows the magnetizing inrush phenomenon:



Steady state



Switch on at voltage Zero – No residual flux

V = Voltage, F = Flux, Im = magnetising current, Fm = maximum flux

E03123

Figure 43: Magnetising inrush phenomenon

The main characteristics of magnetising inrush currents are:

- Higher magnitude than the transformer rated current magnitude
- Containing harmonics and DC offset
- Much longer time constant than that of the DC offset component of fault current

We can see that inrush current is a regularly occurring phenomenon and should not be considered a fault, as we do not wish the protection device to issue a trip command whenever a transformer is switched on at an inconvenient point during the input voltage cycle. This presents a problem to the protection device, because it should always trip

on an internal fault. The problem is that typical internal transformer faults may produce overcurrents which are not necessarily greater than the inrush current. Furthermore, faults tend to manifest themselves on switch on, due to the high inrush currents. For this reason, we need to find a mechanism that can distinguish between fault current and inrush current. Fortunately, this is possible due to the different natures of the respective currents. An inrush current waveform is rich in harmonics, especially 2nd harmonics, whereas an internal fault current consists only of the fundamental. We can therefore develop a restraining method based on the 2nd harmonic content of the inrush current. The mechanism by which this is achieved, is called second harmonic blocking.

6.2.7 OVERFLUXING RESTRAINT

Sometimes the protected transformer is subject to overfluxing due to temporary overloading with a voltage in excess of the nominal voltage, or a reduced voltage frequency. For example, when a load is suddenly disconnected from a power transformer, the voltage at the input terminals of the transformer may rise by 10-20% of the rated value. Since the voltage increases, the flux also increases. As a result, the transformer steady state excitation current becomes higher. The resulting excitation current flows in one winding only and therefore appears as differential current which may rise to a value high enough to operate the differential protection. A typical differential current waveform during such a condition is as follows.

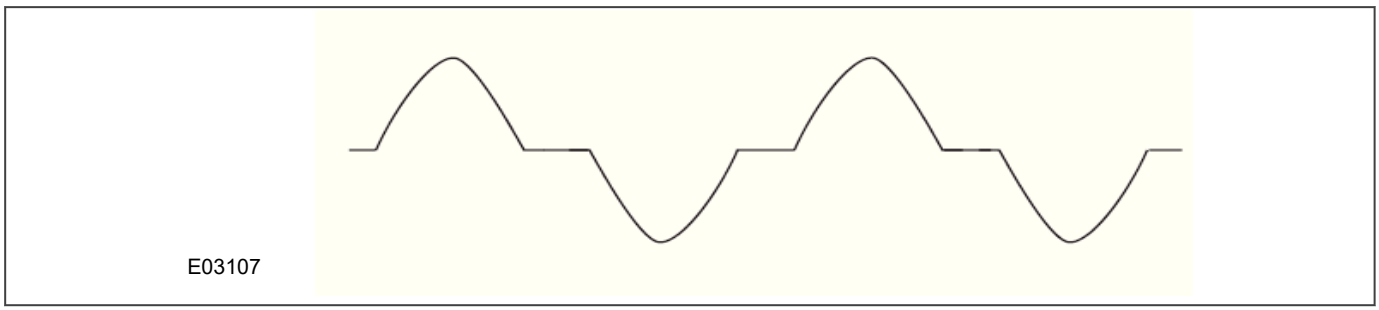


Figure 44: Typical overflux current waveform

Such waveforms have a significant 5th harmonic content. We can therefore develop a restraining method based on the 5th harmonic content of the inrush current. The mechanism by which this is achieved, is called fifth harmonic blocking.

6.3 IMPLEMENTATION

To enable or disable Differential Protection, set ***Diff Protection*** in the *CONFIGURATION* column and ***Trans Diff*** in the *DIFF PROTECTION* column of the of the relevant settings group.

6.3.1 DEFINING THE POWER TRANSFORMER

To set up the transformer differential protection you need to define what type of transformer is being protected. You do this with settings in the *SYSTEM CONFIG* column.

The P642 only supports two-winding transformers. For the P643 and P645, the ***Winding Config*** setting determines whether the power transformer being protected is a two-winding (HV+LV), or a three-winding (HV+LV+TV) transformer.

The ***Winding Type*** setting determines whether the protected transformer is a conventional transformer or an autotransformer.

The ***Ref Power S*** setting sets the reference power of the protected transformer. This is used as a reference by the differential function to calculate the ratio correction factors (which incidentally are displayed in the ***Match Factor CT*** cells. The reference power is the maximum MVA rating specified in the transformer nameplate.

You can define each winding as Y (or Star, or Wye), D (delta), or Z (zigzag) in the settings ***HV connection***, ***LV Connection*** and ***TV connection***.

You also need to set the nominal voltage of each winding. You do this with the settings ***HV Nominal***, ***LV Nominal*** and ***TV Nominal***.

To ensure the device can perform vector group correction, you need to enter the vector groups for the LV and TV windings. You do this by entering the relevant vector group reference (available on the nameplate) using the settings ***LV Vector Group*** and ***TV Vector Group***.

In addition to the ***LV Vector Group*** and ***TV Vector Group*** settings, there is a setting called ***Ref Vector Group***. This setting allows you to apply a phase shift to the HV current inputs. In the majority of cases, this would be set to `0`, but there are some specialist applications where you may wish to set the reference vector group to something other than `0`. An application note at the end of this chapter explains why you would want do to this.

Finally, you need to set the phase sequence with the ***Phase Sequence*** setting. This will be either `standard ABC` or `Reverse ACB`.

If the phase rotation is changed from ABC to ACB, then the vector group settings need to reflect this change accordingly. This can be achieved by setting them to be equal to 12 minus the original value. For example a Yd11 transformer has a vector group setting of 11 when the phase sequence is ABC. However if the phase sequence changes to ACB, then the vector group setting should be set to 1.

> *Note:*
> *To minimise imbalances due to tap changer operation, current inputs to the differential element should be set according to the mid-tap position and not the nominal voltage. The **Ref Vector Group** setting provides a reference vector group to which all other vector groups are referenced. Typically, this is set to 0°.*

6.3.2 SELECTING THE CURRENT INPUTS

The P642 has two current terminal inputs (T1 and T2), the P643 has up to three terminal current inputs (T1 to T3), and the P645 has up to five current terminal inputs (T1 to T5).

For the P642, you associate one terminal current input with the HV (High Voltage) winding and the other with the LV (Low Voltage) winding.

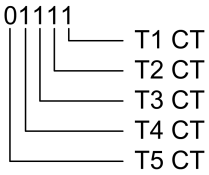
For the P643 and P645 you can choose to associate more than one terminal current input with particular windings. In cases where more than one terminal CT is associated with a winding, the input to the differential protection

function uses the vector sum of the current terminal inputs (on a phase by phase basis) as the input to the calculation for that winding.

You associate these current inputs with the system transformer windings with the settings ***HV CT Terminals***, ***LV CT Terminals*** and ***TV CT Terminals*** in the *SYSTEM CONFIG* column as follows:

Setting	P642	P643	P645
HV CT Terminals	01	001 011	00001 00011 00111 01011 01111
LV CT Terminals	10	100 110	10000 11000 11100 11010 11110
TV CT Terminals		010	00100 01100 00110 01110

Where the terminals T1 to T5 correspond to the bits in the binary string as follows (1 = in use, 0 = not in use). The bit order starts with T1 on the right-hand side. For example:



If a CT is assigned to more than one winding, then an alarm is issued (***CT Selection Alm***). When this DDB signal is asserted, the protection is also blocked.

6.3.3 PHASE CORRECTION

The device automatically carries out phase correction based on the settings made in the *SYSTEM CONFIG* column.

For a reverse phase rotation (ACB), the device will automatically form a complementary value for the vector group ID. You can achieve reverse phase rotation by setting the ***Phase Sequence*** setting in the *SYSTEM CONFIG* column. The device will then automatically form the complementary value of the set vector group ID by subtracting it from the number 12 (vector group ID = 12 - set ID).

6.3.4 RATIO CORRECTION

For transformer differential protection, ratio correction is required. The device automatically calculates the ratio correction factor for each of the current inputs and displays the calculated matching factors in the *SYSTEM CONFIG* column.

As well as the parameters of the power transformer itself, which are defined in the *SYSTEM CONFIG* column, you need to set up the CT ratios and polarities. You do this in the ***CT AND VT RATIOS*** column with the ***Polarity***, ***Primary*** and ***Secondary*** settings for all CTs used.

The device then calculates the ratio correction factors as follows:

$$I_{ref,n} = \frac{S_{ref}}{\sqrt{3}V_{nom,n}} \qquad K_{amp,n} = \frac{I_{nom,n}}{\frac{S_{ref}}{\sqrt{3}V_{nom,n}}}$$

where:

- Sref = common reference power for all ends
- Iref,n = reference current for the respective CT input
- Kamp,n = amplitude-matching factor for the respective CT input
- Inom,n = primary nominal currents for the respective CT input
- Vnom,n = primary nominal voltage for the respective CT input

The device also checks that the matching factors are within their permissible ranges. The matching factors must satisfy the condition:

0.05 <= Kamp <= 15 for standard CTs

0.05 <= Kamp <= 20 for sensitive CTs

6.3.5 CT PARAMETER MISMATCH

The CT parameter (CT Para) mismatch logic implemented in firmware is as follows:

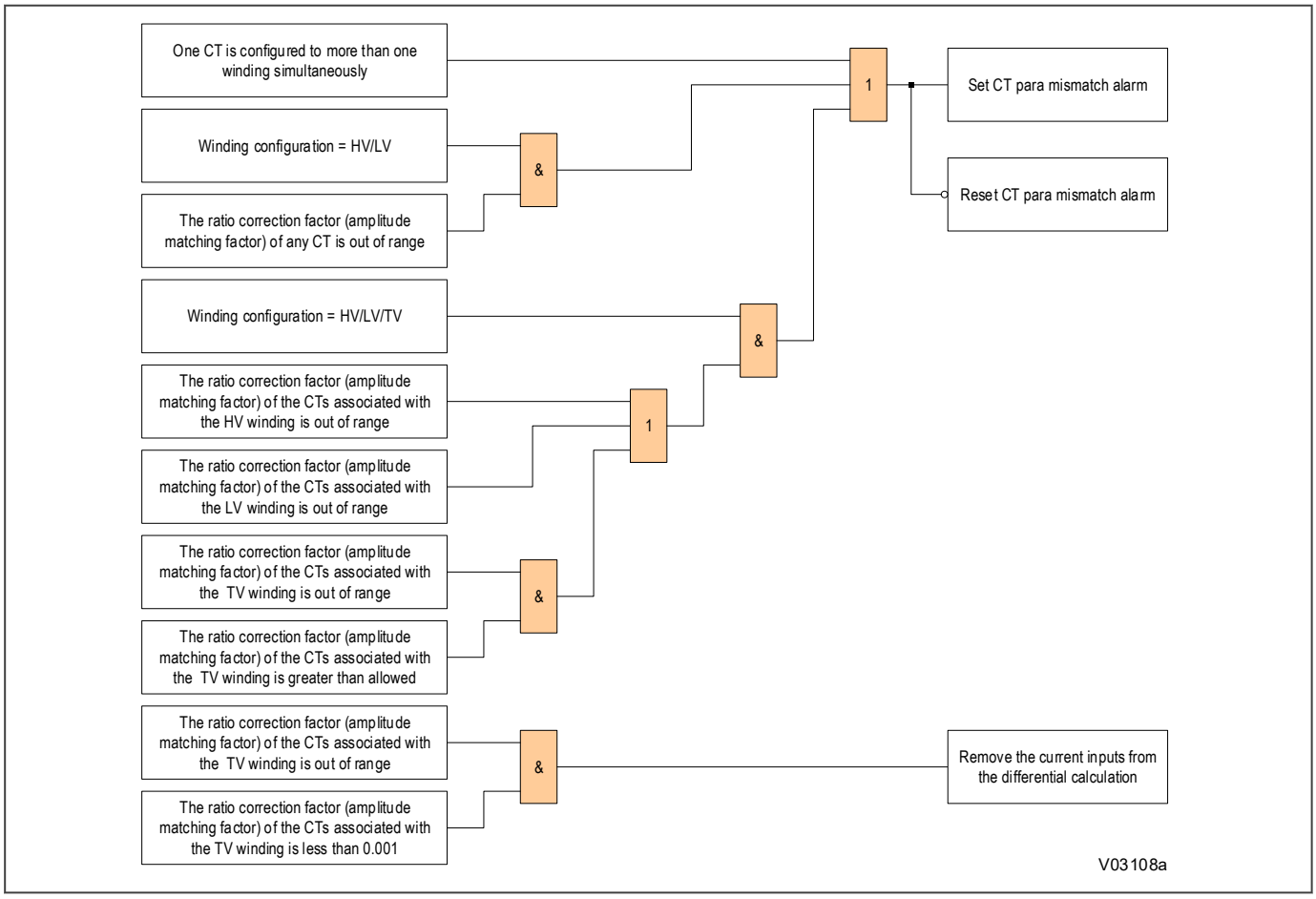


Figure 45: CT parameter mismatch logic diagram

If any of the ratio correction factors in two-winding applications are out of range, the ***CT para mismatch*** alarm is asserted. In multi-winding applications, the alarm is asserted if the ratio correction factor of the CTs associated with

HV or LV windings are out of range or the ratio correction factor of the CTs associated to TV winding is greater than 15 for standard CTs and 20 for sensitive CTs.

If the ratio correction factor of the CT associated to TV winding is lower than 0.001, this current is removed from the differential calculation, as shown in the logic diagram.

If the ***CT para mismatch*** alarm is asserted the protection is also blocked.

The phase current measured values of the windings of the protected object are always scaled by the relevant matching factors. These are then available for further processing. Consequently, all threshold values and measured values refer back to the relevant reference currents rather than to the transformer nominal currents or the nominal currents of the device.

6.3.6 SETTING UP ZERO SEQUENCE FILTERING

There are two modes of operation for zero sequence filtering; simple and advanced. You set the operation mode with the ***Set Mode*** setting in the *DIFFPROTECTION* column.

In simple mode, you cannot disable zero sequence filtering. It is automatically implemented for all earthed windings. You can define whether a winding is earthed or not with the settings ***HV Grounding***, ***LV Grounding*** and ***TV Grounding*** in the *SYSTEM CONFIG* column. If a setting is set to `grounded`, zero sequence filtering will always be implemented for that winding. If set to `Ungrounded`, it will not be implemented.

In advanced mode, you can enable or disable zero sequence filtering manually using the settings ***Zero seq filt HV***, ***Zero seq filt LV*** and ***Zero seq filt TV*** in the *DIFF PROTECTION* column.

6.3.7 TRIPPING CHARACTERISTICS

The differential and bias currents for each phase are calculated from the current variables after amplitude and vector group matching.

The differential current is the vector sum of the CT current inputs as follows:

$$P642: I_{diff,y} = \left| \overrightarrow{I_{s,y,CT1}} + \overrightarrow{I_{s,y,CT2}} \right|$$

$$P643: I_{diff,y} = \left| \overrightarrow{I_{s,y,CT1}} + \overrightarrow{I_{s,y,CT2}} + \overrightarrow{I_{s,y,CT3}} \right|$$

$$P645: I_{diff,y} = \left| \overrightarrow{I_{s,y,CT1}} + \overrightarrow{I_{s,y,CT2}} + \overrightarrow{I_{s,y,CT3}} + \overrightarrow{I_{s,y,CT4}} + \overrightarrow{I_{s,y,CT5}} \right|$$

The bias current is defined as half of the scalar sum of the CT current inputs:

$$P642: I_{bias,y} = 0.5 \cdot \left[\left| \overrightarrow{I_{s,y,CT1}} \right| + \left| \overrightarrow{I_{s,y,CT2}} \right| \right]$$

$$P643: I_{bias,y} = 0.5 \cdot \left[\left| \overrightarrow{I_{s,y,CT1}} \right| + \left| \overrightarrow{I_{s,y,CT2}} \right| + \left| \overrightarrow{I_{s,y,CT3}} \right| \right]$$

$$P645: I_{bias,y} = 0.5 \cdot \left[\left| \overrightarrow{I_{s,y,CT1}} \right| + \left| \overrightarrow{I_{s,y,CT2}} \right| + \left| \overrightarrow{I_{s,y,CT3}} \right| + \left| \overrightarrow{I_{s,y,CT4}} \right| + \left| \overrightarrow{I_{s,y,CT5}} \right| \right]$$

where:

- y is the measured phase (A, B or C)
- I_s is the current after the amplitude and vector group are matched.

The tripping characteristic has two knees. The first knee is dependent on the settings of Is1 and K1. The second knee is defined by the setting Is2. The lower slope provides stability for low external faults. The higher slope provides stability for high through fault conditions, since transient differential currents may be present due to current transformer saturation.

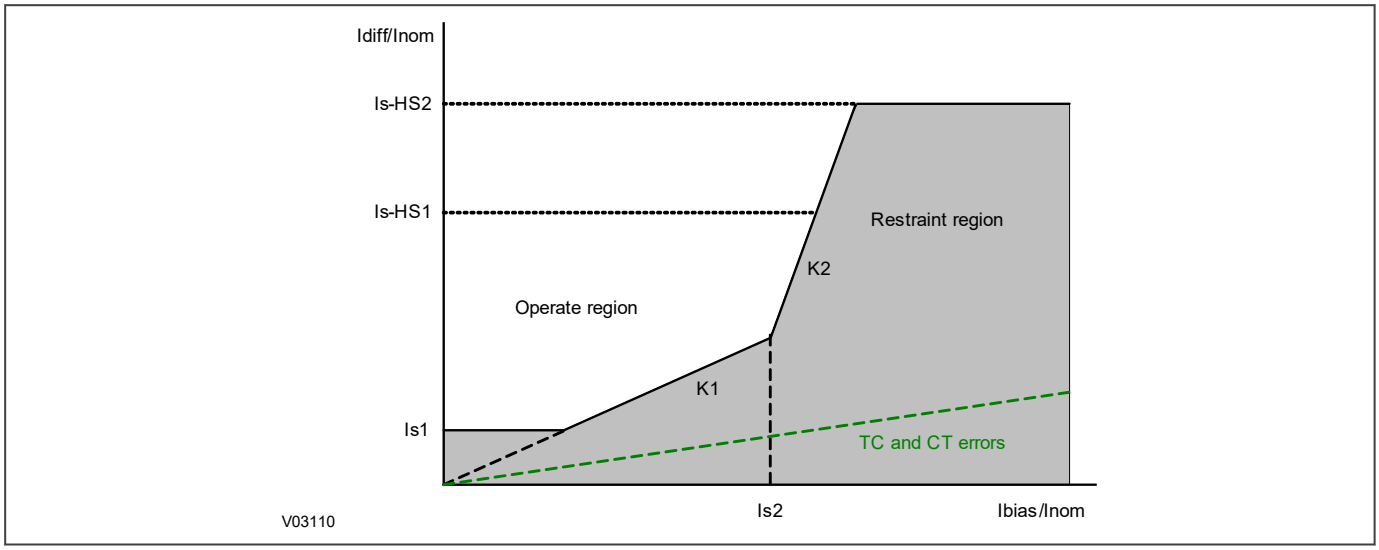


Figure 46: Transformer biased tripping characteristic

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrain signal is obtained:

For the flat slope range: $0 \leq I_{bias\ max} \leq I_{s1}/K_1$

$$I_{diff} \geq I_{s1} + \text{transient bias}$$

For the K1 slope range: $I_{s1}/K_1 \leq I_{bias\ max} \leq I_{s2}$

$$I_{diff} \geq K1.I_{bias\ max} + \text{transient bias}$$

For the K2 slope range: $I_{s2} \leq I_{bias\ max} \leq I_{s\text{-}HS2}/K2$

$$I_{diff} \geq K1.I_{s2} + K2(I_{bias\ max} - I_{s2}) + \text{transient bias}$$

6.3.7.1 HIGH-SET FUNCTION

The High Set 1 algorithm uses a peak detection method to achieve fast operating times. The peak value is the largest absolute value of differential current in the latest cycle. Since the High Set 1 algorithm uses a peak detection method, Is-HS1 is set above the expected highest magnetizing inrush peak to maintain immunity to magnetizing inrush conditions. For a High Set 1 trip, two conditions must be fulfilled:

- The peak value of the differential current is greater than Is-HS1 setting.
- The bias characteristic is in the operate region.

If the differential current is above the adjustable ***Is-HS1*** threshold, the device will trip if in the Operate region, but not in the restrain region. However, second harmonic blocking and overfluxing blocking are NOT taken into account. The High Set 1 resets when the differential and bias currents are in the restraint area.

If the differential current is above the adjustable ***Is-HS2*** threshold, bias current is not taken into account and the device will trip regardless. As with High Set 1, second harmonic blocking and overfluxing blocking are NOT taken into account. The High Set 2 element resets when the differential current drops below 0.95****Is-HS2***.

6.3.7.2 CIRCUITRY FAIL ALARM

The circuitry fail alarm logic requires the following settings:

Circuitry Fail: to enable or disable the function

Is-cctfail: to define the minimum differential threshold

K-cctfail: to define the slope gradient

CctFail Delay: to set a time delay

If the differential current is larger than the ***Is-cctfail*** setting and no trip is issued after the time delay has elapsed, an alarm is issued indicating a CT problem.

6.3.8 TRIPPING CHARACTERISTIC STABILITY

Conditions such as CT saturation and transient switching operations can cause incorrect operation of differential elements. To avoid this a number of techniques are employed in this device. These include :

- Maximum and Residual Bias
- Transient Bias
- CT saturation detection (to discriminate between internal and external faults)
- No Gap Detection
- External Fault Detection
- Current Transformer Supervision
- Circuitry Fail Alarm
- Second Harmonic Blocking
- Fifth Harmonic Blocking

6.3.8.1 MAXIMUM BIAS

The differential and bias currents are calculated on a per phase basis eight times per cycle. A comparison between differential and bias current is used to determine whether to trip or not. The comparison is made on a per phase basis using the differential current measured on that phase. However a common bias current is used for all three phases.. To assure stability, the largest bias current calculated on any phase is used to restrain all phases. This is referred to as the Maximum Bias.

6.3.8.2 DELAYED BIAS

To provide further stability when external faults are being cleared, the protection checks for the highest value of bias current calculated during the previous cycle. If that value is higher than the present value, it is used to restrain the tripping decision. This is referred to as the Residual Bias. The Residual Bias technique maintains through fault stability for clearance of external faults.

6.3.8.3 TRANSIENT BIAS

If there is a sudden increase in the mean-bias measurement, an additional bias quantity (called Transient Bias) can be introduced into the bias calculation, on a per-phase basis. Transient Bias is only active for external faults. It can be enabled or disabled with the Transient Bias setting in the *DIFF PROTECTION* column.

Transient bias, decays exponentially. The transient bias quantity is added to the operating current calculated at the maximum bias. Therefore, the following differential current thresholds are available:

Differential threshold phase A = Iop at max bias + transient bias_phase A

Differential threshold phase B = Iop at max bias + transient bias_phase B

Differential threshold phase C = Iop at max bias + transient bias_phase C

The transient bias technique uses a time decay constant, stability coefficients, and some differential function settings to provide a dynamic bias characteristic. The following diagram shows the behaviour during an external fault. For the device to trip, the fundamental of the differential current should be above the operating current at max bias + transient bias.

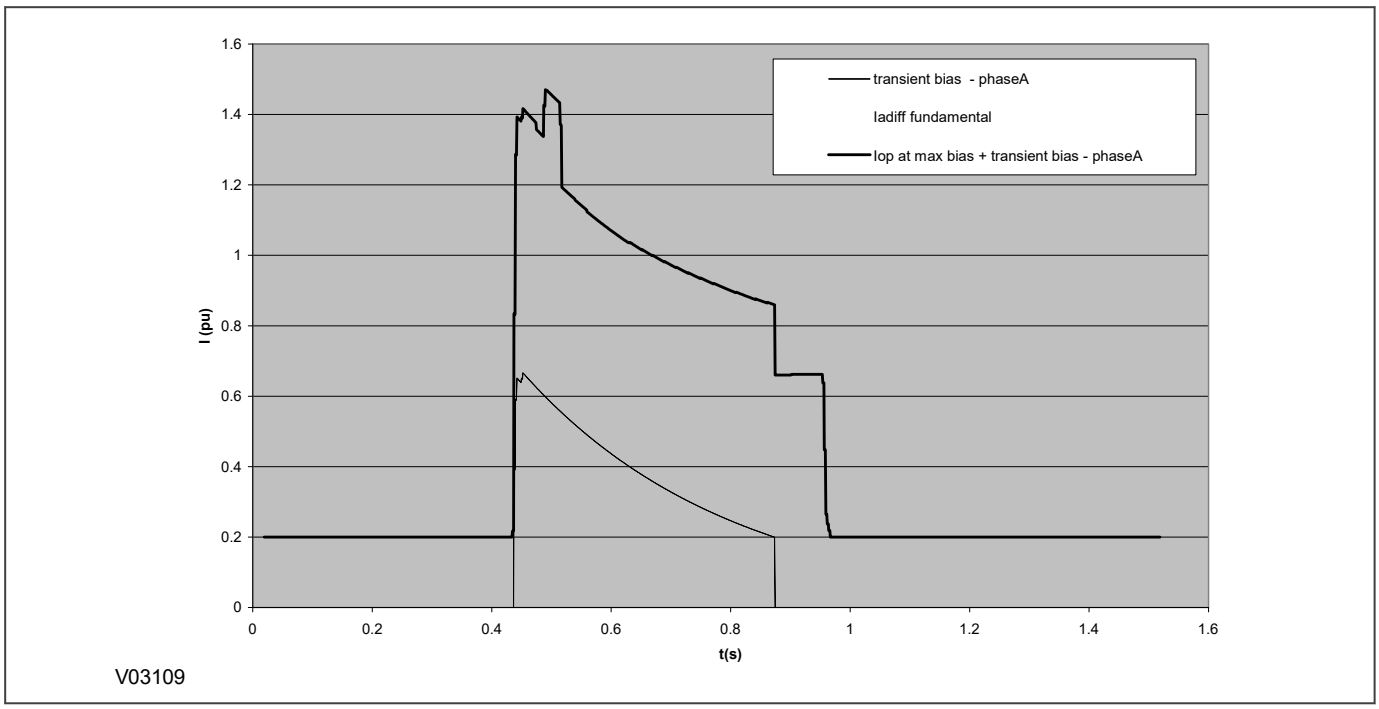


Figure 47: Transient bias characteristic

The transient bias function enhances the stability of the differential element during external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios.

No transient bias is produced under load switching conditions, or when the CT comes out of saturation.

6.3.8.4 CT SATURATION TECHNIQUE

During CT saturation the second harmonic content may be high enough to block the low set differential element. This would result, in the operation of the low set differential element being delayed for some internal faults. The device includes a CT Saturation Detection technique, which unblocks the low set differential element during internal faults with heavy CT saturation. This CT saturation detection technique is capable of distinguishing between magnetising inrush and CT saturation. Therefore the 2nd harmonic blocking will work properly for magnetising inrush, but will not be asserted for internal faults where CT saturation is an issue. This function is enabled or disabled with the ***CT Saturation*** setting in the *DIFF PROTECTION* column.

6.3.8.5 NO GAP DETECTION TECHNIQUE

The No Gap Detection technique detects light CT saturation on a per phase basis. The No Gap Detection technique unblocks the low set differential element during light CT saturation, allowing the low set differential element to trip faster. Stability during inrush conditions is maintained, as this technique distinguishes between an inrush and a saturated waveform. This function is enabled or disabled with the ***No Gap*** setting in the *DIFF PROTECTION* column.

6.3.8.6 EXTERNAL FAULT DETECTION TECHNIQUE

An External Fault Detection technique has been implemented so that the CT saturation and No gap detection techniques do not affect the second harmonic blocking during an external fault.

This technique considers the time to saturation, a delta bias start signal, a delta differential start signal and the ratio of delta differential to delta bias at the time of start. As soon as an external fault occurs, the bias current changes, but the differential current only increases after the time to saturation. The external fault detection DDBs are asserted if the following conditions are fulfilled:

The delta bias start signal is asserted first. The delta bias start signal and the delta differential start signal are asserted if the delta bias and delta differential currents are greater than 0.65 Is1 respectively.

The time difference between the assertion of the delta bias start signal and the assertion of the delta differential signal is greater than the time to saturation. The minimum time to saturation is 2.5 ms for a 50 Hz system and 2.08 ms for a 60 Hz system.

The ratio of delta differential to delta bias is smaller than a fixed threshold when the delta bias start signal is asserted.

The External Fault Detection algorithm is on a per phase basis. If an external fault is detected on phase A, B or C, signals ***External fault A***, ***External fault B*** or ***External fault C*** are asserted. The external fault detector resets after 6 seconds from the start or after 25 cycles from the start if the current is less than 0.9Is1.

The following figure shows the time to saturation for an external fault.

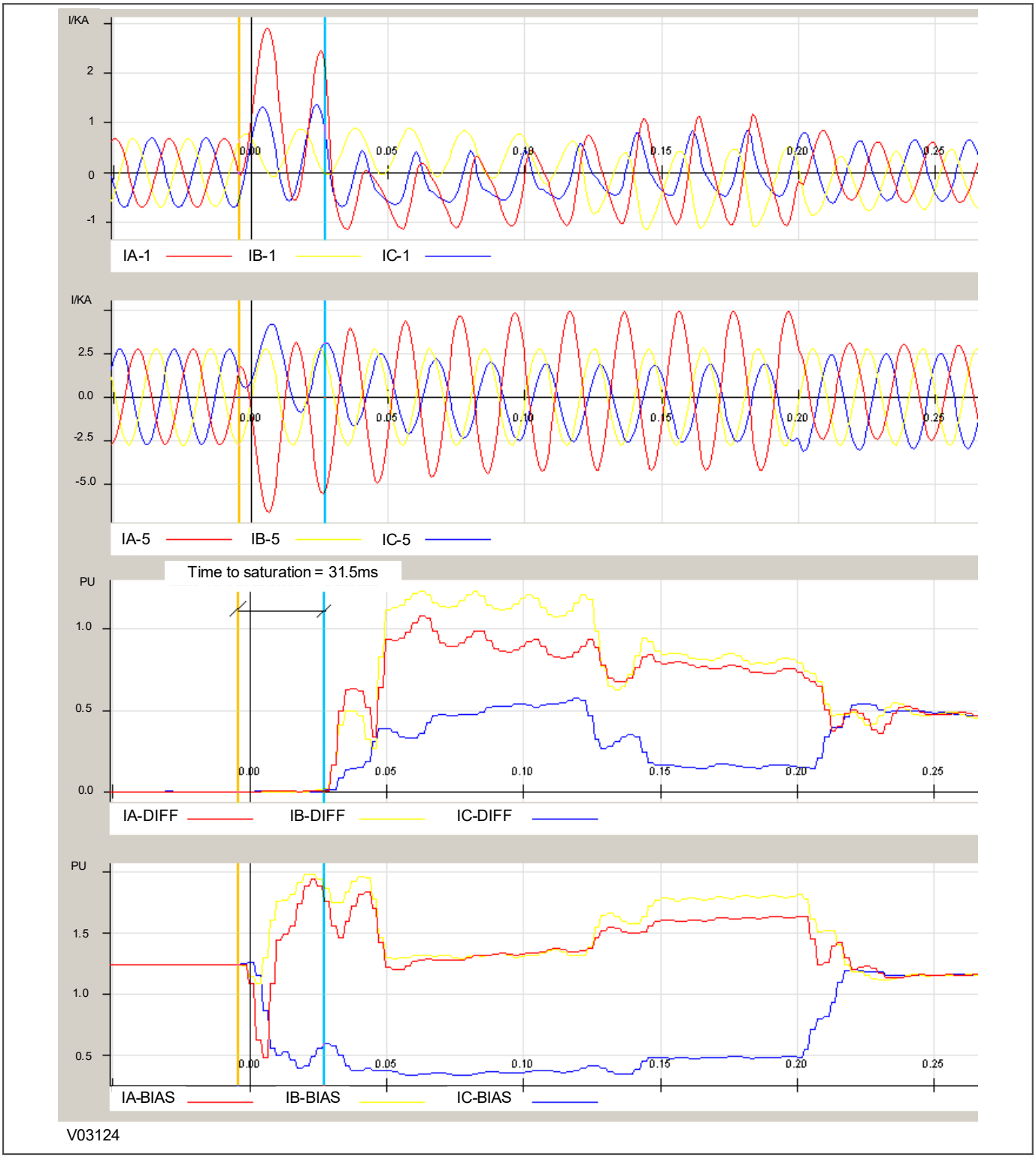


Figure 48: Time to saturation - external AN fault

6.3.8.7 PHASE COMPARISON TECHNIQUE

During some of the evolving fault conditions from an external to an internal fault, the P64 uses a phase comparison technique for faster fault clearance.

The phase comparison technique is activated once an external fault is detected and the bias current is greater than Is2 × Phase Comp Ratio threshold, as shown in the figure below:

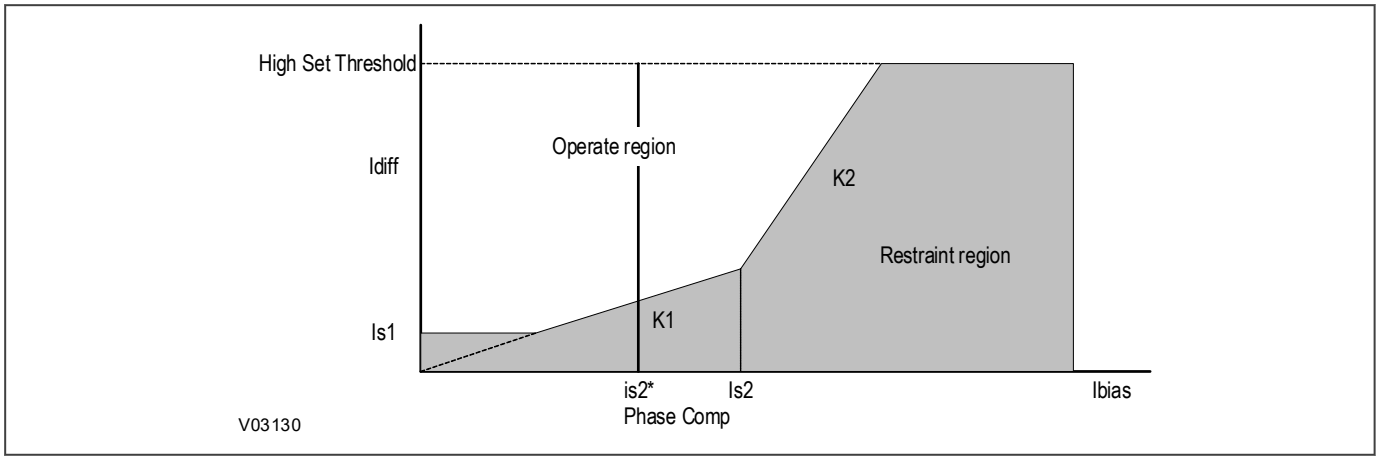


Figure 49: Is2 x phase comparison

When the phase comparison is activated, it compares the relative angle of each winding current after applying phase and amplitude compensation. If the measured relative angle is less than 90 degrees, this indicates the fault is internal and the external fault detector is reset.

When the external fault detector resets it removes the transient bias. CT saturation and NO GAP technique are activated, making the clearance of internal faults faster.

6.3.8.8 CURRENT TRANSFORMER SUPERVISION

If the ***CTS Status*** setting in the SUPERVISION Column is set to restrain, then upon detection of a CTS condition, and following the ***CTS Time Delay***, the minimum operating current is raised to the ***Is-CTS*** value.

This has the effect of lifting the minimum operate current threshold on the bias characteristic as follows:

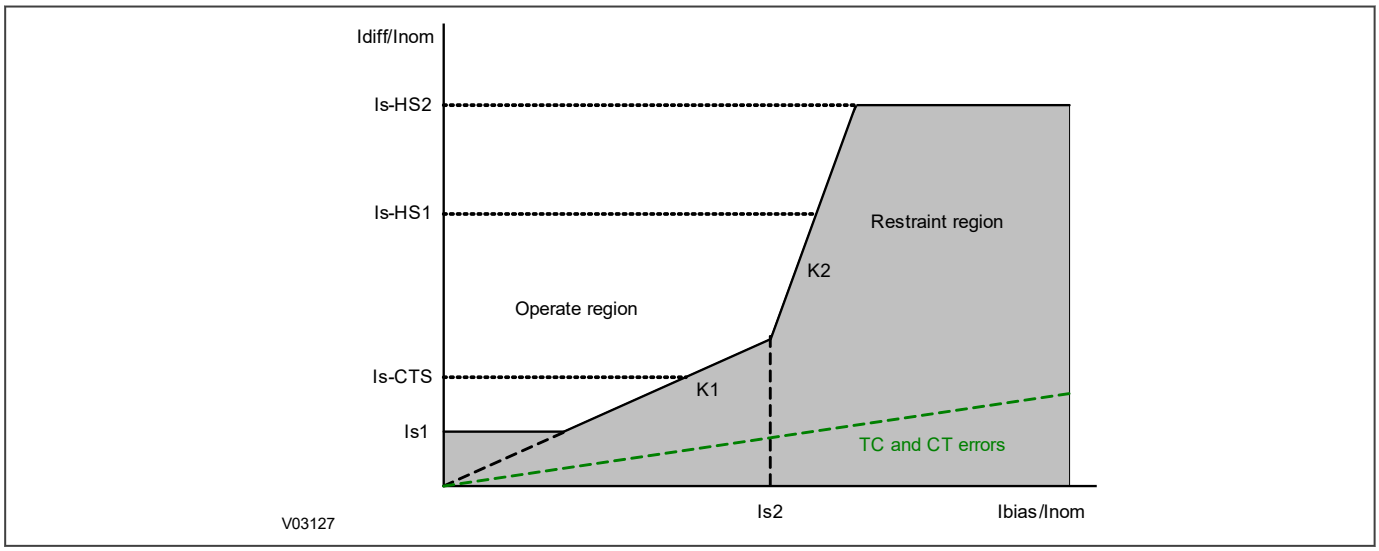


Figure 50: Effect of CTS restrain

6.3.8.9 CIRCUITRY FAIL ALARM

Under normal operating conditions there should be no differential current (although there might be a small amount due to CT mismatch). Under conditions such as current transformer (CT) failure or a failure of the CT circuitry, a small differential current may be seen. This product can monitor the scheme for such conditions with a dual slope differential characteristic, by enabling the ***Circuitry Fail*** setting in the DIFF PROTECTION column. The characteristic is then defined by the settings ***Is-cctfail*** and ***k-cctfail***. By default it is a time-delayed element to prevent conflict with the tripping characteristic in the event of a genuine transformer fault. But if the ratio of

differential to bias current exceeds the ***Is-cctfail*** and ***k-cctfail*** settings, but does not exceed the ***Is1*** and ***k1*** settings, for the duration of the ***Is-cctfail*** setting, a circuitry fail alarm is raised. The ***Is-cctfail*** delay is set to 5 seconds by default.

The level at which the circuitry fail alarm would operate under these circumstances is shown by the red line as follows:

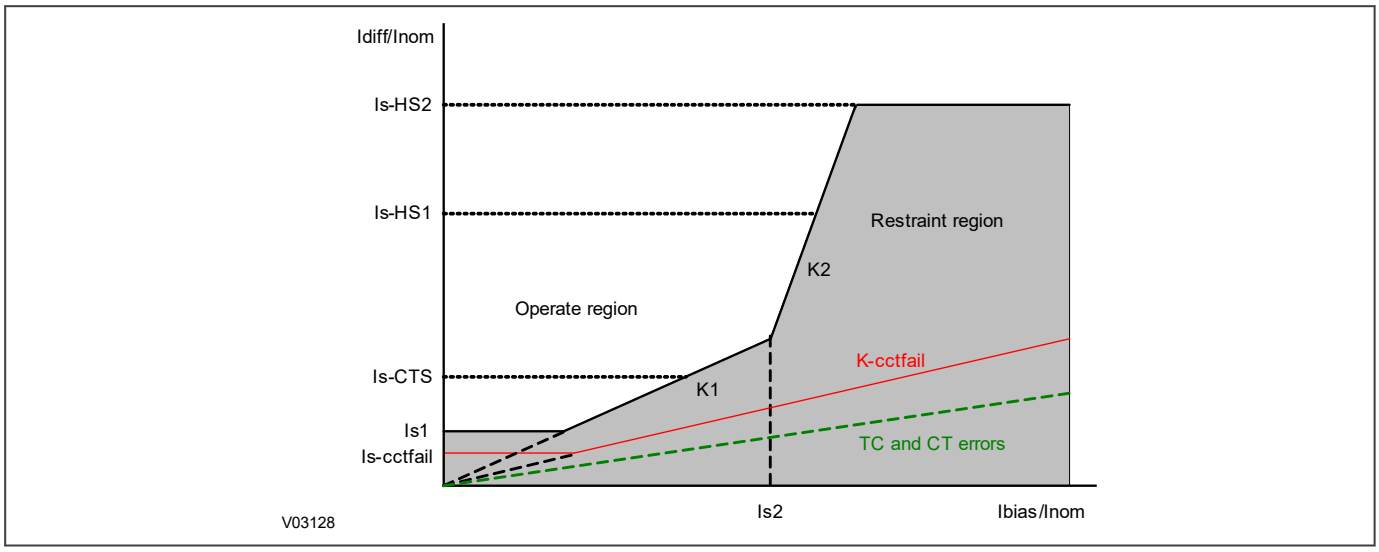


Figure 51: Bias characteristic with circuitry fail alarm

6.3.9 DIFFERENTIAL BIASED TRIP LOGIC

The differential biased trip is affected by both the CT Saturation technique and by the No Gap detection technique. If the second harmonic blocking is asserted and either the CT Saturation Detection or No Gap detection technique is asserted, then the biased differential trip is unblocked.

CT Saturation Detection and No Gap detection act independently from 5th harmonic blocking, however. A biased differential trip will occur only if the fifth harmonic blocking is not asserted and the bias differential start signal is asserted. The differential biased trip logic is described below.

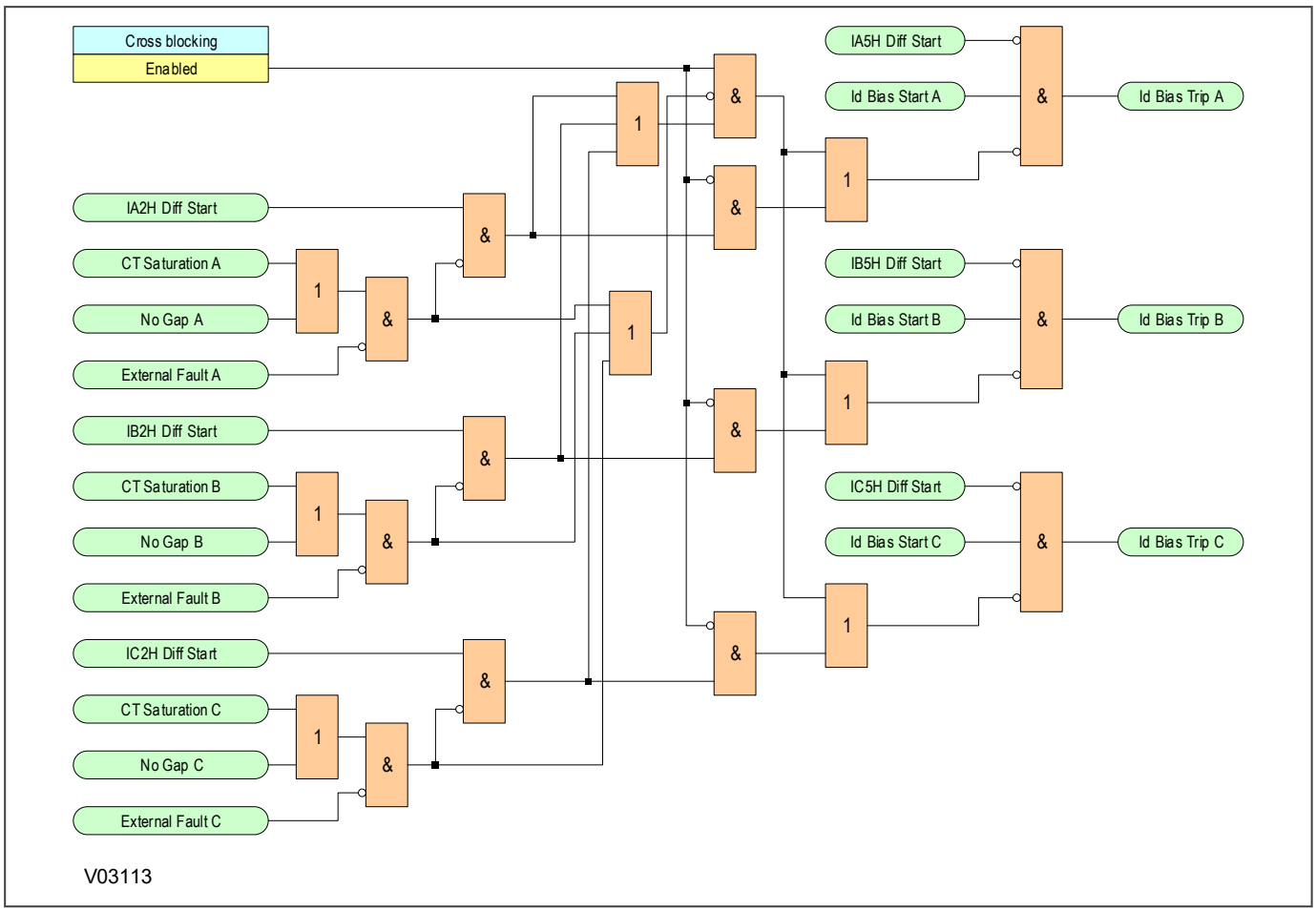


Figure 52: Differential biased trip logic

6.4 HARMONIC BLOCKING

6.4.1 2ND HARMONIC BLOCKING

The IED filters the differential current to determine the fundamental (Idiff(fn)) and second harmonic (Idiff(2fn) current components. The device uses these quantities to produce a blocking signal, which will block the protection in the event that the second harmonic component exceeds a certain level.

Second harmonic blocking is phase segregated. If the ratio of the second harmonic component to fundamental component exceeds an adjustable threshold (set by ***IH2 Diff Set***) in two consecutive calculations, a second harmonic blocking signal is issued for the relevant phase. These are:

IA2H Diff Start (blocking signal for phase A)

IB2H Diff Start (blocking signal for phase B)

IC2H Diff Start (blocking signal for phase C)

If the ***Cross Blocking*** setting in the *DIFF PROTECTION* column is enabled, any one of the phase blocking signals will block all three phases.

No blocking signal is asserted if the differential current exceeds the set thresholds ***Is-HS1*** or ***Is-HS2***.

The following flow diagram summarises the 2nd harmonic blocking procedure:

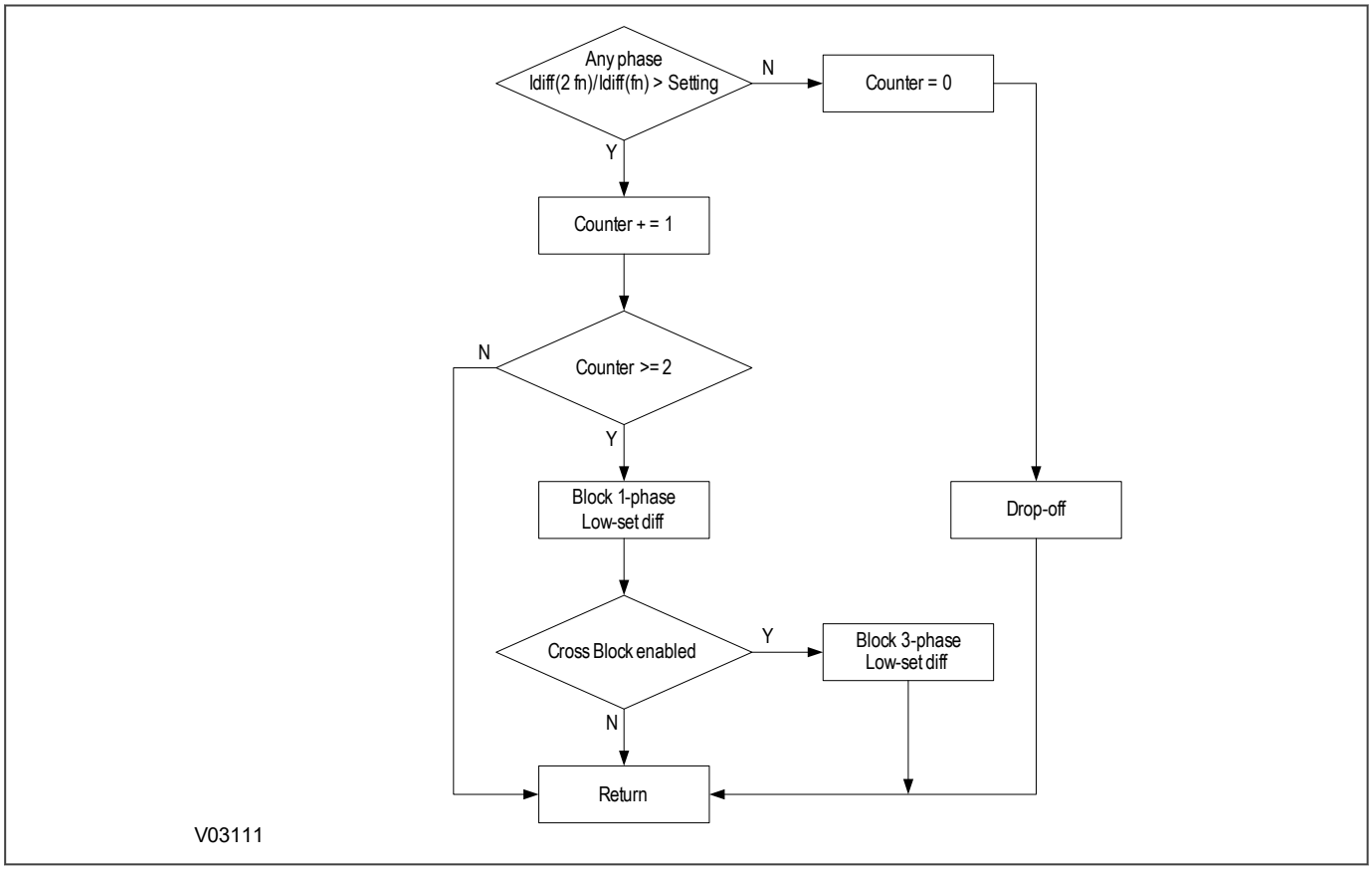


Figure 53: 2nd harmonic blocking process

6.4.2 2ND HARMONIC BLOCKING LOGIC

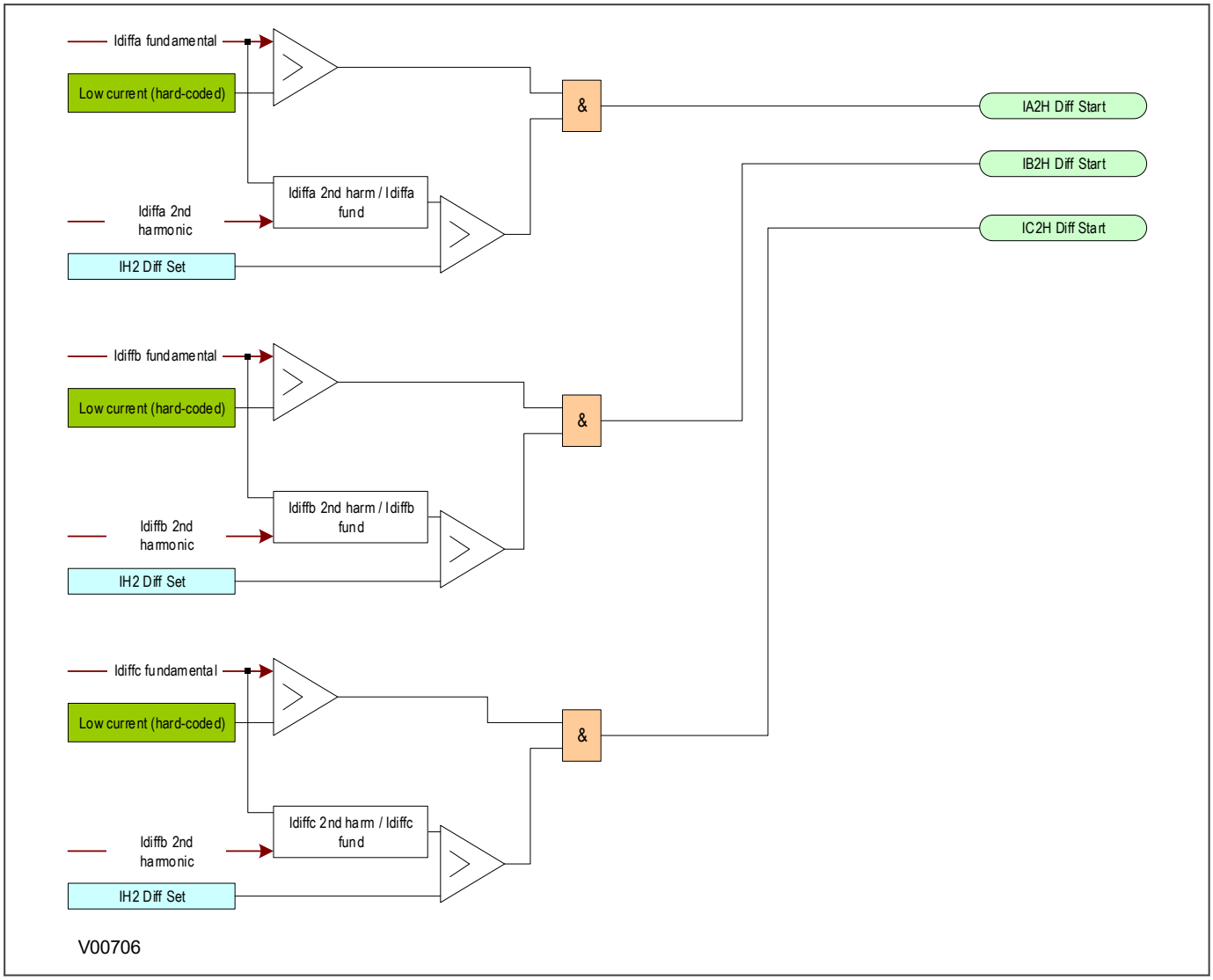


Figure 54: 2nd harmonic blocking logic

6.4.3 2ND HARMONIC SETTING GUIDELINES

During the energization period, the second harmonic component of the inrush current may be as high as 70%, depending on the power rating. The second harmonic level may be different for each phase, which is why phase segregated blocking is available.

If the setting is too low, the 2nd harmonic blocking may prevent tripping during some internal transformer faults. If the setting is too high, the blocking may not operate for low levels of inrush current which could result in undesired tripping of the differential element during the energization period. In general, a setting of 15% to 20% is suitable.

When testing the 2nd Harmonic blocking feature using an Omicron harmonic restraint module, it is recommended that the ***CT Saturation*** and ***No Gap*** settings are `Disabled` while keeping ***Transient Bias*** either `Enabled` or `Disabled`. However, when the relay is in service it is recommended that the ***CT Saturation*** and ***No Gap*** settings are both `Enabled`. This is to make sure that if an internal fault develops during energisation of the transformer, the 2nd Harmonic blocking feature does not delay tripping of the differential protection element.

6.4.4 5TH HARMONIC BLOCKING IMPLEMENTATION

The IED filters the differential current to determine the fundamental Idiff(fn) and the fifth harmonic component Idiff(5fn). The device uses these quantities to produce a blocking signal, which will block the protection in the event that the fifth harmonic component exceeds a certain level.

5th Harmonic blocking can be used to prevent unwanted operation of the low set differential element under transient overfluxing conditions.

The 5th harmonic blocking threshold is adjustable between 0 - 100% differential current. The threshold should be adjusted so that blocking will be effective when the magnetizing current rises above the chosen threshold setting of the low-set differential protection.

Fifth harmonic blocking is phase segregated. If the ratio Idiff(5-fn)/Idiff(fn) exceeds an adjustable threshold (set by ***IH5 Diff Set*** in two consecutive calculations, and if the differential current is larger than 0.1 pu (the minimum setting of Is1), then the fifth harmonic blocking signal is issued for the relevant phase. The DDB signals are:

IA5H Diff Start (blocking signal for phase A)

IB5H Diff Start (blocking signal for phase B)

IC5H Diff Start (blocking signal for phase C)

No cross blocking is available for 5th harmonic blocking.

No blocking signal is asserted if the differential current exceeds the set thresholds ***Is-HS1*** or ***Is-HS2***.

The following flow diagram summarises the 5th harmonic blocking procedure:

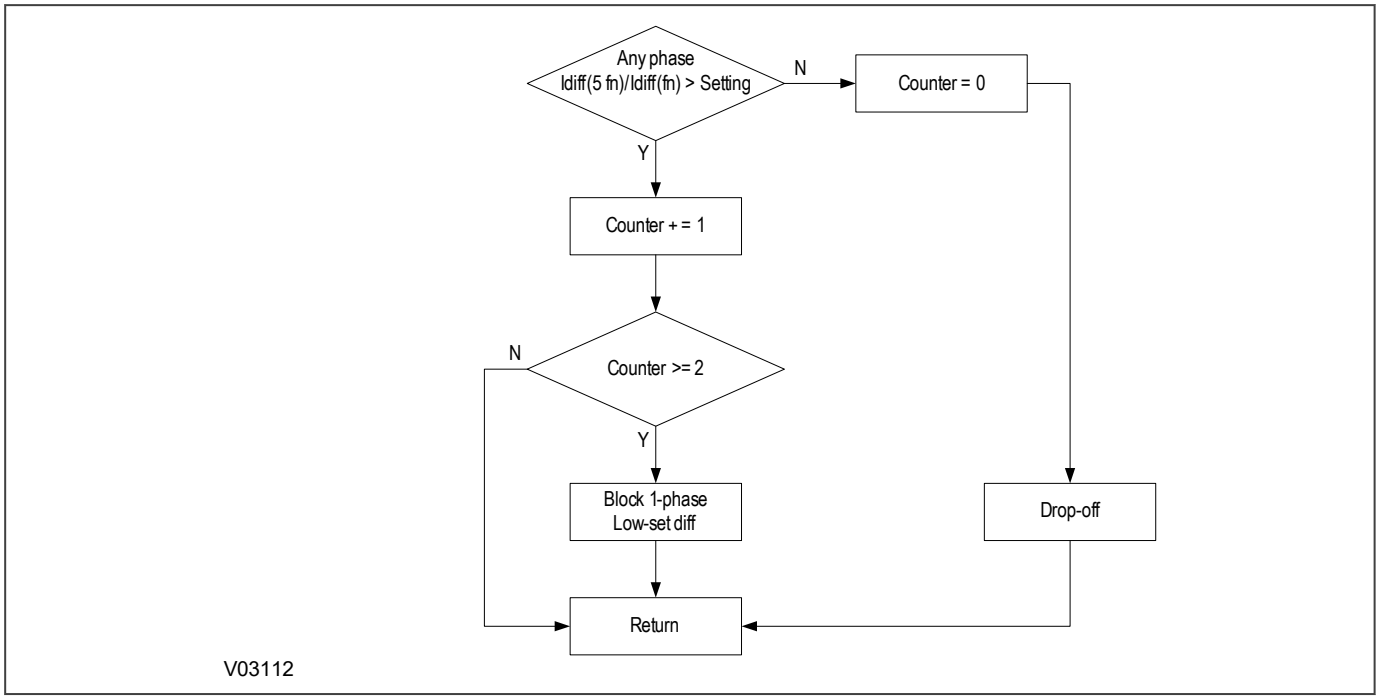


Figure 55: 5th harmonic blocking process

6.4.5 5TH HARMONIC SETTING GUIDELINE

In most applications, the default settings will ensure stability of the differential element. If more difficult situations exist, the 5th harmonic differential current blocking facility may be of use.

A typical setting for ***Ih(5)%>*** is `35%`.

6.4.6 GEOMAGNETIC DISTURBANCES

To offer protection against damage due to persistent overfluxing caused by a geomagnetic disturbance, the 5th harmonic blocking element can be mapped to an output contact using an associated timer. Operation of this element could be used to give an alarm to the network control centre. If such alarms are received from a number of transformers, they could serve as a warning of geomagnetic disturbance so that operators could take some action to safeguard the power system.

Alternatively this element can be used to initiate tripping in the event of prolonged pick up of a 5th harmonic measuring element. It is not expected that this type of overfluxing condition would be detected by the AC overfluxing protection. This form of time delayed tripping should only be applied in regions where geomagnetic disturbances are a known problem and only after proper evaluation through simulation testing.

6.4.7 OVERALL HARMONIC BLOCKING LOGIC

The following logic diagram shows how the differential protection blocking mechanism works under conditions of overfluxing and magnetisation inrush.

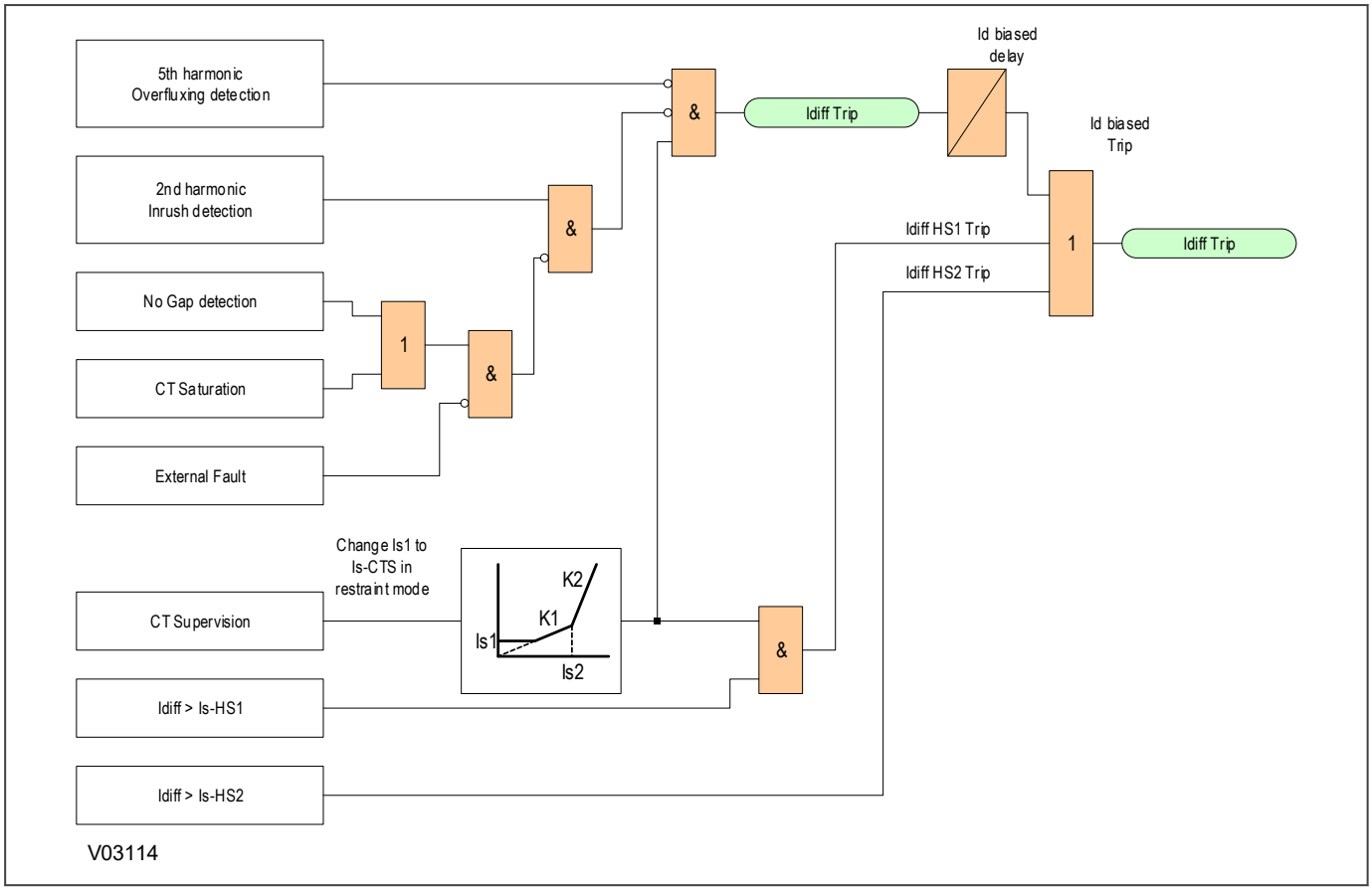


Figure 56: Differential protection blocking mechanisms

6.5 APPLICATION NOTES

6.5.1 SETTING GUIDELINES

The differential setting, Configuration/Diff Protection, should be set to ***Enable***.

The basic pick up level of the low set differential element, ***Is1***, is variable between ***0.1 pu*** and ***2.5 pu*** in ***0.01 pu*** steps. The setting will be dependant on the item of plant being protected and by the amount of differential current that might be seen during normal operating conditions. When the device is used to protect a transformer, we recommend a setting of ***0.2 pu***.

When protecting generators and other items of plant, where shunt magnetizing current is not present, a lower differential setting would be more typical. We recommend ***0.1 pu***.

The P64 percentage bias calculation is performed 8 times per cycle. A triple slope percentage bias characteristic is implemented. Both the flat and the lower slope provide sensitivity for internal faults. Under normal operation steady state magnetizing current and the use of tap changers result in unbalanced conditions and hence differential current. To accommodate these conditions the initial slope, K1, may be set to 30%. This ensures sensitivity to faults while allowing for mismatch when the power transformer is at the limit of its tap range and CT ratio errors. At currents above rated, extra errors may be gradually introduced as a result of CT saturation, Hence, the higher slope may be set to 80% to provide stability under through fault conditions, during which there may be transient differential currents due to saturation effect of the CTs. The through fault current, in all but ring bus or mesh fed transformers, is given by the inverse of the per unit reactance of the transformer. For most transformers, the reactance varies between ***0.05*** to ***0.2 pu***, therefore typical through fault current is given by 5 to 20 In.

The wide matching factor range is provided to allow the designer to trade off between the CT selection and the scheme sensitivity. This is useful for applications such as busbar protection where a wide range of CT ratios may be encountered. You should also note that the matching factor check should be carried out for all ends. One end alone is not sufficient. The maximum sensitivity achieved in this product depends on the type of analog input and is given in the CT requirements.

Note:
Differential protection alone may not achieve the full sensitivity required, and other protection functions such as REF may have to be incorporated in conjunction with the differential protection.

The number of biased differential inputs required for an application depends on the transformer and its primary connections. We recommend, where possible, that a set of biased CT inputs is used for each set of current transformers. According to IEEE C37.110-2007, separate current inputs should be used for each power source to the transformer. If the secondary windings of the current transformers from two or more supply breakers are connected in parallel, under heavy through fault conditions, differential current resulting from the different magnetizing characteristics of the current transformers flows in the IED. This current only flows through one current input in the device and can cause maloperation. If each CT is connected to a separate current input, the total fault current in each breaker provides restraint. You should only connect CT secondary windings in parallel when both circuits are outgoing loads. In this condition, the maximum through fault level is restricted solely by the power transformer impedance.

The P64 IED achieves stability for through faults in two ways, both of which are essential for correct relay operation. The first consideration is the correct sizing of the current transformers. The second is by providing a bias characteristic as shown below:

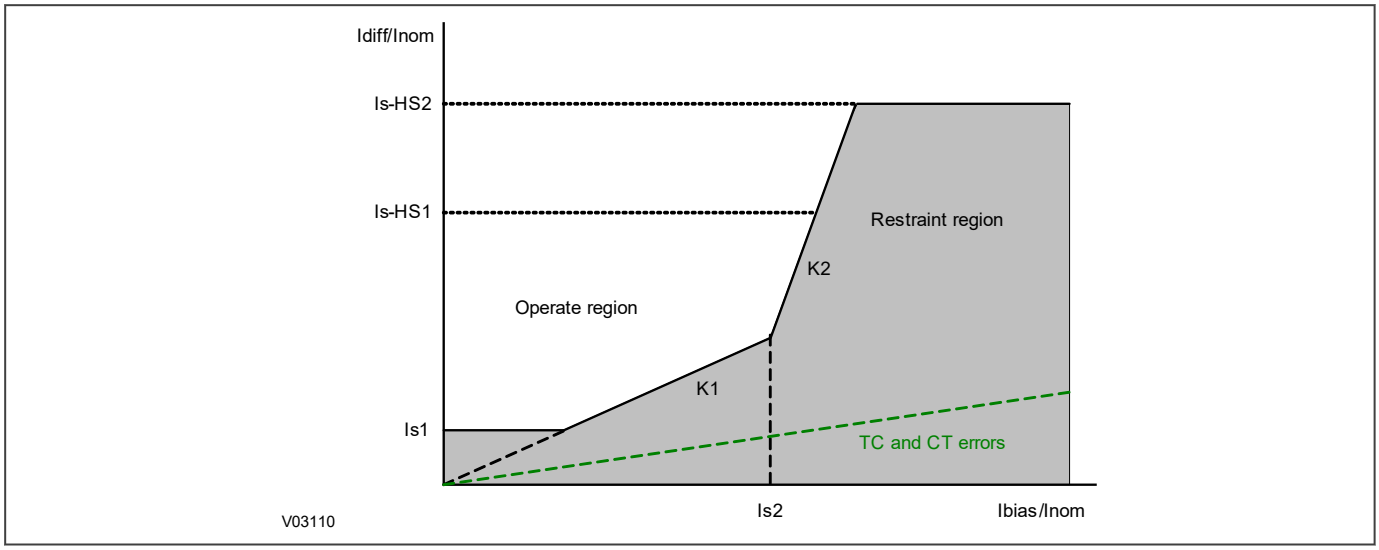


Figure 57: Triple slope characteristic

6.5.2 EXAMPLE 1: TWO-WINDING TRANSFORMER - NO TAP CHANGER

Consider a two-winding power transformer with the following specifications:

- Power rating: 90 MVA Transformer
- Connection type: YNd9
- Voltage specification 132:33 kV.
- HV CT ratio: 400:1
- LV CT ratio: 2000:1
- Percentage reactance: 10%

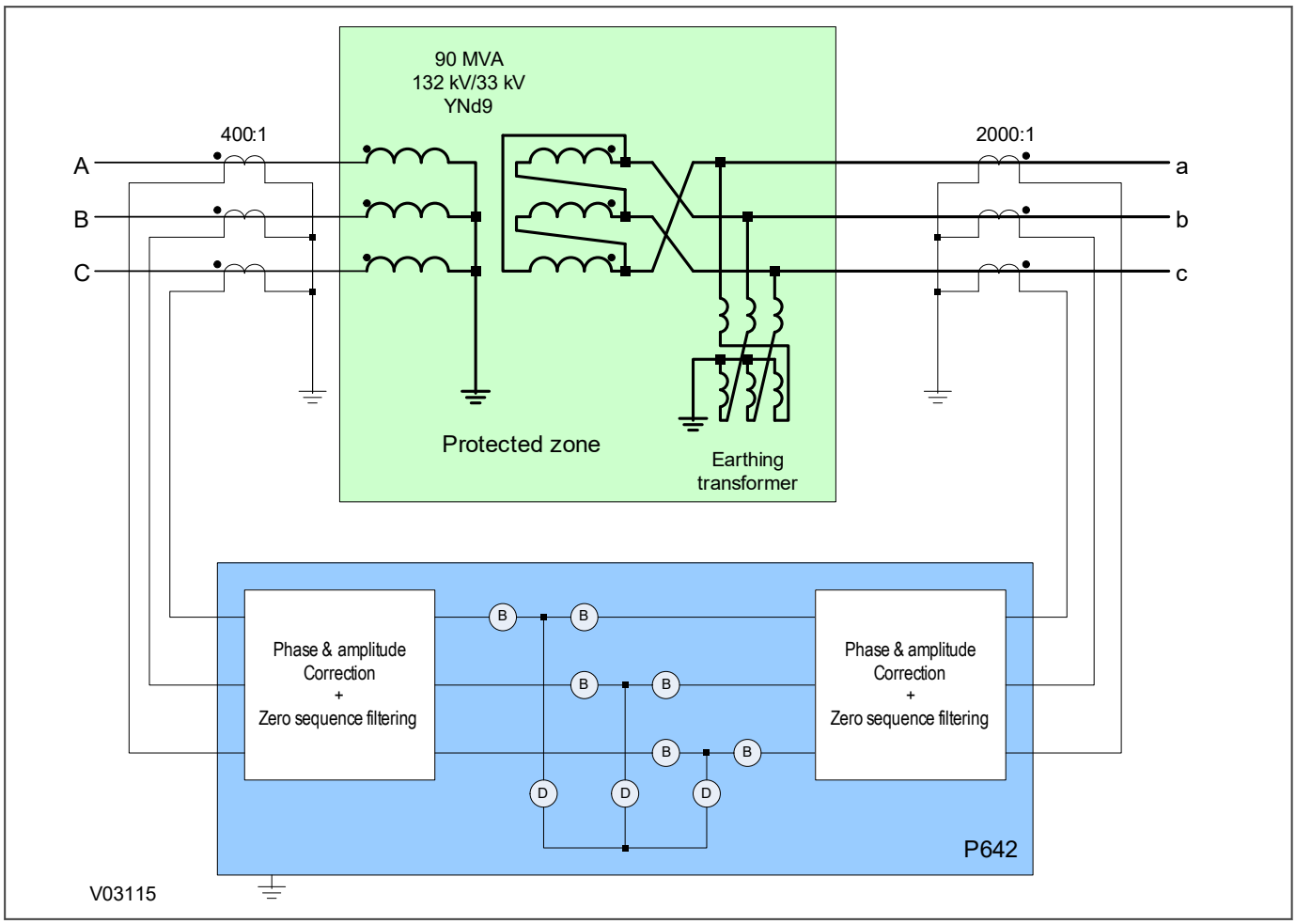


Figure 58: P642 used to protect a two winding transformer

Set the following parameters in the *SYSTEM CONFIG* column:

Setting in GROUP 1 SYSTEM CONFIG	Value
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	01
LV CT Terminals	10
Ref Power S	90.00 MVA
Ref Vector Group	0
HV Connection	Y-Wye
HV Grounding	Grounded
HV Nominal	132.0 kV
HV Rating	90.00 MVA
% Reactance	10.00%
LV Vector Group	9
LV Connection	D-Delta
LV Grounding	Grounded

Setting in GROUP 1 SYSTEM CONFIG	Value
LV Nominal	33.00 kV
LV rating	90.00 MVA
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap

Vector correction and zero sequence filtering are automatically performed by virtue of the LV Vector Group setting and the HV Grounding and LV Grounding settings.

The ratio correction factors are calculated as follows:

$$K_{amp,T1CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{400}{\frac{90\times10^{6}}{\sqrt{3}\times132\times10^{3}}} = 1.016$$

$$K_{amp,T2CT} = \frac{I_{nom,T2CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{2000}{\frac{90\times10^{6}}{\sqrt{3}\times33\times10^{3}}} = 1.270$$

where:

- S_{ref} = common reference power for all ends
- $K_{amp,\ T1CT,\ T2CT}$ = ratio correction factor of T1 CT or T2 CT windings
- $I_{nom,\ T1CT,\ T2CT}$ = primary nominal currents of the main current transformers
- $V_{nom,\ HV,LV}$ = primary nominal voltage of HV or LV windings

These matching factors are also displayed in the *SYSTEM CONFIG* column (***Match Factor CT1*** and ***Match Factor CT2***)

Now set the current differential parameters as follows:

Setting in GROUP 1 DIFF PROTECTION	Value
Trans Diff	Enabled
Set Mode	Advance
Is1	200.0e-3 PU
K1	30.00%
Is2	1.000 PU
K2	80.00%
tdiff	0 s
Is-CTS	1.500 PU
Is-HS1	10.00 PU
HS2 Status	Disabled
Zero seq filt HV	Enabled

Setting in GROUP 1 DIFF PROTECTION	Value
Zero seq filt LV	Enabled
IH2 Diff Block	Enabled
IH2 Diff Set	20%
Cross Blocking	Enabled
CT Saturation	Enabled
No Gap	Enabled
IH5 Diff Block	Enabled
IH5 Diff Set	35%
Circuitry Fail	Disabled

6.5.3 EXAMPLE 2: AUTOTRANSFORMER WITH LOADED DELTA WINDING

Consider an autotransformer with the following specifications:

- Power rating: 175/175/30 MVA
- Connection type: YNyn0d1
- Voltage specification: 230/115/13.8 kV.
- HV CT ratio: 800:5
- LV CT ratio: 1200:5
- TV CT ratio: 2000:5
- HV tap range: +5% / -15% and 19 taps

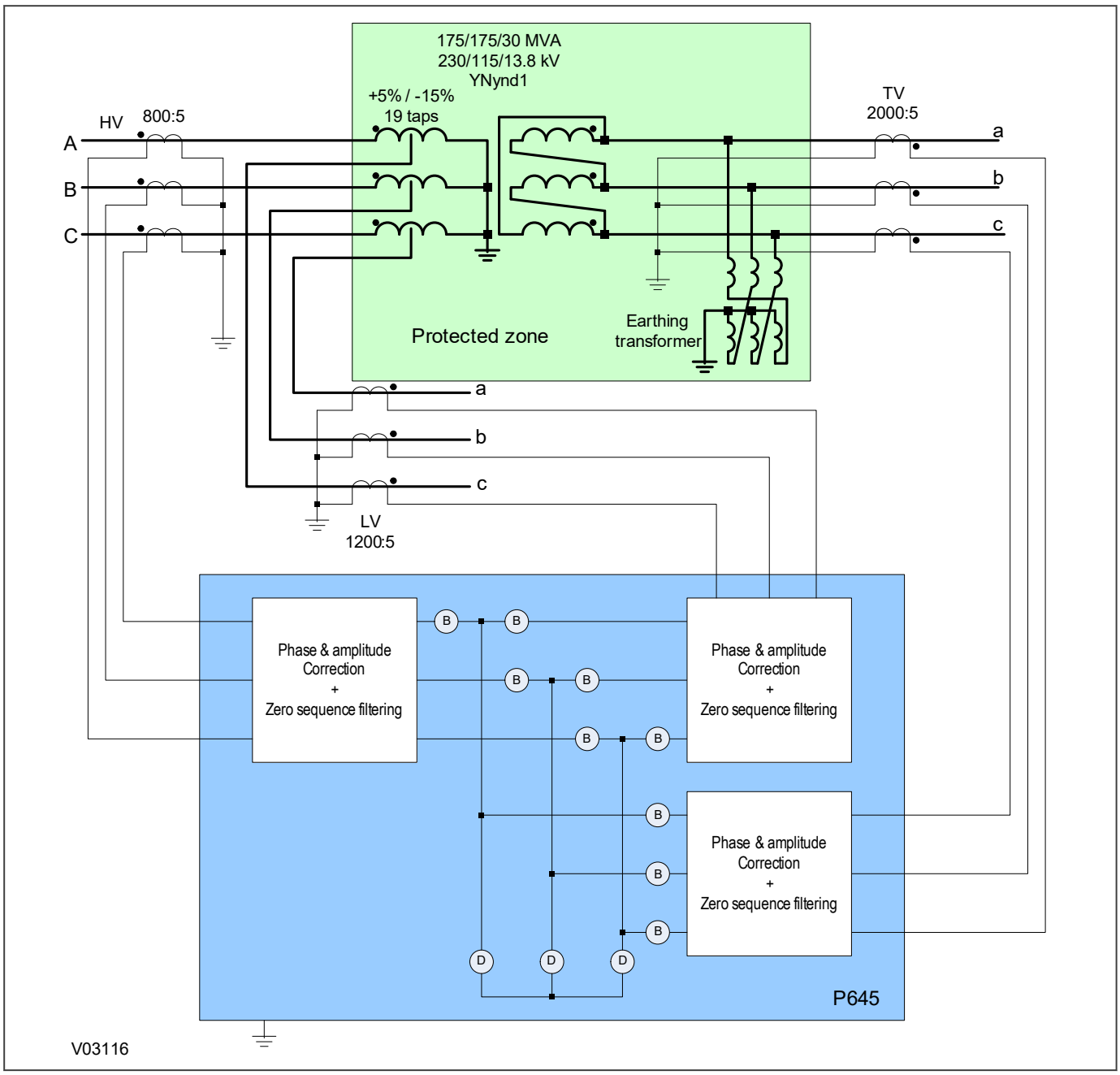


Figure 59: P645 used to protect an autotransformer with loaded delta winding

Since the transformer has an on load tap changer on the HV side, the nominal voltage of the HV winding must be set to the mid tap voltage level. According to the nameplate data, the mid tap voltage is 218.5 kV. The mid tap voltage can also be calculated as follows:

$$\text{Mid tap voltage} = \frac{100 + \frac{(5-15)}{2}}{100} \times 230 = 218.5kV$$

Set the following parameters in the *SYSTEM CONFIG* column:

Setting in GROUP 1 SYSTEM CONFIG	Value
Winding Config	HV+LV+TV
Winding Type	Auto
HV CT Terminals	00001
LV CT Terminals	10000
TV CT Terminals	00100
Ref Power S	175.00 MVA
Ref Vector Group	0
HV Connection	Y-Wye
HV Grounding	Grounded
HV Nominal	218.50 kV
HV Rating	175.00 MVA
% Reactance	10.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Grounded
LV Nominal	115.00 kV
LV rating	145.00 MVA
TV Vector Group	1
TV Connection	D-Delta
TV Grounding	Grounded
TV Nominal	13.800 kV
TV rating	30.00 MVA
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap

Vector correction and zero sequence filtering are automatically performed by virtue of the LV Vector Group setting and the ***HV Grounding*** and ***LV Grounding*** settings.

The device calculates the ratio correction factors as follows:

$$K_{amp,T1CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{800}{\frac{175\times10^6}{\sqrt{3}\times218.5\times10^3}} = 1.730$$

$$K_{amp,T5CT} = \frac{I_{nom,T5CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{1200}{\frac{175\times10^6}{\sqrt{3}\times115\times10^3}} = 1.366$$

$$K_{amp,T3CT} = \frac{I_{nom,T3CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,TV}}} = \frac{2000}{\frac{175\times10^6}{\sqrt{3}\times13.8\times10^3}} = 0.273$$

where:

- Sref = common reference power for all ends
- $K_{amp,\ T1CT,\ T2CT,\ T3CT}$ = ratio correction factor of T1 CT, T2 CT, or T3 windings
  $I_{nom,\ T1CT,\ T2CT,\ T3CT}$ = primary nominal currents of the main current transformers
- $V_{nom,\ HV,\ LV,\ TV}$ = primary nominal voltage of HV, LV, or TV windings

These matching factors are also displayed in the *SYSTEM CONFIG* column (***Match Factor CT1*** and ***Match Factor CT2***)

Now set the current differential parameters as follows:

Setting in GROUP 1 DIFF PROTECTION	Value
Trans Diff	Enabled
Set Mode	Advance
Is1	200.0e-3 PU
K1	30.00%
Is2	1.000 PU
K2	80.00%
tdiff	0 s
Is-CTS	1.500 PU
Is-HS1	10.00 PU
HS2 Status	Disabled
Zero seq filt HV	Enabled
Zero seq filt LV	Enabled
Zero seq filt TV	Enabled
IH2 Diff Block	Enabled
IH2 Diff Set	20%
Cross Blocking	Enabled
CT Saturation	Enabled

Setting in GROUP 1 DIFF PROTECTION	Value
No Gap	Enabled
IH5 Diff Block	Enabled
IH5 Diff Set	35%
Circuitry Fail	Disabled

6.5.4 EXAMPLE 3: AUTOTRANSFORMER WITH UNLOADED DELTA WINDING

Consider an autotransformer with the following specifications:

- Power rating: 175/175/30 MVA
- Connection type: YNyn0d1
- Voltage specification: 230/115/13.8 kV.
- HV CT ratio: 1200:5
- LV CT ratio: 1200:5
- Neutral CT ratio: 1200:5
- HV taps at +5% and -15%

The winding configuration is set to ***HV + LV + TV***. The CT on the HV line side is connected to T1 CT, the CT on the HV neutral side is connected to T2 CT, and the CT on the LV side is connected to T3 CT.

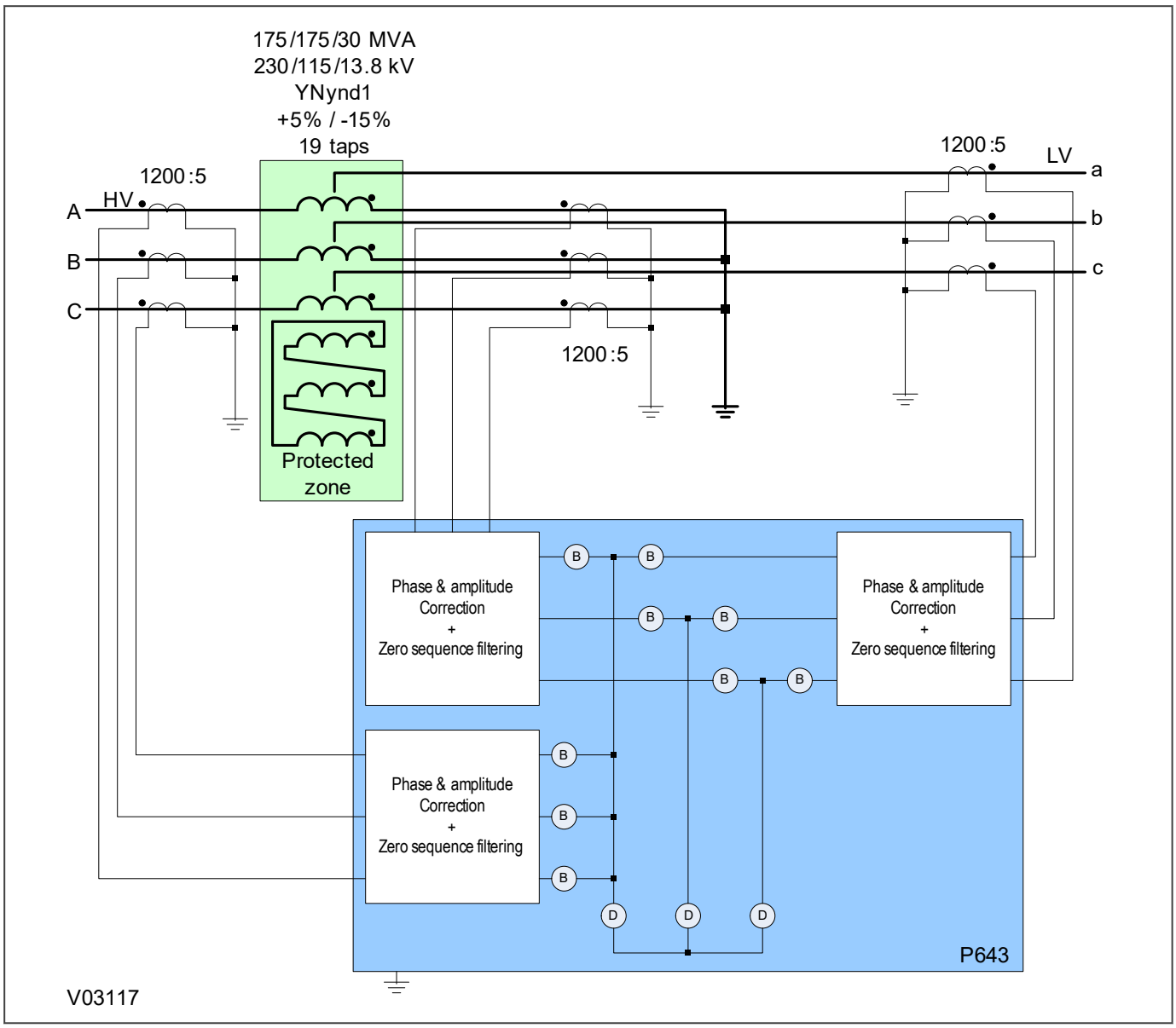


Figure 60: P643 used to protect an autotransformer with unloaded delta winding

Set the following parameters in the *SYSTEM CONFIG* column:

Setting in GROUP 1 SYSTEM CONFIG	Value
Winding Config	HV+LV+TV
Winding Type	Auto
HV CT Terminals	001
LV CT Terminals	100
TV CT Terminals	010
Ref Power S	175.00 MVA
Ref Vector Group	0
HV Connection	Y-Wye
HV Grounding	Ungrounded

Setting in GROUP 1 SYSTEM CONFIG	Value
HV Nominal	230.0 kV
HV Rating	175.00 MVA
% Reactance	10.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	230.00 kV
LV rating	175.00 MVA
TV Vector Group	0
TV Connection	Y-Wye
TV Grounding	Ungrounded
TV Nominal	230.0 kV
TV rating	175.0 MVA
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap
CT3 Reversal	No Swap

Vector correction and zero sequence filtering are automatically performed by virtue of the ***LV Vector Group*** setting and the ***HV Grounding*** and ***LV Grounding*** settings.

It is preferable to have the ratio correction factors equal to or close to 1.

Applying Kirchoff's law, assume that the full load current is flowing, that an equivalent source is connected to the HV winding and that an equivalent load is connected to the LV winding. The current distribution is as follows:

$$I_{FLC-HV} = \frac{S}{\sqrt{3}V_{nom,HV}} = \frac{175\times10^{6}}{\sqrt{3}\times230\times10^{3}} = 439A$$

$$I_{FLC-LV} = \frac{S}{\sqrt{3}V_{nom,LV}} = \frac{175\times10^{6}}{\sqrt{3}\times115\times10^{3}} = 878A$$

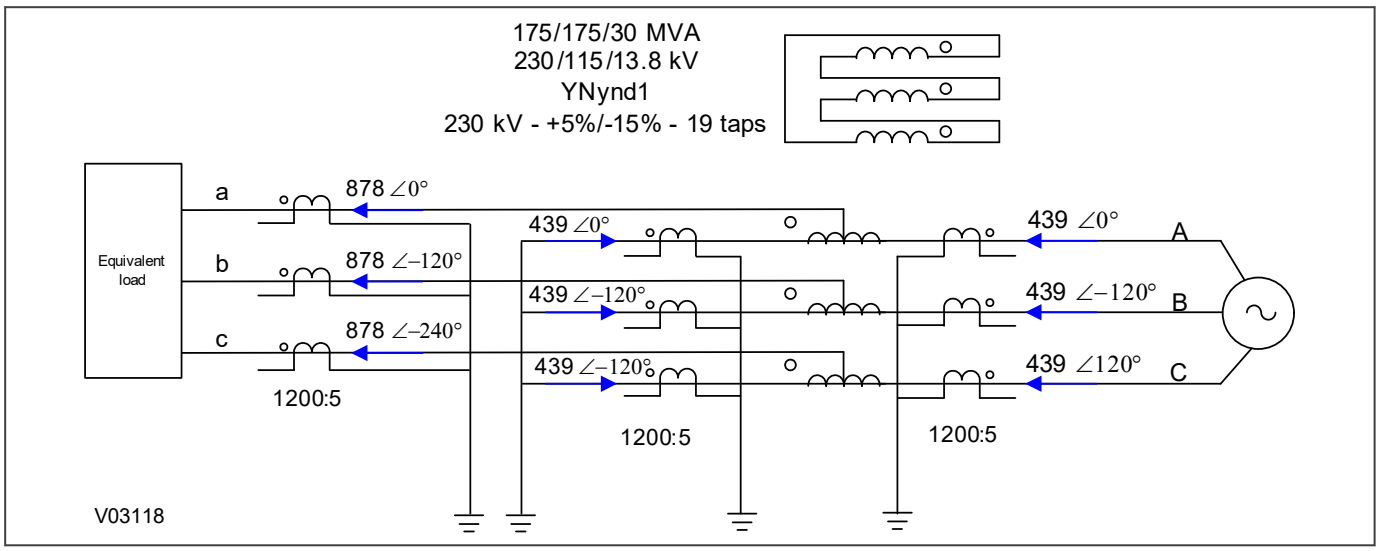


Figure 61: Unloaded delta – current distribution

The reference power is set to 175 MVA and the nominal voltage in HV, LV and TV windings is set to 230 kV. In this application, you do not need to consider the mid tap voltage, even though, there is an on load tap changer on the HV side.

The device calculates the ratio correction factors as follows:

$$K_{amp,T1CT} = K_{amp,T2CT} = K_{amp,T3CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom}}} = \frac{1200}{\frac{175\times10^{6}}{\sqrt{3}\times230\times10^{3}}} = 2.73$$

Now set the current differential parameters as follows:

Setting in GROUP 1 DIFF PROTECTION	Value
Trans Diff	Enabled
Set Mode	Advance
Is1	200.0e-3 PU
K1	20.00%
Is2	1.000 PU
K2	80.00%
tdiff	0 s
Is-CTS	1.500 PU
Is-HS1	10.00 PU
HS2 Status	Disabled
Is-HS2	32.00 PU
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
Zero seq filt TV	Disabled
IH2 Diff Block	Enabled
IH2 Diff Set	20%

Setting in GROUP 1 DIFF PROTECTION	Value
Cross Blocking	Enabled
CT Saturation	Enabled
No Gap	Enabled
IH5 Diff Block	Enabled
IH5 Diff Set	35%
Circuitry Fail	Disabled

The differential element does not protect the tertiary winding. Unloaded delta-connected tertiary windings are often not protected. If protection is required, the delta winding can be earthed at one point through a current transformer used to provide instantaneous overcurrent protection for the tertiary winding.

6.5.5 SETTING GUIDELINES FOR SHORT-INTERCONNECTED BIASED DIFFERENTIAL PROTECTION

The P645 can be used to protect busbars. Consider the five feeders - single bus scheme and its differential protection zone shown below:

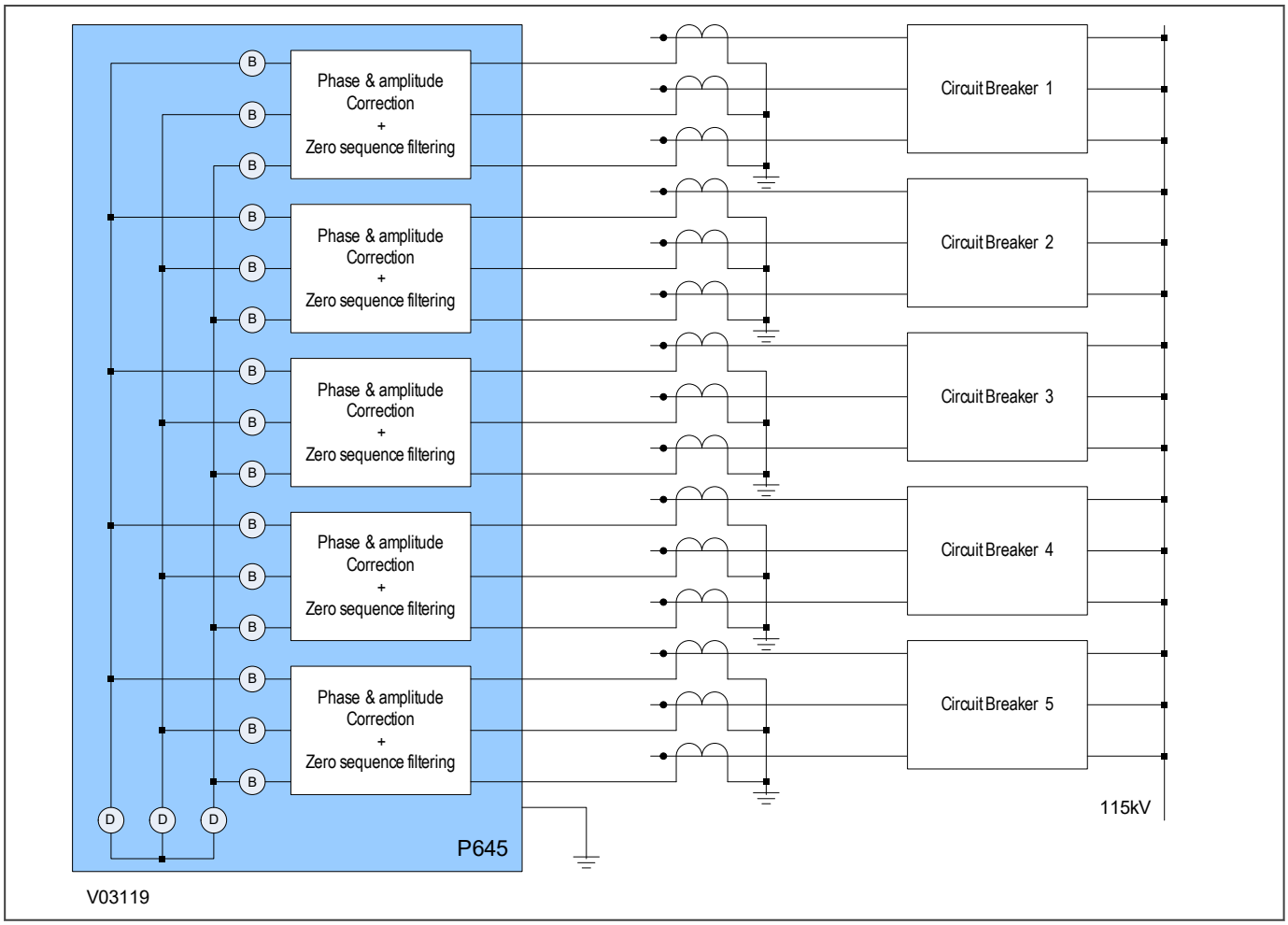


Figure 62: Single bus differential protection zone

Assume that feeder CTs 1 to 5 are connected to inputs T1 to T5 respectively.

Set the following parameters in the *SYSTEM CONFIG* column:

Setting in GROUP 1 SYSTEM CONFIG	Value
Winding Config	HV+LV+TV
Winding Type	Conventional
HV CT Terminals	01111
LV CT Terminals	10000
Ref Power S	145.0 MVA*
Ref Vector Group	0
HV Connection	Y-Wye
HV Grounding	Ungrounded**
HV Nominal	115.0 kV***
HV Rating	145.0 MVA****
% Reactance	10.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded**
LV Nominal	115.0 kV***
LV rating	145.00 MVA****
TV Vector Group	0
TV Connection	Y-Wye
TV Grounding	Ungrounded**
TV Nominal	115.0 kV***
TV rating	145.0 MVA****

Note:
** This is the maximum load (including overloads) that would be handled by the busbar.*

Note:
*** This disables the zero sequence filters.*

Note:
**** This is the system voltage.*

Note:
***** This setting has no impact on the differential protection. It is used by other functions such as the thermal and through-fault monitoring elements which are not required for busbar protection.*

Now set the current differential parameters as follows:

Setting in GROUP 1 DIFF PROTECTION	Value
Trans Diff	Enabled
Set Mode	Advance

Setting in GROUP 1 DIFF PROTECTION	Value
Is1	1.200 PU
K1	20.00%
Is2	400.0e-3 PU
K2	80.00%
tdiff	0 s
Is-CTS	1.500 PU
Is-HS1	10.00 PU
HS2 Status	Disabled
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
IH2 Diff Block	Disabled
IH5 Diff Block	Disabled
Circuitry Fail	Enabled
Is-cctfail	100.0e-3 PU
K-cctfail	10.00%
Cctfail Delay	5.000 s

Note:
Set the Circuitry Fail alarm to Enabled and set K-cctfail to 15% to allow the maximum composite error of 10% that may be introduced by class 10P current transformers. Is-cctfail is typically set between 5 to 20% to prevent CT noise and differential current caused by load imbalance. This element is typically delayed by 5 s.

Note:
CT supervision should be used to prevent maloperation if there is an open circuited CT secondary. The CTS feature can be used to desensitize the biased differential protection. To do this, raise the differential current pickup setting Is1 to the value of Is-CTS.

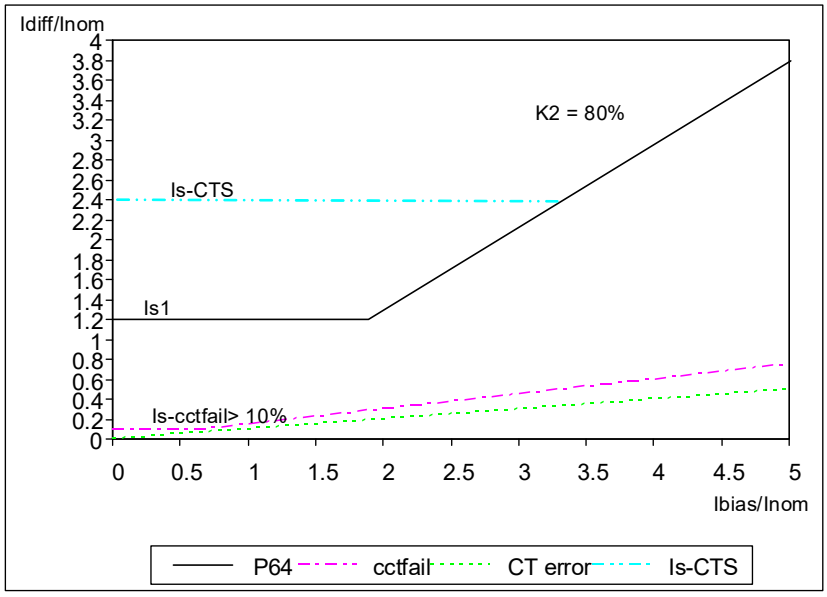


Figure 63: Busbar biased differential protection

6.5.6 SETTING GUIDELINES FOR SHUNT REACTOR BIASED DIFFERENTIAL PROTECTION

Shunt reactors are commonly used in the power system to compensate for the capacitive reactance of long transmission lines. Shunt reactors are inductive loads that are used to absorb reactive power to reduce the over voltages generated by line capacitance.

One of the main difficulties with shunt reactor protection is that the protection IED may maloperate during iron-core reactor energization and de-energization. A shunt reactor is typically switched in and out regularly depending on the power system load. The iron-core shunt reactor energization current contains a DC offset with a long time constant (up to 1 second) and low frequency components. These current waveforms cause a certain level of flux in the CT magnetic core. During normal reactor operation the current is generally the nominal current, which is not high enough to reduce the flux level in the CT. In the next switch in operation, the flux may either increase or decrease depending on the point o on the wave when energization occurs. The regular switching in and out of the reactor causes CT saturation; therefore, we recommend that the current transformers on both sides of the reactor have similar excitation characteristics to reduce the risk of maloperations. A high impedance differential scheme is generally better than a low impedance differential scheme, because it is not affected by CT saturation.

As per IEEE C37.109-2006 the properties of shunt reactors can be summarized as follows:

- Dry air-air core type reactors: no magnetizing inrush during energization as there is no iron core. The peak current during energization might be as high as 2 $\sqrt{2}I_{nominal}$ due to transient offset. Air core type reactors are normally used up to 34.5 kV and often installed on the transformer tertiary winding.
- Oil-immersed type reactors: the gapped iron-core type might experience severe energizing inrush. The coreless type experiences less severe magnetizing inrush.

Consider the following shunt reactor:

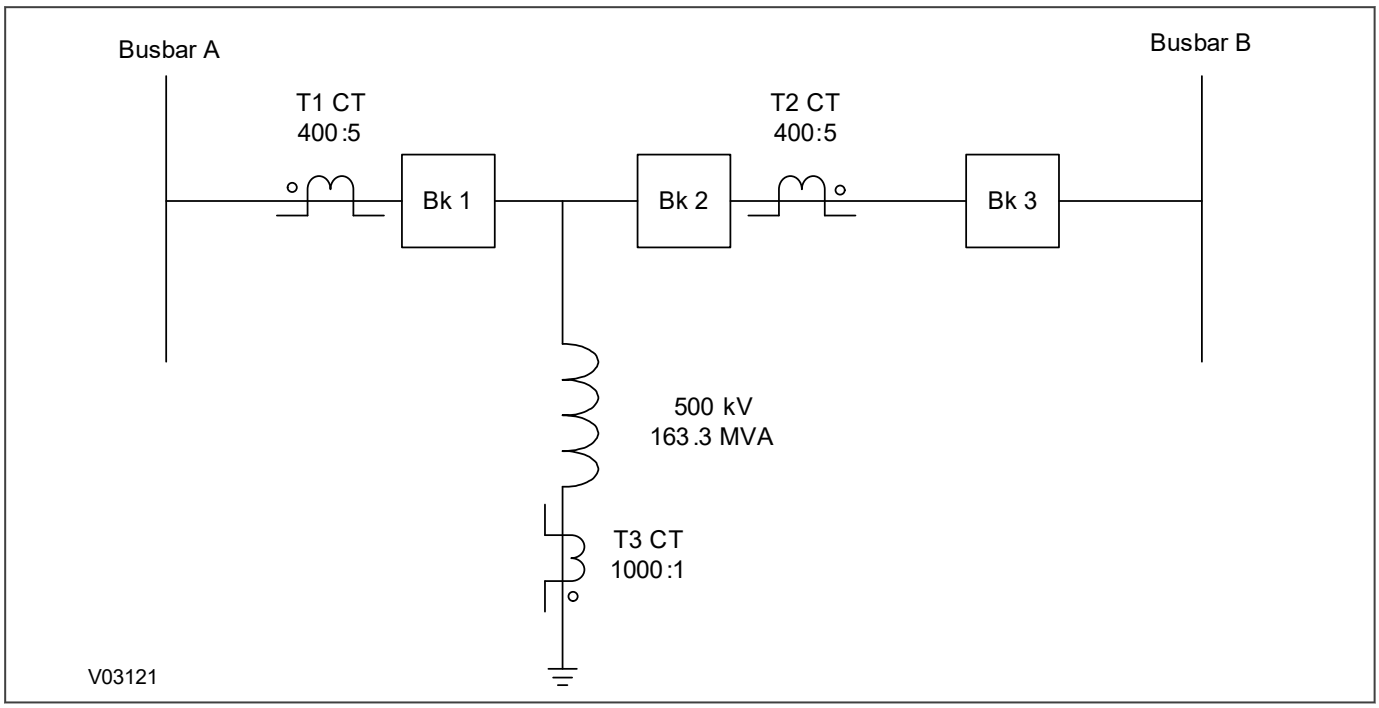


Figure 64: Shunt Reactor single line diagram

The bias differential element in the P643 would be used to protect the reactor. In a reactor application the low set differential element ***Is1***, should be set between 10%-15%. Inrush current in a shunt reactor does not appear as a differential current like that which appears in a transformer, unless the CT saturates after some time due to long DC time constant. Though the level of second harmonic in many cases can be relatively high, there are many cases with no or very low content of harmonics in the differential current. Since the level of 2nd harmonic is small in shunt reactors compared with transformers, the high set 1 differential element, ***Is-HS1***, can be set to 250% of the reactor current at rated voltage.

Set the following parameters in the *SYSTEM CONFIG* column:

Setting in GROUP 1 SYSTEM CONFIG	Value
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	011
LV CT Terminals	100
Ref Power S	163.3 MVA
Ref Vector Group	0
HV Connection	Y-Wye
HV Grounding	Ungrounded
HV Nominal	500.0 kV
HV Rating	163.3 MVA
% Reactance	40.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	115.0 kV
LV rating	163.3 MVA

Setting in GROUP 1 SYSTEM CONFIG	Value
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap
CT3 Reversal	No Swap

Now set the current differential parameters as follows:

Setting in GROUP 1 DIFF PROTECTION	Value
Trans Diff	Enabled
Set Mode	Simple
Is1	100.0e-3 PU
K1	30.00%
Is2	1.000 PU
K2	80.00%
tdiff	0 s
Is-CTS	1.500 PU
Is-HS1	2.500 PU
HS2 Status	Disabled
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
IH2 Diff Block	Disabled
Cross blocking	Enabled
CT Saturation	Disabled
No Gap	Disabled
IH5 Diff Block	Disabled
Circuitry Fail	Disabled

6.5.7 SETTING GUIDELINES FOR USING SPARE CT INPUTS

The P643 and P645 can be configured to protect transformers for differential protection and the unused CT inputs can be used to protect other circuits. For example the P643 can use 2 of the 3 phase CT inputs to provide differential protection of a 2 winding transformer by setting ***Winding Config*** to *HV+LV* and the unused 3rd 3 phase current input can be used to provide overcurrent protection on another circuit such as an auxiliary transformer, as shown below:

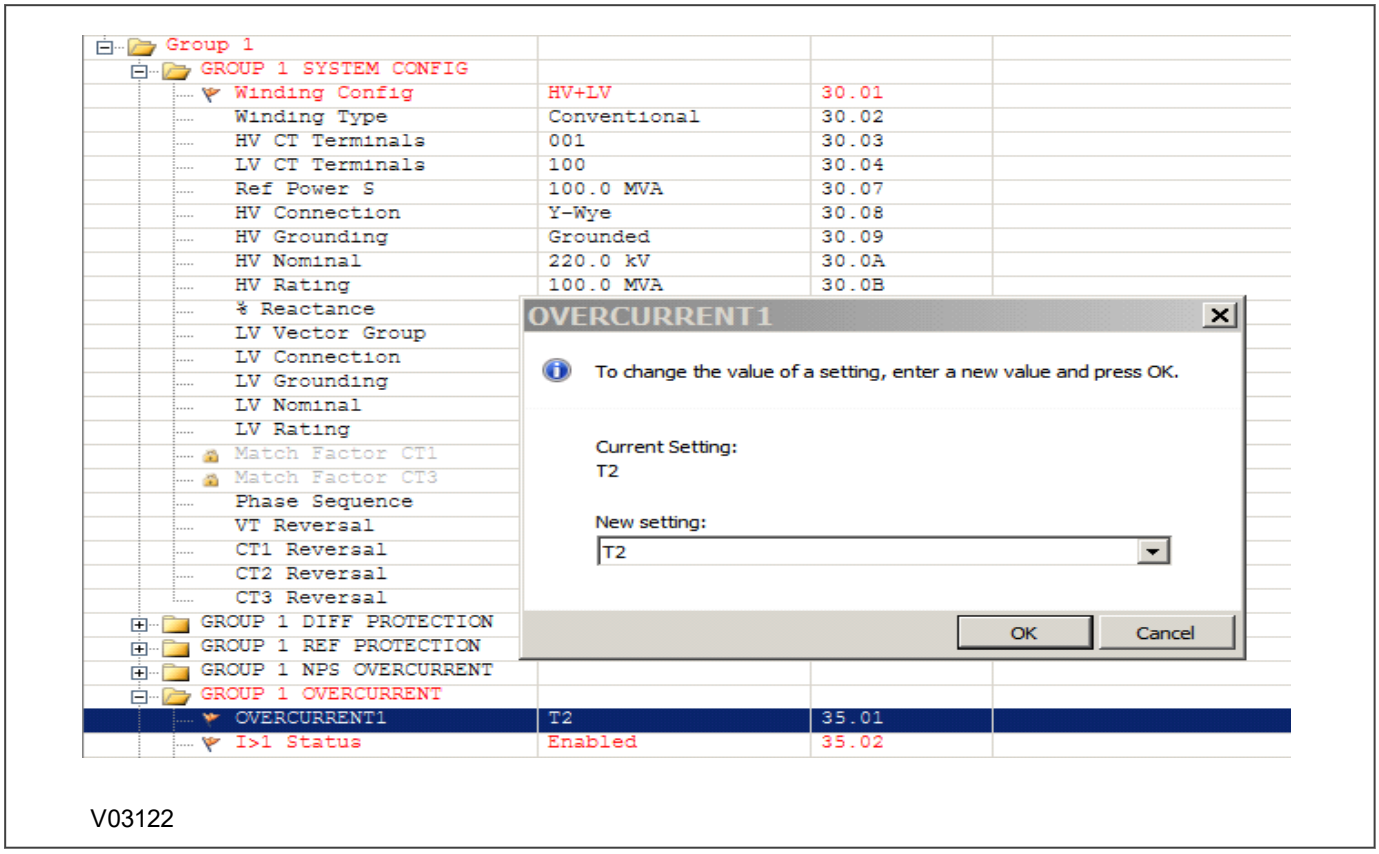


Figure 65: P643 Using spare CT input for overcurrent protection

6.5.8 SETTING GUIDELINES FOR REFERENCE VECTOR GROUP

The following table shows how to set the zero sequence filter for the different Ref Vector Group options.

Ref Vector Group	Zero Seq Filt HV Setting	Zero Seq Filt LV Setting	Zero Seq Filt TV Setting
0	Enabled	Disabled	Disabled
1	Disabled	Disabled	Enabled
2	Enabled	Enabled	Disabled
3	Disabled	Disabled	Enabled
4	Enabled	Disabled	Disabled
5	Disabled	Disabled	Enabled
6	Enabled	Disabled	Disabled
7	Disabled	Disabled	Enabled
8	Enabled	Disabled	Disabled
9	Disabled	Disabled	Enabled
10	Enabled	Disabled	Disabled
11	Disabled	Disabled	Enabled

In the majority of applications, the reference vector group setting ***Ref Vector Group*** is set to 0. However there are occasional applications where it may be desirable to set it to a value other than 0.

One example is to increase the sensitivity for phase-to-phase faults where it is used to protect a YNyn0 transformer. In this scenario, the P64 would normally apply a -30° phase shift to both HV and LV windings due to the way it works. However, by setting the reference vector group to 1, the device knows it does not have to apply a -30° shift in its calculations, thus increasing its sensitivity to phase-to-phase faults.

6.5.9 STUB BUS APPLICATION

When a winding isolator is open (e.g. for maintenance purposes), a section of energized line, called the stub, could be left unprotected. In the diagram below, we see that the HV winding disconnector is open and there is a fault in the stub zone, which needs to be protected against.

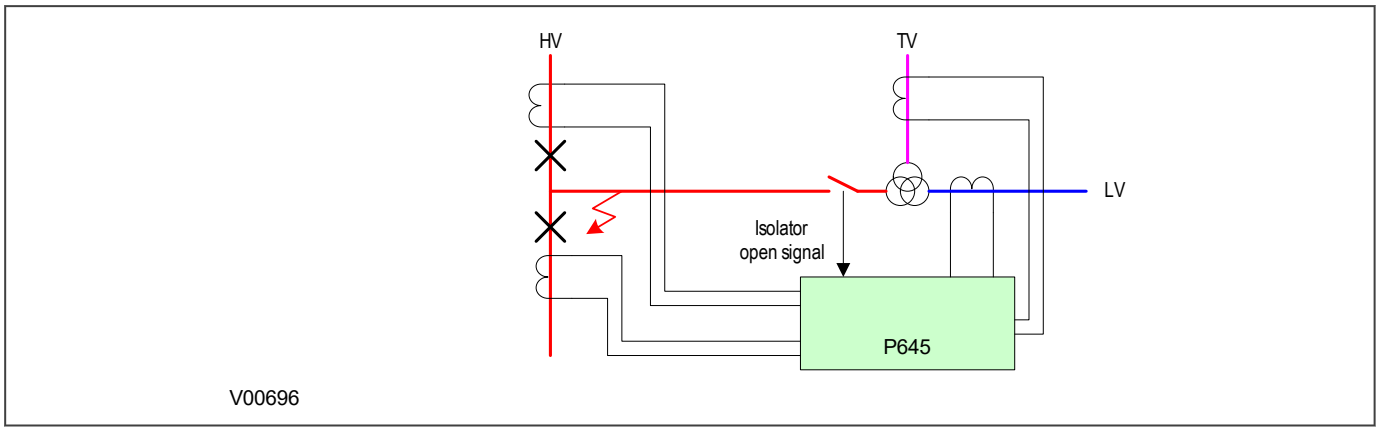


Figure 66: Stub Bus arrangement

We do not want the standard differential protection or low impedance REF protection to operate, as this may have repercussions on the rest of the system. In this case, Stub Bus protection should be used, when available. Stub Bus protection is achieved by using the isolator status , applying this to an opto-input and combining it with a phase overcurrent element (linked to the relevant winding) to provide a trip signal for the relevant circuit breakers.

6.5.9.1 STUB BUS IMPLEMENTATION

When the protection is used in one and half breaker busbar topology and the disconnector of any of the three windings of the transformer is open, the differential and low impedance REF elements related to this winding are affected.

The differential and low impedance REF protection elements should not trip for a stub bus fault and should be blocked on a per winding basis.

6.5.9.1.1 STUB BUS ACTIVATION

The Stub Bus active signals ***HV StubBus Act***, ***LV StubBus Act*** and ***TV StubBus Act*** are asserted when the appropriate conditions are met to activate Stub Bus for the relevant winding. A fast under current DDB signal, available on a per winding basis along with the isolator status, should be used to assert the respective Stub Bus active signal. The fast under current DDB will become asserted if the current measured falls below the ***I< Current Set*** of the relevant CBF element. For the fast undercurrent DDBs, ***I< Current Set*** represents a percentage of the CT secondary nominal current (In). CBF does not need to be activated for the fast under current DDB to assert.

6.5.9.1.2 STUB BUS DIFFERENTIAL BLOCKING

When a Stub Bus active signal is asserted for a winding, the current of the respective winding is not considered in the calculation of the differential and bias currents. The differential trip is not blocked however, and should be blocked on the winding with Stub Bus active only (it should remain unblocked on the other windings). For example, if a fault occurs within the differential zone and the HV Stub Bus is active, the differential element should only trip the breakers connected to the LV and TV sides of the transformer. In this case, blocking of the HV winding differential trip in can be achieved via the PSL logic.

Low impedance REF protection is blocked internally on a per winding basis by the fixed scheme logic. For example, if HV StubBus Act is activated, then HV low impedance REF is blocked.

In applications where the protection is per differential scheme, the Stub Bus protection cannot be used since the differential protection trip will be blocked each time any Stub Bus is activated.

6.5.9.1.3 STUB BUS TRIPPING

You can protect the Stub Bus zone by a non-directional DT phase overcurrent element with a delay time set to zero second. To issue a Stub Bus trip, the overcurrent element and the relevant Stub Bus active DDB signals must both be high. You can configure the Stub Bus tripping scheme in PSL.

6.5.9.2 STUB BUS SCHEME

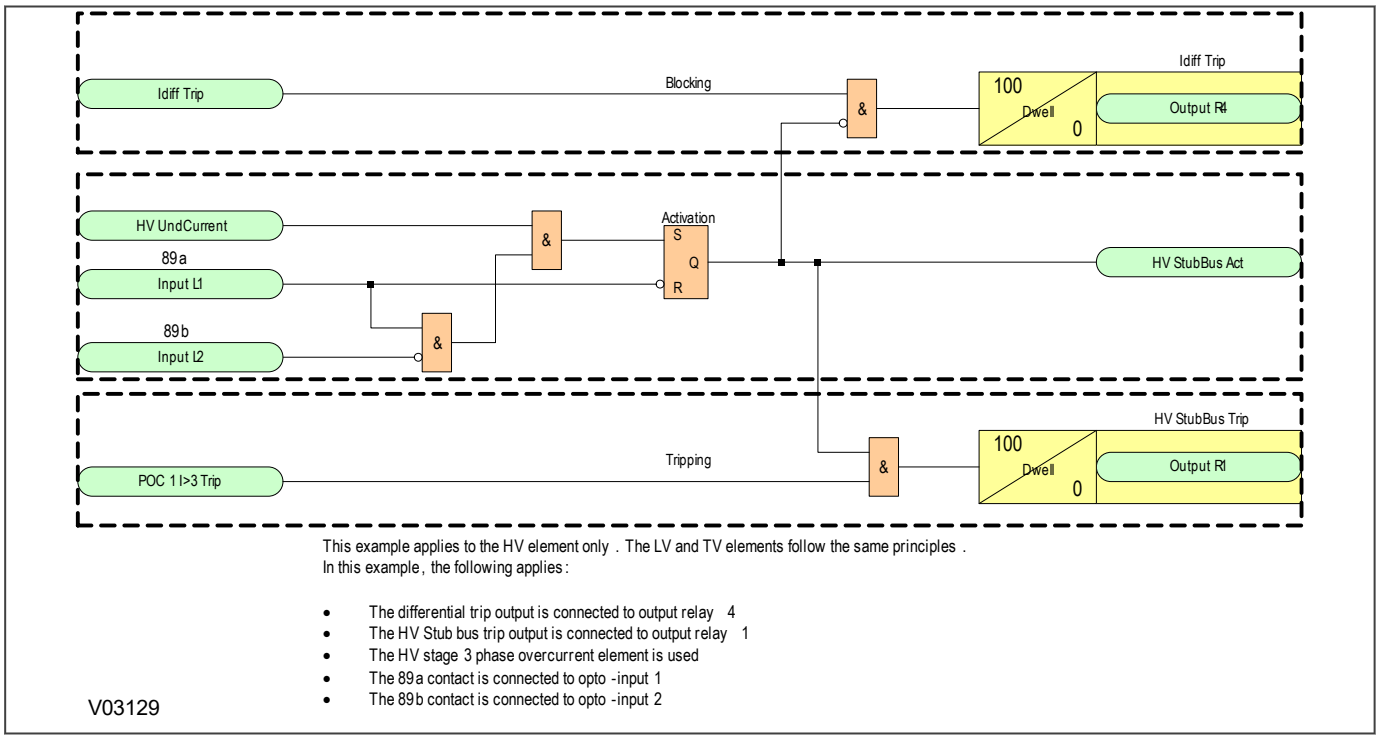


Figure 67: Stub Bus Scheme Logic

6.5.10 TRANSFORMER DIFFERENTIAL PROTECTION CT REQUIREMENTS

The CT requirements detailed below are applicable to both standard CTs and sensitive CTs.

6.5.10.1 CT REQUIREMENTS - TRANSFORMER APPLICATION

We strongly recommend Class X or Class 5P current transformers for transformer differential protection applications.

The current transformer knee-point voltage requirements are based on the following settings:

Parameter	Description	Value
Is1	This sets the minimum differential current threshold required for the transformer differential protection to trip.	0.2 pu
Is2	This defines the bias current threshold at which the second slope of the bias current characteristic becomes active.	1 pu
K1	This setting defines the gradient of the first slope in the bias current characteristic.	30%

Parameter	Description	Value
K2	This setting defines the gradient of the second slope in the bias current characteristic.	80%
Is-HS1	This setting defines the first High set threshold on the bias current characteristic. This setting is only used in advanced mode.	10 pu
Is-HS2	This setting defines the second High set threshold on the bias current characteristic. This setting is only used in advanced mode.	32 pu
Transient Bias	This setting enables or disables the transient bias factor	Enabled
Zero seq filt HV	This setting enables or disables zero sequence filtering on the HV winding	Enabled
Zero seq filt LV	This setting enables or disables zero sequence filtering on the LV winding	Enabled
Zero seq filt TV	This setting enables or disables zero sequence filtering on the TV winding	Enabled
IH2 Diff Set	This setting defines the second harmonic blocking threshold.	20%
Cross blocking	This setting enables or disables cross blocking (cross blocking is where a 2nd harmonic blocking signal from any one phase, blocks all three phases).	Enabled
CT Saturation	This setting enables or disables CT saturation detection.	Enabled
No Gap	This setting enables or disables CT Gap detection.	Enabled
IH5 Diff Set	This setting defines the fifth harmonic blocking threshold.	35%

The following table provides the maximum sensitivity and its corresponding matching factor for different CT types:

CT Type	Max. Sensitivity	Permitted Matching Factor Range	Matching Factor for Typical Setting Is1 = 0.2 pu
Standard	43 mA	0.05 - 15	4.65
Sensitive	13 mA	0.05 - 20	15.38

A series of external faults were simulated to determine the CT requirements for the differential function, by using a state of the art Real Time Digital Simulation system (RTDS). We performed these tests with different X/R ratios, CT burdens, fault currents, fault types and points on the current waveform.

To achieve through-fault stability, the K dimensioning factor must comply with the following expressions:

System Conditions	K	Kneepoint Voltage (VK)
$In < I_F <= 40In$ $5 <= X/R <= 20$	16	$V_K => 16In(R_{CT} + 2R_L + R_r)$ (earth fault) $V_K => 16In(R_{CT} + R_L + R_r)$ (phase fault)
$40In < I_F <= 64In$ $5 <= X/R <= 20$	30	$V_K => 30In(R_{CT} + 2R_L + R_r)$ (earth fault) $V_K => 30In(R_{CT} + R_L + R_r)$ (phase fault)
$In < I_F <= 40In$ $20 <= X/R <= 120$	17	$V_K => 17In(R_{CT} + 2R_L + R_r)$ (earth fault) $V_K => 17In(R_{CT} + R_L + R_r)$ (phase fault)
$40In < I_F <= 64In$ $20 <= X/R <= 120$	34	$V_K => 34In(R_{CT} + 2R_L + R_r)$ (earth fault) $V_K => 34In(R_{CT} + R_L + R_r)$ (phase fault)

where:

- V_K = kneepoint voltage
- K = CT dimensioning factor

- I_n = rated current
- R_{CT} = resistance of CT secondary winding
- R_L = resistance of a single lead from device to current transformer
- R_r = resistance of any other protection devices sharing the current transformer
- I_F = maximum external fault level

6.5.10.2 CT REQUIREMENTS - SMALL BUSBAR APPLICATION

We strongly recommend Class X or Class 5P current transformers for this application.

The current transformer knee-point voltage requirements are based on the following settings:

Parameter	Description	Value
Is1	This sets the minimum differential current threshold required for the transformer differential protection to trip.	1.2 pu
Is2	This defines the bias current threshold at which the second slope of the bias current characteristic becomes active.	0.4 pu
K1	This setting defines the gradient of the first slope in the bias current characteristic.	20%
K2	This setting defines the gradient of the second slope in the bias current characteristic.	80%
Is-HS1	This setting defines the first High set threshold on the bias current characteristic. This setting is only used in advanced mode.	10 pu
Is-HS2	This setting defines the second High set threshold on the bias current characteristic. This setting is only used in advanced mode.	Disabled
Transient Bias	This setting enables or disables the transient bias factor	Enabled
Zero seq filt HV	This setting enables or disables zero sequence filtering on the HV winding	Disabled
Zero seq filt LV	This setting enables or disables zero sequence filtering on the LV winding	Disabled
Zero seq filt TV	This setting enables or disables zero sequence filtering on the TV winding	Disabled
IH2 Diff Set	This setting defines the second harmonic blocking threshold.	Disabled
CT Saturation	This setting enables or disables CT saturation detection.	Disabled
No Gap	This setting enables or disables CT Gap detection.	Disabled
IH5 Diff Set	This setting defines the fifth harmonic blocking threshold.	Disabled

A series of internal and external faults were simulated to determine the CT requirements for the differential function. We performed these tests with different X/R ratios, CT burdens, fault currents, fault types and points on the current waveform.

The system conditions, CT dimensioning factor and CT kneepoint voltage are as follows:

System Conditions	K	Kneepoint Voltage (VK)
$In < I_F <= 40In$ $5 <= X/R <= 20$	16	$VK => 16In(R_{CT} + 2R_L + R_r)$ (earth fault) $VK => 16In(R_{CT} + R_L + R_r)$ (phase fault)
$40In < I_F <= 64In$ $5 <= X/R <= 20$	30	$VK => 30In(R_{CT} + 2R_L + R_r)$ (earth fault) $VK => 30In(R_{CT} + R_L + R_r)$ (phase fault)
$In < I_F <= 40In$ $20 <= X/R <= 120$	21	$VK => 21In(R_{CT} + 2R_L + R_r)$ (earth fault) $VK => 21In(R_{CT} + R_L + R_r)$ (phase fault)
$40In < I_F <= 64In$ $20 <= X/R <= 120$	30	$VK => 30In(R_{CT} + 2R_L + R_r)$ (earth fault) $VK => 30In(R_{CT} + R_L + R_r)$ (phase fault)

where:

- V_K = kneepoint voltage
- K = CT dimensioning factor
- I_n = rated current
- R_{CT} = resistance of CT secondary winding
- R_L = Resistance of a single lead from device to current transformer
- R_r = resistance of any other protection devices sharing the current transformer
- I_F = maximum external fault level

CHAPTER 7

TRANSFORMER CONDITION MONITORING

7.1 CHAPTER OVERVIEW

This chapter contains the following sections:

Chapter Overview 144
Thermal Overload Protection 145
Loss of Life Statistics 152
Through Fault Monitoring 156
RTD Protection 160
CLIO Protection 162

7.2 THERMAL OVERLOAD PROTECTION

Transformer overheating can be caused due to failures of the cooling system, external faults that are not cleared promptly, or overload and abnormal system conditions. These abnormal conditions include low frequency, high voltage, non-sinusoidal load current, or phase-voltage imbalance.

Overheating shortens the life of the transformer insulation in proportion to the duration and magnitude of the high temperature. If excessive, this may even result in an immediate insulation failure. Overheating can also generate gases that could result in electrical failure, or cause the transformer coolant to be heated above its flashpoint temperature, introducing the risk of fire.

Studies suggest that the life of insulation is approximately halved for each 10°C rise in temperature above the rated value. However, the life of insulation is not wholly dependent on the rise in temperature but on the time the insulation is subjected to this elevated temperature. Due to the relatively large heat storage capacity of a transformer, infrequent overloads of short duration may not damage it. However, sustained overloads of a few percent may result in premature aging and consequent insulation failure.

Transformer thermal overload protection is designed to protect equipment from sustained overload. Thermal overload protection allows modest but transient overload conditions to occur, while tripping for sustained overloads, which would not be detected by standard overcurrent protection.

Transformer Losses

The losses in a transformer are shown in the following diagram:

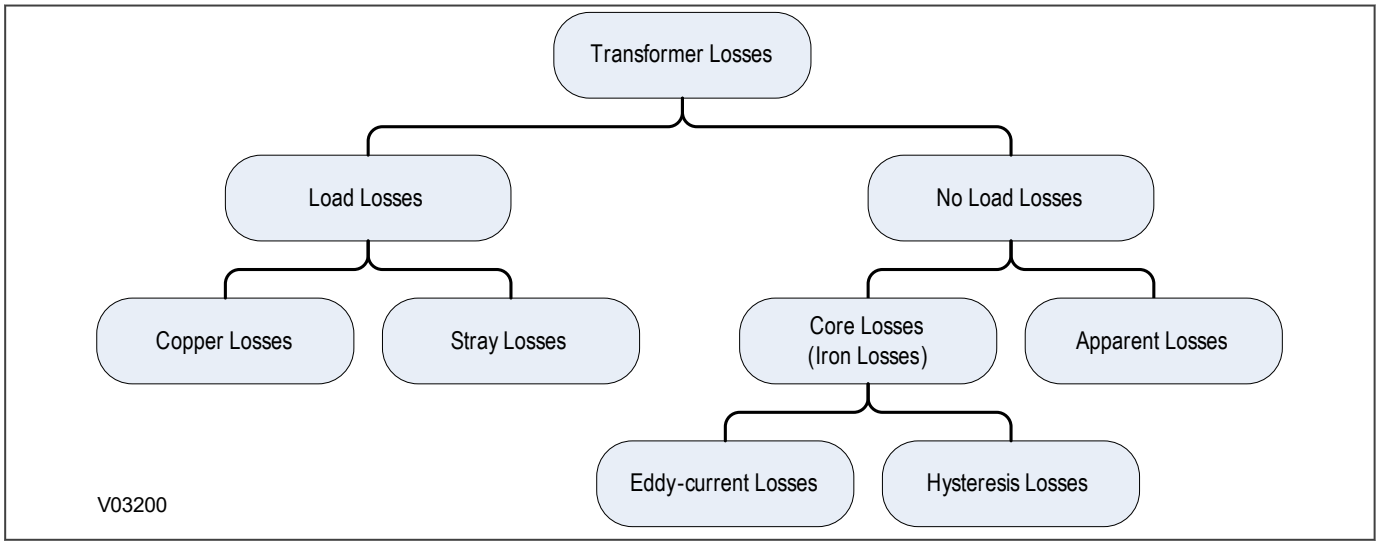


Figure 68: Transformer losses

The flow of the magnetising current through the resistance of the winding creates a real but generally relatively small I^2R loss and voltage drop. The loss that is due to this magnetizing current in the primary winding is called the apparent loss.

Time-varying fluxes in iron-based materials, cause losses called core losses, or iron losses. These iron losses are divided into two categories; hysteresis losses and eddy-current losses.

The sum of copper losses and the stray losses is called the load loss. Copper losses are due to the flow of load currents through the primary and secondary windings. They are equal to I^2R, and they heat up the wires and cause voltage drops. Stray losses are due to the stray capacitance and leakage inductance. Stray capacitance exists between turns, between one winding and another, and between windings and the core.

7.2.1 THERMAL OVERLOAD IMPLEMENTATION

The thermal overload protection in this device is based on the IEEE Standard C57.91-1995. It provides thermal overload protection for either an individual winding or the transformer as a whole. The thermal overload protection settings are in the *THERMAL OVERLOAD* column.

For individual windings, you set the ***MonitoredWinding*** setting to `HV, LV, TV` accordingly. If you wish to protect the transformer as a whole set the ***MonitoredWinding*** setting to `Biased Current`, which provides an overall loading picture of the transformer.

The device provides two 3-stage Definite Time delayed trip elements; one element for Hotspot temperature and one for Top Oil temperature. Top Oil temperature can be calculated, or measured directly using CLIO or RTD methods, but Hotspot temperature is always calculated.

A pre-trip alarm can be configured in the ***tPre-trip Set*** setting. This alarm indicates that thermal overload will trip after the set time if the load level remains unchanged.

Four cooling modes are available. You can set the oil exponent constant and winding exponent constant independently for each mode. You can set the cooling mode automatically in the PSL or manually in the setting file. For the latter, you will need to configure two opto-inputs as ***CM Select 1X*** and ***CM Select X1***, and you must wire the contacts to energise or de-energise these inputs. The selected cooling mode would then be as follows:

CM Select 1X	CM Select X1	Selected Cooling Mode
0	0	1
0	1	2
1	0	3
1	1	4

To calculate the Top Oil and hotspot winding temperature, the device takes into consideration the ratio of the actual load to the rated load. If the monitored winding is set to `HV`, `LV`, or `TV`, the rated load is determined by the ***HV rating***, ***LV rating***, or ***TV rating*** settings respectively and the ***Irated*** setting. If the monitored winding is set as the the biased current, the rated load is calculated using the ***Sref*** power rating setting in the *SYSTEM CONFIG* column and the ***Irated*** setting in the *THERMAL PROTECTION* column.

The thermal overload model is executed once every power cycle. The thermal overload trip can be based on either hot spot temperature or top oil temperature, or both.

The device has up to three hot spot stages and up to three top oil stages. The tripping signal, **Top Oil T>x Trip**, is asserted when the top oil (measured or calculated) temperature is above the setting, ***Top Oil>x Set***, and the time delay, ***tTop Oil>x*** Set has elapsed. Also, the tripping signal, ***Hotspot>x Trip***, is asserted when the hottest-spot (calculated only) temperature is above the setting, ***Hotspot>x*** Set, and the time delay, ***tHotspot>x Set*** has elapsed.

7.2.1.1 THERMAL OVERLOAD BIAS CURRENT

The biased current used by the thermal protection is not the same as the biased current used by the differential protection. No vector correction or zero sequence filtering is performed. To calculate the bias current, the thermal element considers the maximum RMS current on a per winding basis. Note that the bias current calculation performed by the thermal element is not on a per-phase basis. The thermal bias current calculation is as follows:

$$I_{bias} = \frac{\frac{Max\lfloor I_{HVArms}, I_{HVBrms}, I_{HVCrms} \rfloor}{HV\_FLC_{Sref}} + \frac{Max\lfloor I_{LVArms}, I_{LVBrms}, I_{LVCrms} \rfloor}{LV\_FLC_{Sref}} + \frac{Max\lfloor I_{TVArms}, I_{TVBrms}, I_{TVCrms} \rfloor}{TV\_FLC_{Sref}}}{2}$$

where:

- HV_FLC_{Sref} = HV full load current at the reference power
- LV_FLC_{Sref} = LV full load current at the reference power
- TV_FLC_{Sref} = TV full load current at the reference power

7.2.2 THE THERMAL MODEL

The simplest implementation of overload protection employs an I^2t characteristic. You set time constants such as the winding time constant at Hotspot location and top oil rise time constant, so that the thermal model can follow the correct exponential heating and cooling profile. Transformer loads are becoming increasingly non-linear; therefore the device uses true RMS current values to replicate the winding Hotspot temperature.

Note:
"True RMS" refers to the RMS value of a non-sinusoidal waveform including the fundamental and all other components.

7.2.2.1 TOP OIL TEMPERATURE CACULATIONS

If the Top Oil temperature is not available as a measured input quantity, it is calculated every cycle by the following equation:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

where:

- Θ_{TO} = Top Oil temperature
- Θ_A = Ambient temperature
- $\Delta\Theta_{TO}$ = Top Oil rise over ambient temperature due to a step load change

You can either measure the ambient temperature directly, or set it in the Ambient T setting. The ultimate top oil rise is given by the following equation:

$$\Delta\Theta_{TO,U} = \Delta\Theta_{TO,R} \cdot \left[\frac{K_u^2 R + 1}{R + 1} \right]^n$$

where:

K_u = the ratio of actual load to rated load

R = the ratio of the load loss at rated load to no load loss (***Rated NoLoadLoss*** setting)

n = Oil exponent (***Oil exp n*** setting)

$\Theta_{TO,R}$ = Top Oil rise over ambient temperature at rated load (***Top Oil Overamb*** setting)

The load current used in the calculations is the RMS value.

7.2.2.2 HOTSPOT CACULATIONS

The Hotspot temperature can only be obtained by calculation. The following equation is used to calculate the hot spot temperature every cycle:

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

where:

- Θ_H = Hotspot (winding) temperature
- Θ_{TO} = Top Oil temperature
- $\Delta\Theta_H$ = Hotspot rise above top oil temperature

The ultimate Hotspot rise over top oil is given by:

$\Delta\Theta_{H,U} = \Delta\Theta_{H,R} . K_U^{2m}$

where:

- $\Delta\Theta_{H,R}$ = winding hottest spot rise over top oil temperature at rated load. This parameter is set by the user
- K_U = the ratio of actual load to rated load
- m = winding exponent (***Winding exp m*** setting)

7.2.2.3 THERMAL STATE MEASUREMENT

ΔHot spot temperature, Top oil temperature and ambient temperature are stored in non-volatile memory. These measurements are updated every power cycle. The thermal state can be reset to zero by any of the following:

- The ***Reset Thermal*** cell under the *MEASUREMENTS 3* column on the front panel
- A remote communications interface command
- A status input state change.

The top oil temperature, hot spot temperature, ambient temperature and pre-trip time left are available as a measured value in the *MEASUREMENT 3* column.

If you need a more accurate representation of the transformer thermal state, you can use temperature monitoring devices (RTDs or CLIO), which target specific areas. For short period overloads, RTD, CLIO and overcurrent protection techniques provide better protection.

The PSL provides a signal indicating that the transformer is de-energised (***TFR De-energised***). This signal is asserted when all the circuit breakers are open. In this case, the transformer no-load losses are not considered. As a result, the top oil and hottest spot temperatures are equal to the ambient temperature when the monitored current is zero. If this signal is removed, the top oil and hottest spot temperatures are not equal to the ambient temperature even when the monitored current is zero. In this case the top oil and hottest spot temperatures will increase according to the described equations.

7.2.3 APPLICATION NOTES

7.2.3.1 RECOMMENDATIONS

Monitored Winding

You can set the monitored winding to `HV`, `LV`, `TV` or `Biased Current`. We recommend setting it to `Biased Current` to provide an overall thermal condition for the transformer.

Ambient Temperature

Ambient temperature is an important factor when determining the load capability of a transformer, because you add it to the temperature rise due to loading to determine the operating temperature. IEEE C57.91-1995 states that transformer ratings are based on an average ambient temperature of 30°C.

The ***Ambient T Source*** setting defines whether the ambient temperature should be set to an average level or measured directly using a CLI or RTD input. When measuring the ambient temperature, it should be averaged over a 24-hour period.

Top Oil Temperature

The ***Top Oil T source*** setting defines whether the Top Oil temperature is calculated or measured.

We recommend setting the rated load (***Rated Current***) to 1.0 pu.

7.2.3.2 IEEE RECOMMENDATIONS

Winding Exponent

IEEE C57.91-1995 suggests the following winding and oil exponents.

Type of Cooling	m (Winding Exponent)	n (Oil Exponent)
OA	0.8	0.8
FA	0.8	0.9
Non-directed FOA or FOW	0.8	0.9
Directed FOA or FOW	1.0	1.0

The cooling mechanisms are:

- OA (Oil/Air): The cooling system transfers heat using oil or air without using pumps or fans.
- FA (Forced Air): The cooling is aided by fans, without any pumps to circulate the oil.
- FOA (Forced Oil and Air): The cooling system uses both pumps and fans to cool the winding.
- FOW (Forced Oil and Water): The heat exchanger is water-cooled and does not have the typical radiator configuration. The cooler is normally a chamber with many tubes inside where the oil and water exchange heat energy. In non-directed flow transformers, the pumped oil flows freely through the tank. In directed flow transformers, the pumped oil is forced to flow through the windings.

The exponents are empirically derived and are required to calculate the variation of $\Delta\Theta H$ and $\Delta\Theta TO$ with load changes. The value of m has been selected for each mode of cooling to approximately account for effects of changes in resistance and viscosity with changes in load. The value of n has been selected for each mode of cooling to approximately account for effects of change in resistance with change in load.

Oil Time Constant

When setting the Hotspot and Top Oil stages take into consideration the suggested temperature limits (IEEE Std. C57.91-1995):

Suggested Limits of Temperature for Loading Above Nameplate Distribution Transformers with 65°C Rise	
Top Oil temperature	120°C
Hotspot conductor temperature	200°C

Suggested Limits of Temperature for Loading Above Nameplate Power Transformers with 65°C Rise	
Top Oil temperature	110°C
Hotspot conductor temperature	180°C

7.2.3.3 DATA PROVIDED BY TRANSFORMER MANUFACTURERS

The transformer manufacturer should provide information pertaining to the following parameters:

Rated NoLoadLoss: The ratio of load loss at rated load to no load loss.

Hot Spot Overtop: Winding hottest-spot rise over Top Oil at rated load

Top Oil overamb: Top Oil rise over ambient temperature at rated load

Winding exp m: Winding exponent

Oil exp n: Oil exponent

HotSpotRiseConst: Winding time constant at Hotspot location (this may also be estimated from the resistance cooling curve during thermal tests)

TopOilRiseConst (Oil time constant)

The following tables are examples of the thermal data provided by the transformer manufacturer:

Thermal Characteristics for a 735 MVA 300 kV +7% to -18% / 23 kV ODWF Cooled Generator Transformer	
Specification	**Value**
No load losses (core losses)	340 kW
Load losses at nominal tap	1580 kW
Load losses at maximum current tap	1963 kW
Oil time constant	2.15 hr
Oil exponent	1.0
Top Oil rise over ambient temperature at rated load	33.4 K
Winding time constant at Hotspot location	14 mins
Winding hottest spot rise over Top Oil temperature at rated load	30.2 K
Winding exponent	2.0

Note:
OD (oil directed) indicates that oil from heat exchangers (radiators) is forced through the windings. WF (Water Forced) states that the oil is externally cooled by pumped water.

Thermal Characteristics for a 600 MVA 432/23.5 kV ODWF Cooled Generator Transformer	
Specification	**Value**
No load losses (core losses)	237 kW
Load losses at nominal tap	1423 kW
Load losses at maximum current tap	1676 kW
Oil time constant	2.2 hr
Oil exponent	1.0
Top Oil rise over ambient temperature at rated load	46.6 K
Winding time constant at Hotspot location	9 mins
Winding hottest spot rise over Top Oil temperature at rated load	33.1K
Winding exponent	2.0

Thermal Characteristics for IEC 60354 Figures Based on Medium-Large Power Transformers OD Cooled	
Specification	**Value**
Oil time constant	1.5 hr
Oil exponent	1.0
Top Oil rise over ambient temperature at rated load	49 K

Thermal Characteristics for IEC 60354 Figures Based on Medium-Large Power Transformers OD Cooled	
Specification	**Value**
Winding time constant at Hotspot location	5-10 mins
Winding hottest spot rise over Top Oil temperature at rated load	29 K
Winding exponent	2.0

7.3 LOSS OF LIFE STATISTICS

Deterioration of transformer insulation is a time dependent function of temperature, moisture and oxygen content. The effects of moisture and oxygen can be minimized through designing in preservation systems for most modern transformers, therefore it is temperature that is the main reason for transformer aging. Frequent overloading will shorten the life expectancy of a transformer due to the elevated winding temperatures.

Insulation deterioration is not uniform and will be more pronounced at Hotspots within the transformer tank. Therefore any asset management system intending to model the rate of deterioration is based on simulated real-time Hotspot temperature algorithms. These models may take ambient temperature, Top Oil temperature, load current, oil pump status (pumping or not), and radiator fan status (blowing or not).

Alstom transformer protection devices provide such a loss of life monitoring facility in accordance with the thermal model defined in IEEE C57.91. The protection algorithm determines the current rate of life-loss, and uses that information to indicate the likely remaining service time. The asset owner can be alerted in advance, so that he can plan an outage in which to carry out the required maintenance such as reconditioning or rewinding.

7.3.1 LOSS OF LIFE IMPLEMENTATION

Loss of life settings are found in the *THERMAL OVERLOAD* column of the required setting group.

The device provides two single-stage definite time delay alarms based on aging acceleration factor (FAA) or loss of life (LOL).

A reset command is provided to allow you to reset the calculated parameters displayed in the *MEASUREMENTS 3* column: Loss of Life status (***LOL status***), Loss of Life aging factor (***LOL Aging Factor***), mean aging factor (***FAA,m***), rate of loss of life (***Rate of LOL***), residual life at mean aging factor (***Lres at FAA,m***), and residual life at designed (***Lres at designed***).

The loss of life model is executed once every power cycle.

7.3.1.1 LOSS OF LIFE CALCULATIONS

IEEE C57.91-1995 defines the aging acceleration factor as the rate at which transformer insulation aging for a given maximum Hotspot temperature is accelerated compared with the aging rate at a reference maximum Hotspot temperature. For transformers with average winding temperature rise of 65°C, the reference maximum Hotspot temperature is 110°C. For transformers with average winding temperature rise of 55°C, the reference maximum Hotspot temperature is 95°C. For maximum Hotspot temperatures in excess of the reference maximum Hotspot temperature, the aging acceleration factor is greater than 1. For maximum Hotspot temperatures lower than the reference maximum Hotspot temperature, the aging acceleration factor is less than 1.

The model used for loss of life statistics is given by the equations for LOL and FAA. LOL is calculated every hour according to the following formula:

$$LOL = L(\Theta_{H,r}) - L_{res}(\Theta_{H,r})$$

where:

- $L(\Theta_{H,r})$ = life hours at reference winding hottest-spot temperature (***Life Hours at HS*** setting)
- $L_{res}(\Theta_{H,r})$ = residual life hours at reference winding hottest-spot temperature

The aging acceleration factor FAA is calculated once every cycle as follows:

$$F_{AA} = \frac{L\left(\Theta_{H,r}\right)}{L\left(\Theta_{H}\right)} = \frac{e^{\left[A+\frac{B}{\Theta_{H,r}+273}\right]}}{e^{\left[A+\frac{B}{\Theta_{H}+273}\right]}} = e^{\left[\frac{B}{\Theta_{H,r}+273}-\frac{B}{\Theta_{H}+273}\right]}$$

If a 65°C average winding rise transformer is considered, the equation for FAA is as follows:

$$F_{AA} = e^{\left[\frac{B}{383} - \frac{B}{\Theta_H + 273}\right]}$$

If a 55°C average winding rise transformer is considered, the equation for FAA is as follows:

$$F_{AA} = e^{\left[\frac{B}{368} - \frac{B}{\Theta_H + 273}\right]}$$

where:

- $L(\Theta_H)$ = life hours at winding hottest-spot temperature
- $\Theta_{H,r}$ = hottest-spot temperature at rated load
- B = constant B from life expectancy curve. This parameter is set by the user. IEEE Std. C57.91-1995 recommends a B value of 15000.

The residual life hours at reference hottest-spot temperature is updated every hour as follows:

$$L_{res}(\Theta_{H,r}) = L_{res,p}(\Theta_{H,r}) - \frac{\sum_{i=1}^{3600} F_{AA,i}(\Theta_H)}{3600}$$

where:

- $L_{res,p}(\Theta_{H,r})$ = residual life hours at reference temperature one hour ago
- $F_{AA,i}(\Theta_H)$ = mean aging acceleration factor, as calculated above (calculated every second)

The accumulated loss of life is updated in non-volatile memory once per hour. It is possible to reset this to a new value if required; for example if the device is applied in a new location with a pre-aged resident transformer.

The rate of loss of life (ROLOL) in percentage per day is as follows. It is updated every day:

$$ROLOL = \frac{24}{L(\Theta_{H,r})} \cdot F_{AA,m}(\Theta_H) \cdot 100\%$$

The mean aging acceleration factor, $F_{AA,m}$, is as follows. It is updated every day:

$$F_{AA,m} = \frac{\sum_{n=1}^{N} F_{AAn} \cdot \Delta t_n}{\sum_{n=1}^{N} \Delta t_n} = \frac{\sum_{n=1}^{N} F_{AAn}}{N}$$

where:

- $F_{AA,n}$ is calculated every power cycle
- Δtn = 1 cycle
- $F_{AA,m}$ states the latest one-day statistics of F_{AA}. When the device is energized for the first time, $F_{AA,m}$ default value is 1.

The residual life in hours at $F_{AA,m}$ is as follows. It is updated every day:

$$L_{res}(F_{AA,m}) = \frac{L_{res}(\Theta_{H,r})}{F_{AA,m}}$$

7.3.2 APPLICATION NOTES

7.3.2.1 LOL SETTING GUIDELINES

Set the life hours at the reference maximum Hotspot temperature. According to IEEE Std. C57.91-1995, the normal insulation life at the reference temperature in hours or years must be user-defined. The following table extracted from IEEE Std. C57.91-1995 gives values of normal insulation life for a well-dried, oxygen-free 65°C average winding temperature rise insulation system at the reference temperature of 110°C.

Basis	Normal Insulation life Hours	Normal Insulation Life Years
50% retained tensile strength of insulation (former IEEE Std C57.92-1981 criterion)	65000	7.42
25% retained tensile strength of insulation	135000	15.41
200 retained degree of polymerization in insulation	150000	17.12
Interpretation of distribution transformer functional life test data (former IEEE Std. C57.91-1981)	180000	20.55

Note:
Tensile strength or degree of polymerization (D.P.) retention values were determined by sealed tube aging on well-dried insulation samples in oxygen-free oil.
Refer to I.2 in annex I of the IEEE Std. C57.91-1995 for discussion of the effect of higher values of water and oxygen and also for the discussion on the basis given above.

You should set the designed Hotspot temperature setting (***Designed HS temp***) to 110°C if the transformer is rated 65°C average winding rise. If the transformer is rated 55°C average winding rise, set it to 95°C.

As recommended by IEEE C57.91-1995, set the ***Constant B Set*** setting to 5000.

If the calculated aging acceleration factor is greater than the setting ***FAA> Set*** and the time delay ***tFAA> Set*** has elapsed, the ***FAA alarm*** DDB signal is activated.

If the calculated loss of life is greater than the setting ***LOL>1*** Set and the time delay ***tLOL> Set*** has elapsed, the ***LOL alarm*** DDB signal is activated.

7.3.2.2 EXAMPLE

Consider a new 65°C average winding rise rated transformer whose life hours figure at designed maximum Hotspot temperature is 180,000 hrs. As a result, you set the ***Life Hours at HS*** setting to `180,000`, and the ***Designed HS temp*** setting to 110.0°C. Set ***Constant B Set*** to `15,000` as recommended by IEEE. The aging acceleration factor takes into consideration the constant B and the hottest spot temperature calculated by the thermal function. For a distribution transformer, IEEE suggests 200°C as the limit for the maximum hot spot temperature. The aging acceleration factor alarm will be asserted when 70% of the 200°C has been reached. The aging acceleration factor is calculated as follows:

$$FAA = e^{\left[\frac{B}{383} - \frac{B}{hottest-spot-tempt+273}\right]} = e^{\left[\frac{B}{383} - \frac{B}{0.7\times200+273}\right]} = 17.2$$

Therefore:

FAA>set should be set to `17.2`. ***tFAA> Set*** may be set to `10.00 min`. ***LOL>1 Set*** may be set to `115,000 hrs`, if it is considered that the transformer has 65,000 hrs left (Life Hours at HS – hours left = 180,000 – 65,000 = 115,000 hrs). ***tLOL> Set*** may be set to `10.00 min`. Finally, the ***Reset Life Hours*** setting determines the value of the LOL measurement once the ***Reset LOL*** command is executed. The default value is zero because considering a new transformer, after testing the thermal function the LOL measurement should be reset to zero.

You should perform certain tests to determine the age of an old transformer. Please obtain advice from the transformer manufacturer.

7.4 THROUGH FAULT MONITORING

Through faults are a major cause of transformer damage and failure, as they can stress the insulation and mechanical integrity of the transformer. Through-fault monitoring is usually used to tackle this problem. This mechanism monitors fault currents passing through the transformer, which may significantly exceed its rated current. The through-fault monitoring mechanism is based on an I^2t calculation.

According to IEEE C57.109-1993(R2008), mechanical effects are more significant than thermal effects for fault-current magnitudes near the design capability of the transformer. However, at fault-current magnitudes close to the overload range, mechanical effects are less important unless the frequency of fault occurrence is high. Note that mechanical effects are more important in large kVA transformers. The standard states that the maximum duration limit for the worst case of mechanical duty is 2 s.

The standard defines the following transformer categories:

Category	Single Phase (kVA)	Three-Phase (kVA)
I	5 to 500	15 to 500
II	501 to 1667	501 to 5000
III	1668 to 10000	5001 to 30000
IV	Above 10000	Above 30000

Categories I and II consider only the transformer short-circuit impedance, whereas categories III and IV consider the system short-circuit impedance at the transformer location as well as transformer short-circuit impedance. The short-circuit impedance is expressed as a percentage of the transformer rated voltage and the rated power of the transformer.

7.4.1 THROUGH FAULT MONITORING IMPLEMENTATION

Through-fault monitoring can be enabled with the ***Through Fault*** setting in the *TF MONITORING* column.

The through-fault current monitoring function monitors the fault current level, the duration of the faulty condition and the date and time for each through-fault. An I^2t calculation based on the recorded time duration and maximum current is performed for each phase.

This calculation is only performed when the current exceeds the ***TF I> Trigger*** setting and if the DDB signal ***Any Diff Start*** is NOT asserted. Cumulative stored calculations for each phase are monitored so you can schedule the transformer maintenance based on this data.

A single-stage alarm is available for through-fault monitoring. The alarm is issued if the maximum cumulative I^2t in the three phases exceeds the ***TF I2t> Alarm*** setting. A through fault event is recorded if any of the phase currents is larger than the ***TF I> Trigger*** setting. You should always set ***TF I> Trigger*** greater than the overload capability of the transformer.

7.4.2 THROUGH FAULT MONITORING LOGIC

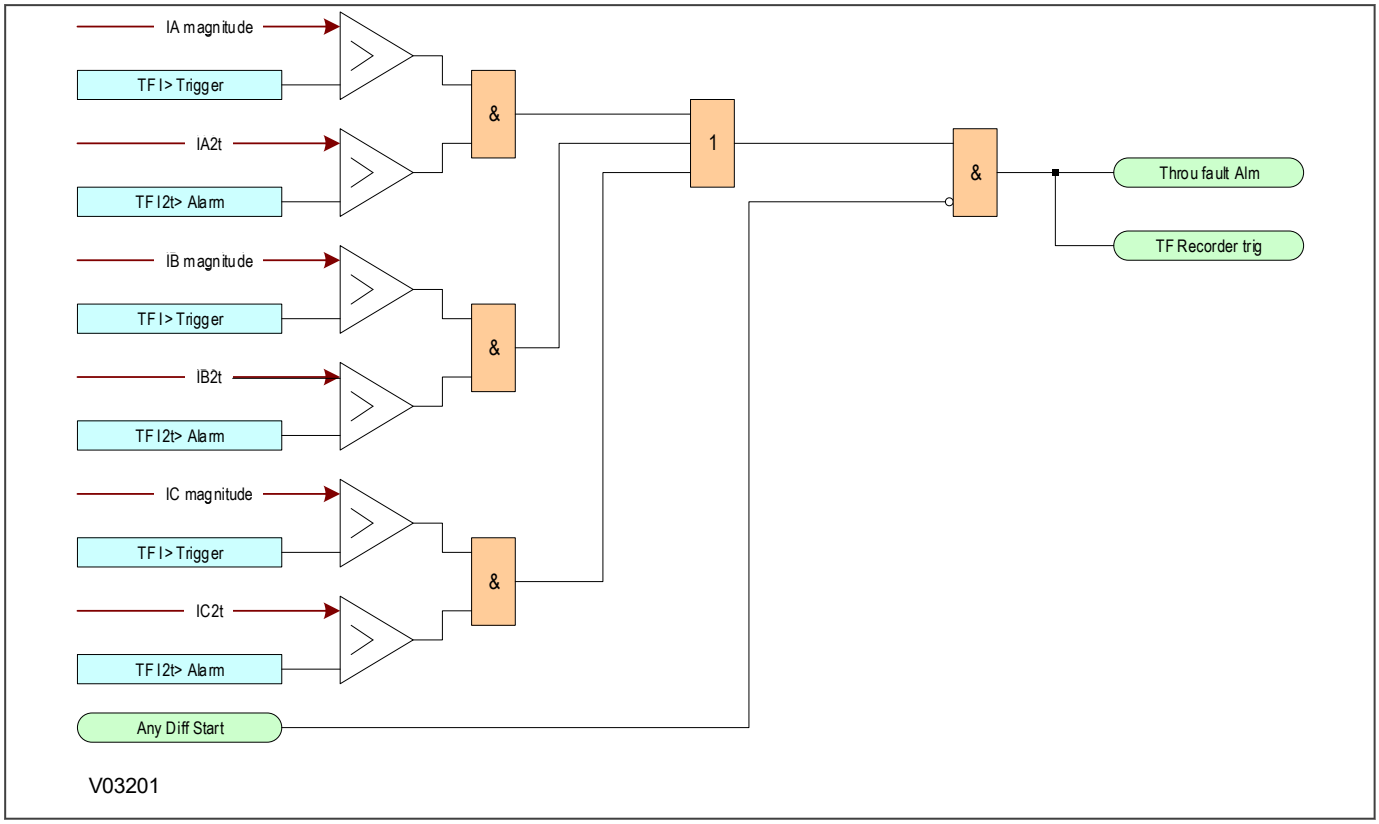


Figure 69: Through-fault alarm logic

7.4.3 APPLICATION NOTES

7.4.3.1 TFM SETTING GUIDELINES

According to IEEE Std. C57.109-1993, values of 3.5 x normal base current may result from overloads rather than faults. According to IEEE C57.91-1995, the suggested load limits depend on the type of transformer and are as follows:

- For distribution transformers: Loads above the nameplate specification with 65°C rise is 300% of rated load during short-time loading (0.5 hours or less).

For power transformers: Loads above the nameplate specification with 55°C rise is 200% of rated load.

To set ***TF I2t> Alarm*** you should consider the recommendations given in IEEE Std. C57.109-1993 for transformers built from the early 1970s onwards. For transformers built before this time, always consult the transformer manufacturer concerning the short circuit withstand capabilities.

Example

The through fault monitoring element can monitor either the HV, the LV or the TV winding. In three winding applications, you should monitor the winding through which the highest current would flow during an external fault. Fault studies are required to determine the maximum through fault current and which winding carries the most current. For example, consider the following autotransformer:

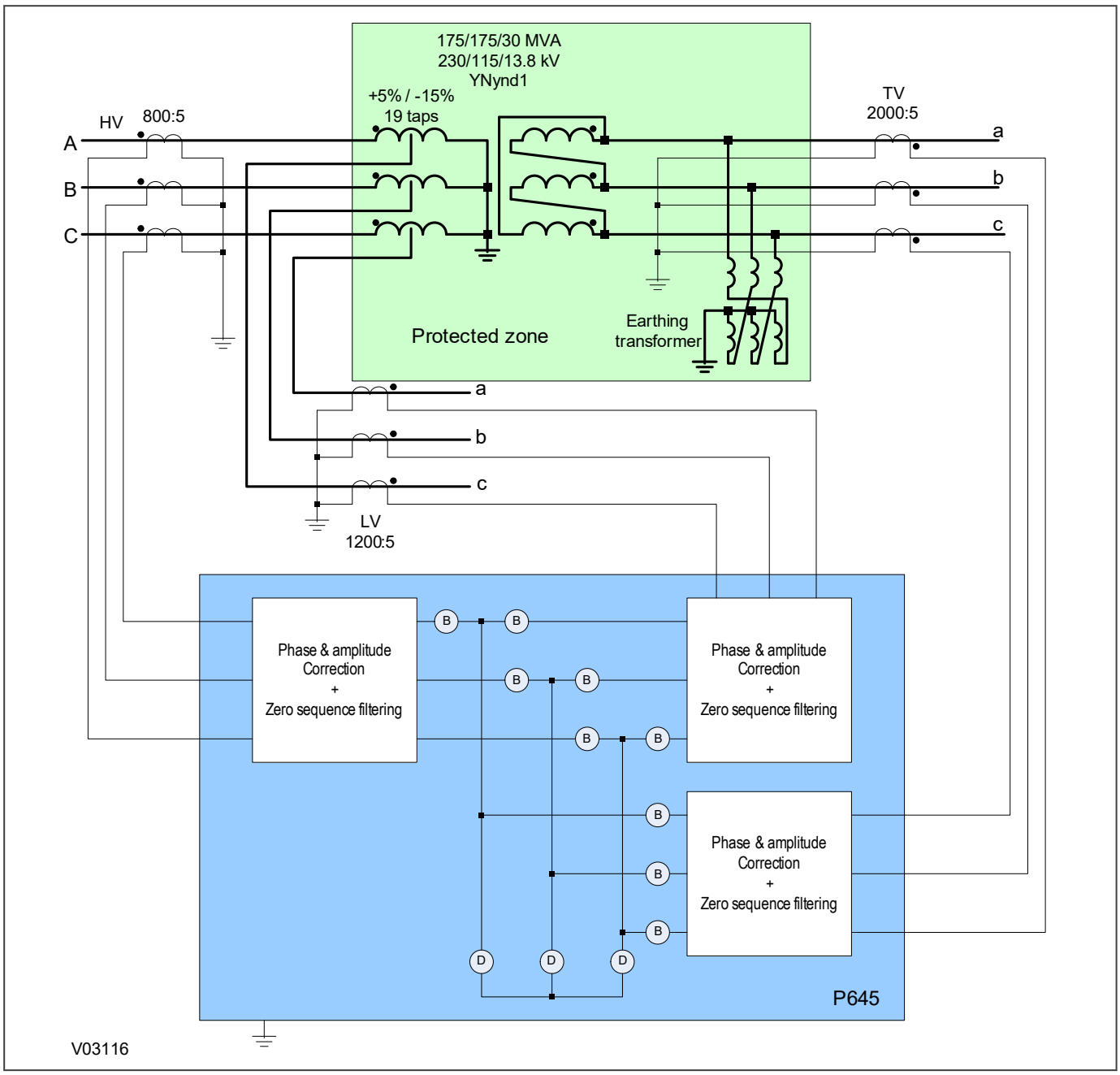


Figure 70: P645 used to protect an autotransformer with loaded delta winding

Consider the case where an equivalent source and load are connected to the 230 kV terminal and an equivalent source and load are connected to the 115 kV terminal, but only the load is connected to the 13.8 kV terminal. An external fault on the 230 kV side would be fed by the source on the 115 kV side. Therefore, the current would mainly flow from the 115 kV side to the 230 kV side. If the external fault occurs on the 115 kV side, the through-fault current would flow from the 230 kV side to the 115 kV side. If an external fault occurs on the 13.8 kV side, the through fault current would flow from the 230 kV and 115 kV sides to the 13.8 kV side. The source and transformer impedances determine the fault current level.

Set the ***TF I> Trigger*** setting above the maximum overload. According to IEEE Std. C57.109-1993, values of 3.5 or less times normal base current may result from overloads instead of faults. ***TF I> Trigger*** may be set to 3.85 pu. If the monitored current is above this level and no differential element has started, then the I2t is calculated.

To set the ***TF I2t> Alarm*** consider the maximum through fault current and the maximum time duration. The maximum through-fault current may be determined as 1/X, where X is the transformer impedance. This

approximation is valid when the source is strong, so that its impedance is small compared with the transformer impedance. If the transformer has an impedance of 10%, the maximum through fault current is calculated as:

$$1/X = 1/0.1 = 10 \text{ pu}$$

7.5 RTD PROTECTION

Prolonged overloading of transformers may cause their windings to overheat, resulting in premature aging of the insulation, or in extreme cases, insulation failure. To protect against this, resistive temperature sensing devices (RTDs) can be used to measure temperatures at various locations within a transformer. RTDs work by using the resistance versus temperature characteristic of metals. When metal heats up, its resistance changes. This can be used to feed back temperature information, which can be used by protection devices for temperature monitoring, alarming, or making protection decisions.

Probes are usually placed in areas of the equipment that are susceptible to overheating or heat damage. This could protect against winding Hotspot overheating or overtemperature in the insulating oil.

Direct temperature measurement can provide more reliable thermal protection than thermal model calculations.

Note:
Do Not select RTD options if RTD board is not fitted.

7.5.1 RTD PROTECTION IMPLEMENTATION

The P64 uses PT100 RTD probes to protect against any general or localized overheating. These can measure temperatures between –40° and +300°C. At 0°C they have a resistance of 100 Ohms.

The device accepts inputs from up to ten 2-wire or 3-wire PT100 resistive temperature sensing devices (RTD). These are connected as shown:

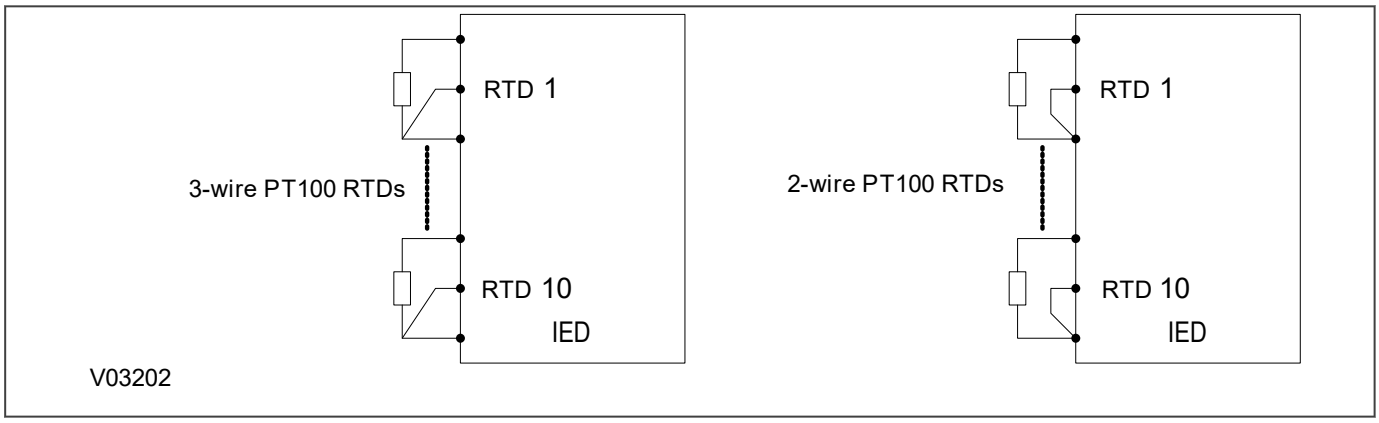


Figure 71: Connection for RTD thermal probes

You can enable or disable each RTD using the ***Select RTD*** setting in the *RTD PROTECTION* column of the relevant settings group. The setting contains a binary string of ten digits to represent the 10 RTDs in sequence from right to left. For example if you set ***Select RTD*** to 0000000111, RTD1, RTD2 and RTD3 would be enabled and the associated settings would be visible in the menu.

You set the temperature setting for the alarm stage for each RTD in the ***RTD Alarm Set*** cells and the alarm stage time delay in the ***RTD Alarm Dly*** cells.

Likewise, you set the trip stage for each RTD in the ***RTD Trip Set*** cells and the trip stage time delay in the ***RTD Trip Dly*** cells.

Should the measured resistance of an RTD be outside of the permitted range, an RTD failure alarm is raised, indicating an open or short circuit RTD input. These conditions are signalled by the DDB signals ***RTD Open Cct***, ***RTD Short Cct*** and ***RTD Data Error***. These DDB statuses are also shown in the *MEASUREMENTS 3* column.

DDB signals are also available to indicate the alarm and trip of the each and any RTD. You can set the monitor bit cells in the *COMMISSION TESTS* column to view the statuses of these signals.

7.5.2 RTD LOGIC

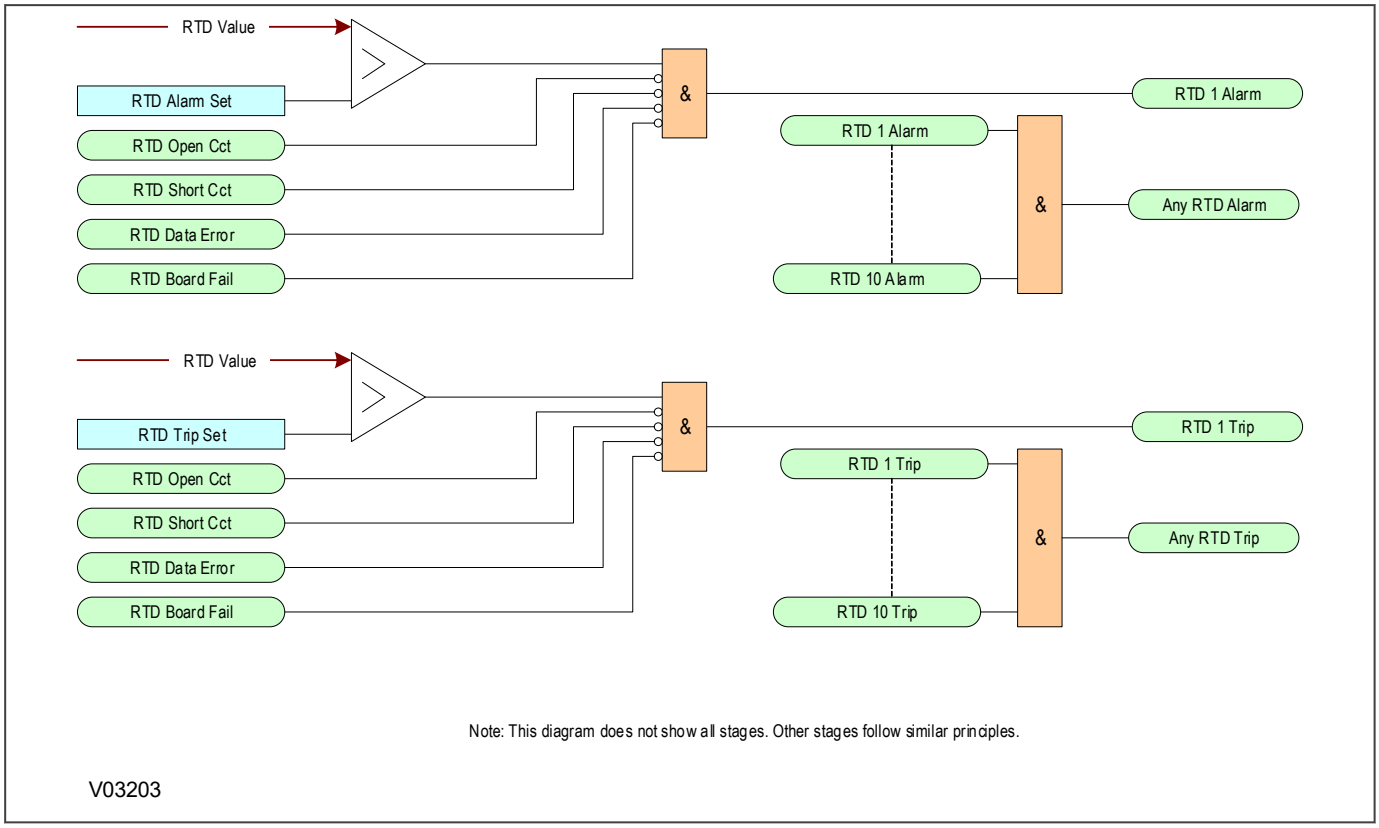


Figure 72: RTD logic

7.5.3 APPLICATION NOTES

7.5.3.1 SETTING GUIDELINES FOR RTD PROTECTION

The following table shows typical operating temperatures for protected plant. These are for guidance only. You must obtain the actual figures from the equipment manufacturers:

Parameter	Typical Service Temperature	Short Term Overloading at Full Load
Bearing temperature generators	60° - 80°C, depending on the type of bearing.	60 - 80°C+
Top oil temperature of transformers	80°C (50 - 60°C above ambient).	A temperature gradient from winding temperature is usually assumed, so that top oil RTDs can provide winding protection
Winding hot spot temperature	98°C for normal aging of insulation.	140°C+ during emergencies

7.6 CLIO PROTECTION

To help with monitoring the condition of a power systems, various transducers such as vibration monitors, tachometers, voltage, current and pressure transducers can be used to extract useful metrics from the system. Such transducers work by converting the measured data into currents, which can then be fed into instrumentation device such as meters or IEDs. This mechanism is called CLIO protection. CLIO stands for Current Loop Input Output.

Transducers have current ranges associated with the full scale of what they are measuring. Typically these ranges are 0-1 mA, 0-10 mA, 0-20 mA, or 4-20 mA.

Note:
Do Not select CLIO options if CLIO board is not fitted.

7.6.1 CURRENT LOOP INPUT IMPLEMENTATION

Four analog current loop inputs are provided for transducers with ranges of 0 – 1 mA, 0 – 10 mA, 0 – 20 mA, or 4 – 20 mA. Each input can be configured to accept any one of these ranges. Associated with each input are two protection stages; one for alarming and the other for tripping. Each stage can be individually enabled or disabled and each stage has a definite time delay setting.

Each current loop input may beset to alarm for an 'over' condition or an 'under' condition. You do this with the setting ***CLI Alarm Fn*** and selecting `under` or `over` as appropriate. Likewise, each CL input may be also set to trip for an 'over' condition or an 'under' condition. You do this with the setting ***CLI Trip Fn*** and selecting `under` or `over` as appropriate. The sample interval is nominally 50 ms per input.

The relationship between the transducer measuring range and the current input range is linear. The maximum and minimum settings correspond to the limits of the current input range. This relationship is shown below. The diagram also shows the relationship between the measured current and the analog to digital conversion (ADC) count. The hardware design allows for over-ranging, with the maximum ADC count corresponding to 1.0836 mA for the 0 - 1 mA range, and 22.7556 mA for the 0 - 10 mA, 0 - 20 mA and 4 - 20 mA ranges. The device will therefore continue to measure and display values beyond the Maximum setting, within its numbering capability.

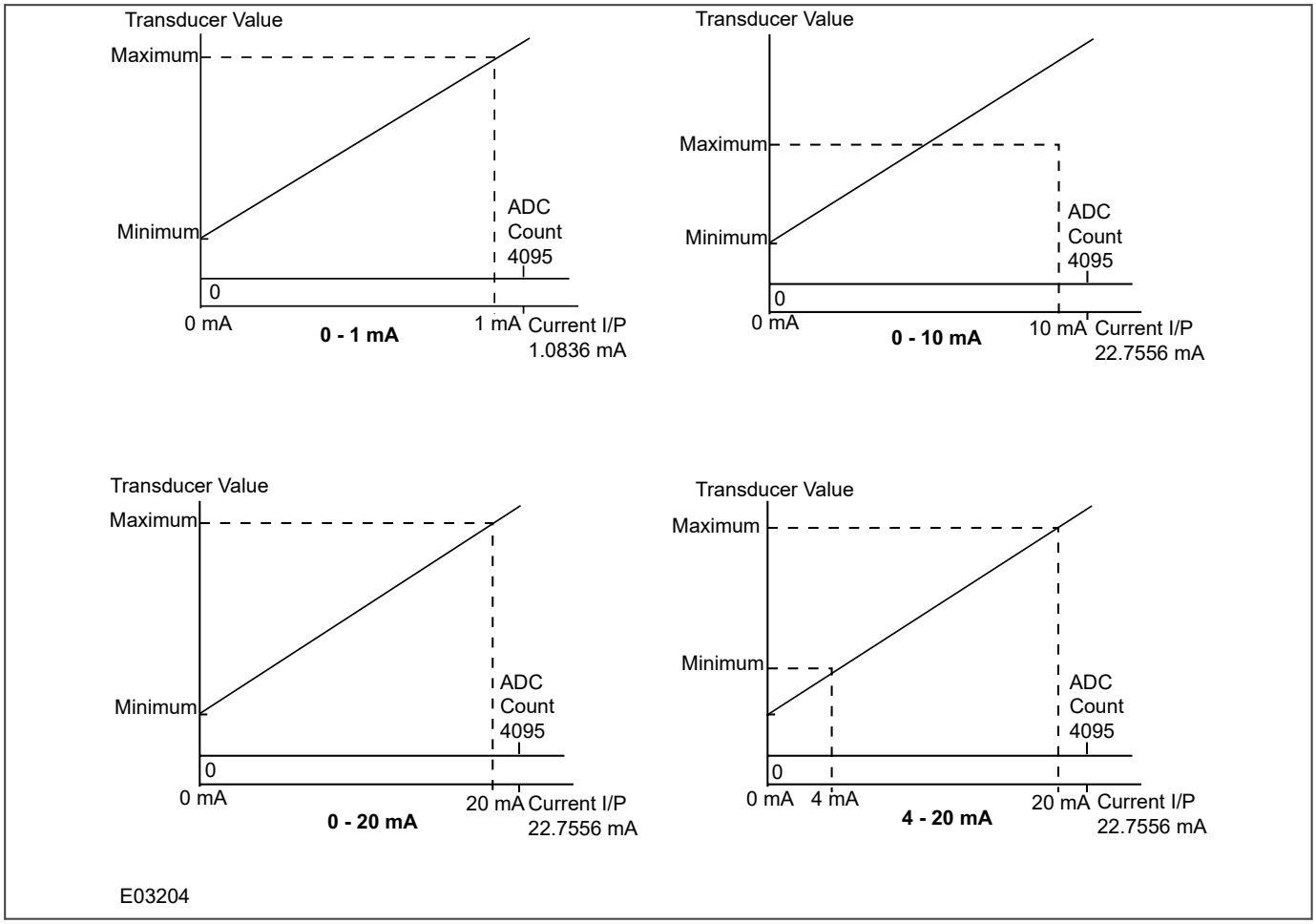


Figure 73: Current loop input ranges

Note:
If the Maximum is set less than the Minimum, the slopes of the graphs will be negative.

Power-on diagnostics and continuous self-checking of the current loop inputs are integrated into the hardware. When a failure is detected, the protection associated with all the current loop inputs is disabled and a single alarm DDB signal (***CL Card I/P Fail***) is set and an alarm is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

For the 4 – 20 mA input range, a current level below 4 mA indicates that there is a fault with the transducer or the wiring. An instantaneous undercurrent alarm element is available, with a setting range from 0 to 4 mA. This element controls a DDB output signal for each CL input (***CL(n)I< Fail Alm***), where (n) is the number of the CL input. You can then map this to a user defined alarm if required.

Hysteresis is implemented for each protection element. For 'Over' protection, the drop-off/pick-up ratio is 95%, for 'Under' protection, the ratio is 105%.

A timer block input is available for each current loop input stage. This will reset the CL input timers of the relevant stage if energized. If a current loop input is blocked, the protection and alarm timer stages and the 4 – 20 mA undercurrent alarm associated with that input are blocked. The blocking signals may be useful for blocking the current loop inputs when the CB is open for example.

DDB signals are available for each current loop input to indicate the start of alarm and trip stages. These are ***CLI(n) Alarm Start***, and ***CLI(n) Trip Start***, ***CLI(n) Alarm*** and ***CLI(n) Trip***, where (n) is the number of the current loop input. The ***Monitor Bit*** cells of the *COMMISSIONTESTS* column can be configured to show the state of the DDB signals.

The current loop input starts are mapped internally to the ***Any Start*** DDB signal.

7.6.2 CURRENT LOOP INPUT LOGIC

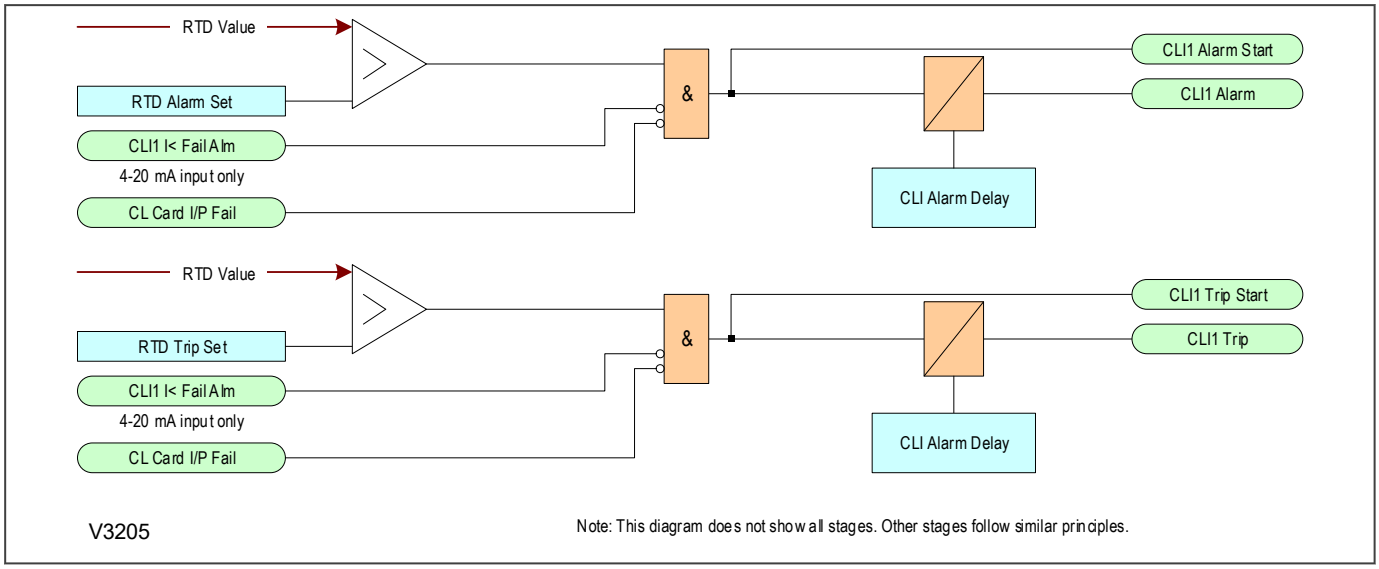


Figure 74: Current Loop Input logic

7.6.3 CLO IMPLEMENTATION

Four analog current outputs are provided with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA, which can alleviate the need for separate transducers. These may be used to feed moving coil ammeters for measuring analog quantities, or to feed into a SCADA using an existing analog remote terminal unit (RTU).

The current loop output conversion task runs every 50 ms and the refresh interval for the output measurements is nominally 50 ms.

You can set the measuring range for each analog output. The range limits are defined by the ***CLO Minimum*** and ***CLO Maximum*** settings in the *CLIO PROTECTION* column for each CL output. This allows you to zoom in and monitor a restricted range of the measurements with the desired resolution. You can set the voltage and current quantities to either `primary` or `secondary` quantities with the ***CLO Set Values*** setting.

The output current of each analog output is linearly scaled to its range limits by the Maximum and Minimum settings, as shown below:

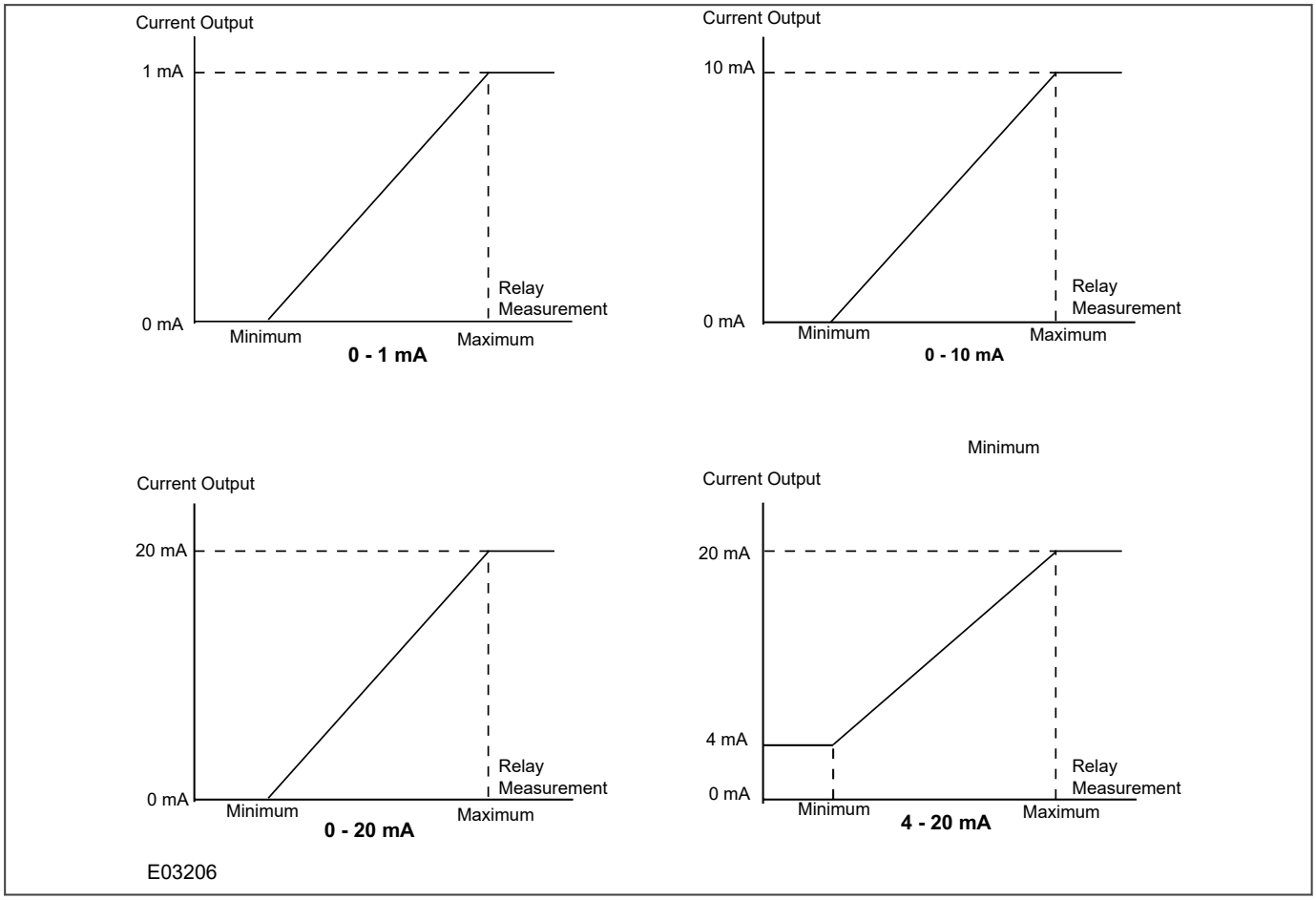


Figure 75: Current Loop Output ranges

Note:
If the Maximum is set less than the Minimum, the slopes of the graphs will be negative.

The transducers inside the device are of the current output type. This means that the correct value of output is always maintained over the load range specified. The range of load resistance varies a great deal, depending on the design and the value of output current. Transducers with a full-scale output of 10 mA will normally feed any load up to a value of 1000 ohms (compliance voltage 10V). This equates to an approximate cable length of 15 km. We recommend using a screened cable, earthed at one end. This helps reduce interference on the output current signal. The table below shows typical cable impedances per kilometer for common cables. The compliance voltage dictates the maximum load that a transducer output can feed. Therefore, the 20 mA output will be restricted to a maximum load of 500 ohms.

Cable	1/0.6 mm	1/0.85 mm	1/1.38 mm
CSA (mm2)	0.28	0.57	1.50
R (ohms/km)	65.52	32.65	12.38

You can connect the receiving equipment at any point in the output loop and install additional equipment later. You do not need to adjust the transducer output, providing the compliance voltage is not exceeded.

Where you use the output current range for control purposes, you may wish to fit appropriately rated diodes, or Zener diodes, across the terminals of each of the units in the series loop. This will guard against the possibility of their internal circuitry becoming open circuit. In this way, a faulty unit in the loop does not cause all the indications to

disappear, because the constant current nature of the transducer output simply raises the voltage and continues to force the correct output signal around the loop.

The device provides power-on diagnostics and continuous self-checking of the current loop hardware. If a failure is detected, all the current loop output functions are disabled and an alarm signal (***CL Card O/P Fail***) is raised. A maintenance record (with an error code) is also produced, which provides additional details about the type of failure.

7.6.4 APPLICATION NOTES

7.6.4.1 CLI SETTING GUIDELINES

For each analog input, you can define the following:

- The current input range: 0 – 1 mA, 0 – 10 mA, 0 – 20 mA, 4 – 20 mA
- The analog input function (in the form of a 16-character input label)
- Analog input minimum value
- Analog input maximum value
- Alarm threshold, range within the maximum and minimum set values
- Alarm function (under or over)
- Alarm delay
- Trip threshold, range within maximum and minimum set values
- Trip function (under or over)
- Trip delay

The Maximum and Minimum settings allow you to enter the range of physical or electrical quantities measured by the transducer. These are without units, however, you can enter the transducer function and the unit of the measurement using the 16-character user-defined CL Input Label. For example, if using an input to monitor a power measuring transducer, the text could be “Active Power (MW)”.

You need to set the alarm and trip thresholds within the range of physical or electrical quantities. The device will convert the current input value into its corresponding transducer measuring value for the protection calculation.

For example if the CL input minimum is -1000 and the CL input maximum is 1000 for a 0 to 10 mA input, an input current of 10 mA is equivalent to a measurement value of 1000, 5 mA is 0, and 0 mA is -1000.

These values are available for display in the ***CLIO Input (n)*** cells in the *MEASUREMENTS 3* menu. The top line shows the CL Input Label and the bottom line shows the measurement value.

7.6.4.2 CLO SETTING GUIDELINES

The outputs can be assigned to any of the following relay measurements:

- Magnitudes of IA, IB, IC of every CT input
- Magnitudes of IA, IB, IC at HV, LV and TV sides of the transformer
- Magnitudes of IN Measured and IN Derived of every winding
- Magnitudes of I1, I2, I0 at HV, LV and TV sides of the transformer
- Magnitudes of VAB, VBC, VCA, VAN, VBN, VCN, VN Measured, VN Derived
- Magnitude of Vx
- VAN RMS, VBN RMS, VCN RMS
- Frequency
- CL Inputs 1-4
- RTD 1-10

The relationship of the output current to the value of the measured values is of vital importance and needs careful consideration. Any receiving equipment must be used within its rating but, if possible, you should apply some kind of standard.

One of the objectives is to monitor the voltage over a range of values, so you need an upper limit, for example 120%. However, this may lead to difficulties when it comes to scaling an instrument.

The same considerations apply to current transducer outputs and with added complexity to power transducers outputs, where both the voltage and current transformer ratios must be taken into account.

Some of these difficulties do not need to be considered if the transducer is only feeding, for example, a SCADA outstation. Any equipment, which can be programmed to apply a scaling factor to individual inputs can accommodate most signals. The main consideration is to ensure that the transducer is capable of providing a signal right up to the full-scale value of the input.

CHAPTER 8

RESTRICTED EARTH FAULT PROTECTION

8.1 CHAPTER OVERVIEW

The device provides extensive Restricted Earth Fault functionality. This chapter describes the operation of this function including the principles of operation, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 170
REF Protection Principles 171
Restricted Earth Fault Protection Implementation 177
Second Harmonic Blocking 183
Application Notes 184

8.2 REF PROTECTION PRINCIPLES

Winding-to-core faults in a transformer can be caused by insulation breakdown. Such faults can have very low fault currents, but they still need to be picked up. If such faults are not identified, this could result in extreme damage to very expensive equipment.

Often the associated fault currents are lower than the nominal load current. Neither overcurrent nor percentage differential protection is sufficiently sensitive in this case. We therefore require a different type of protection arrangement. Not only should the protection arrangement be sensitive, but it must create a protection zone, which is limited to each transformer winding. Restricted Earth Fault protection (REF) is the protection mechanism used to protect individual transformer winding sets.

The following figure shows a REF protection arrangement for protecting the delta side of a delta-star transformer.

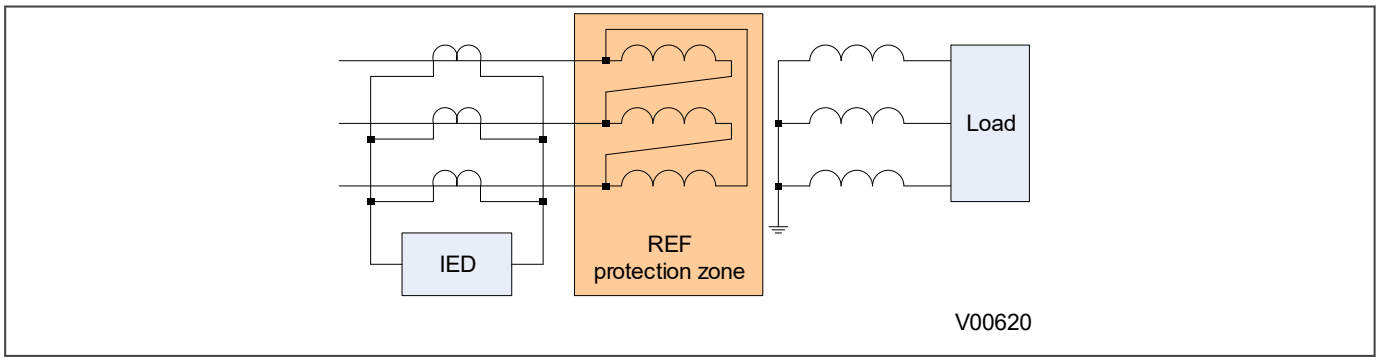


Figure 76: REF protection for delta side

The current transformers measuring the currents in each phase are connected in parallel. The currents from all three phases are summed to form a differential current, sometimes known as a spill current. Under normal operating conditions the currents of the three phases add up to zero resulting in zero spill current. A fault on the star side will also not result in a spill current, as the fault current would simply circulate in the delta windings. However, if any of the three delta windings were to develop a fault, the impedance of the faulty winding would change and that would result in a mismatch between the phase currents, resulting in a spill current. If the spill current is large enough, it will trigger a trip command.

The following figure shows a REF protection arrangement for the star side of a delta-star transformer.

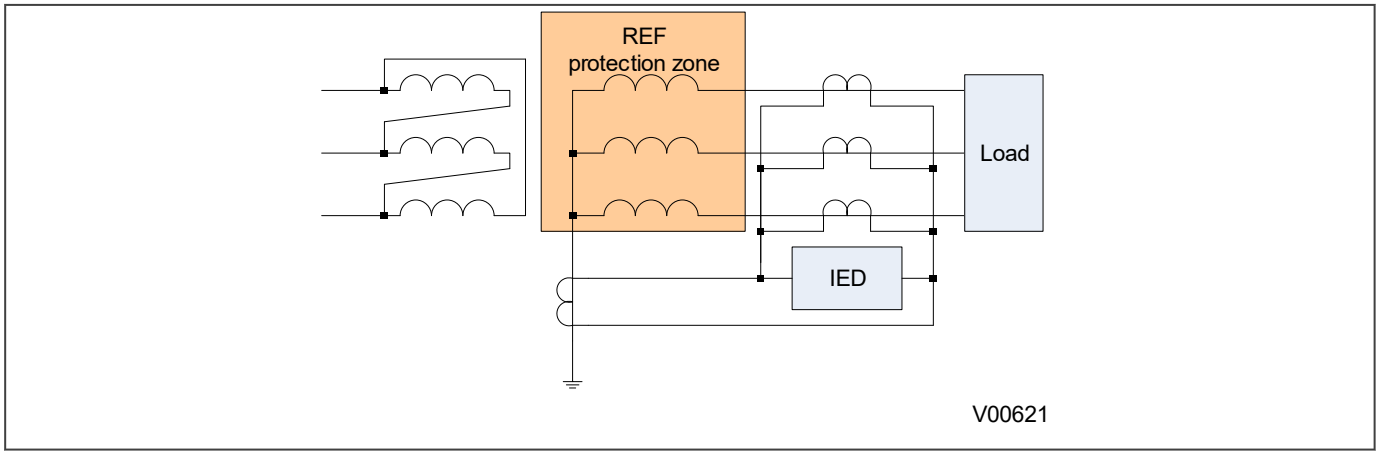


Figure 77: REF protection for star side

Here we have a similar arrangement of current transformers connected in parallel. The difference is that we need to measure the zero sequence current in the neutral line as well. An external unbalanced fault causes zero sequence current to flow through the neutral line, resulting in uneven currents in the phases, which could cause the protection to maloperate. By measuring this zero sequence current and placing it in parallel with the other three, the currents

are balanced, resulting in stable operation. Now only a fault inside the star winding can create an imbalance sufficient to cause a trip.

8.2.1 RESISTANCE-EARTHED STAR WINDINGS

Most distribution systems use resistance-earthed systems to limit the fault current. Consider the diagram below, which depicts an earth fault on the star winding of a resistance-earthed Dyn transformer (Dyn = Delta-Star with star-point neutral connection).

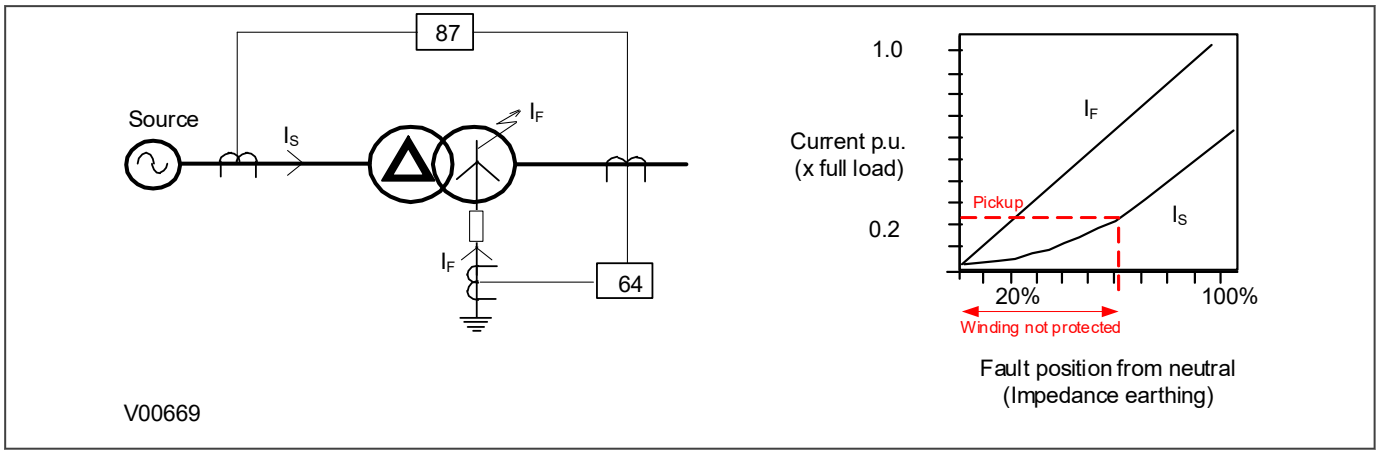


Figure 78: REF protection for resistance-earthed systems

The value of fault current (I_F) depends on two factors:

- The value of earthing resistance (which makes the fault path impedance negligible)
- The fault point voltage (which is governed by the fault location)

Because the fault current (I_F) is governed by the resistance, its value is directly proportional to the location of the fault.

A restricted earth fault element is connected to measure I_F directly. This provides very sensitive earth fault protection. The overall differential protection is less sensitive, since it only measures the HV current I_S. The value of I_S is limited by the number of faulty secondary turns in relation to the HV turns.

8.2.2 SOLIDLY-EARTHED STAR WINDINGS

Most transmission systems use solidly-earthed systems. Consider the diagram below, which depicts an earth fault on the star winding of a solidly-earthed Dyn transformer.

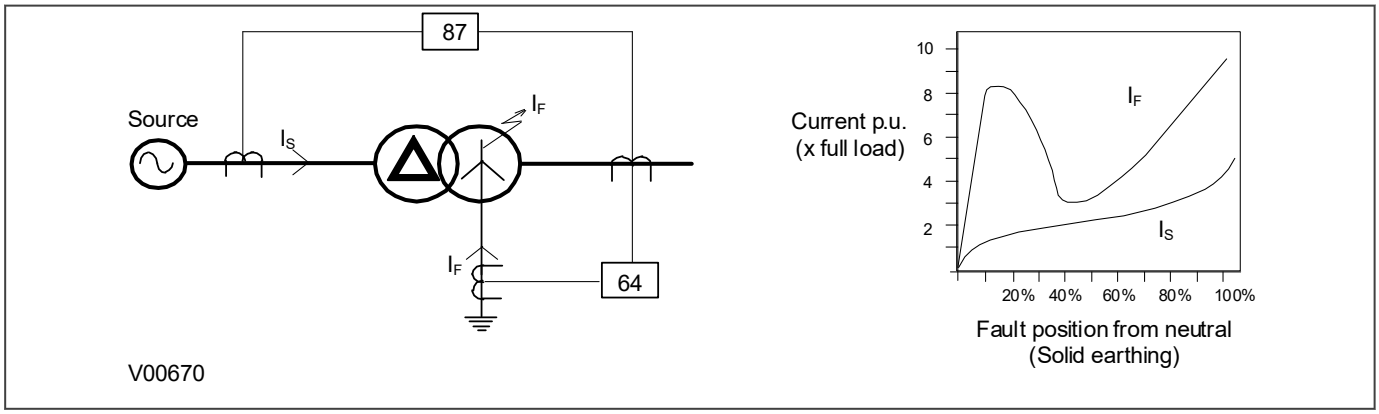


Figure 79: REF protection for solidly earthed system

In this case, the fault current I_F is dependant on:

- The leakage reactance of the winding
- The impedance in the fault path
- The fault point voltage (which is governed by the fault location)

In this case, the value of fault current (I_F) varies with the fault location in a complex manner.

A restricted earth fault element is connected to measure I_F directly. This provides very sensitive earth fault protection.

For solidly earthed systems, the operating current for the transformer differential protection is still significant for faults over most of the winding. For this reason, independent REF protection may not have been previously considered, especially where an additional device would have been needed. But with this product, it can be applied without extra cost.

8.2.3 THROUGH FAULT STABILITY

In an ideal world, the CTs either side of a differentially protected system would be identical with identical characteristics to avoid creating a differential current. However, in reality CTs can never be identical, therefore a certain amount of differential current is inevitable. As the through-fault current in the primary increases, the discrepancies introduced by imperfectly matched CTs is magnified, causing the differential current to build up. Eventually, the value of the differential current reaches the pickup current threshold, causing the protection element to trip. In such cases, the differential scheme is said to have lost stability. To specify a differential scheme's ability to restrain from tripping on external faults, we define a parameter called 'through-fault stability limit', which is the maximum through-fault current a system can handle without losing stability.

8.2.4 RESTRICTED EARTH FAULT TYPES

There are two different types of Restricted Earth Fault; Low Impedance REF (also known as Biased REF) and High Impedance REF. Each method compensates for the effect of through-fault errors in a different manner.

With Low Impedance REF, the through-fault current is measured and this is used to alter the sensitivity of the REF element accordingly by applying a bias characteristic. So the higher the through fault current, the higher the differential current must be for the device to issue a trip signal, Often a transient bias component is added to improve stability during external faults.

Low impedance protection used to be considered less secure than high impedance protection. This is no longer true as numerical IEDs apply sophisticated algorithms to match the performance of high-impedance schemes. Some advantages of using Low Impedance REF are listed below:

- There is no need for dedicated CTs. As a result CT cost is substantially reduced
- The wiring is simpler as it does not require an external resistor or Metrosil
- Common phase current inputs can be used
- It provides internal CT ratio mismatch compensation. It can match CT ratios up to 1:40 resulting flexibility in substation design and reduced cost
- Advanced algorithms make the protection secure

With High Impedance REF, there is no bias characteristic, and the trip threshold is set to a constant level. However, the High Impedance differential technique ensures that the impedance of the circuit is sufficiently high such that the differential voltage under external fault conditions is lower than the voltage needed to drive differential current through the device. This ensures stability against external fault conditions so the device will operate only for faults occurring inside the protected zone.

High Impedance REF protection responds to a voltage across the differential junction points. During external faults, even with severe saturation of some of the CTs, the voltage does not rise above certain level, because the other

CTs will provide a lower-impedance path compared with the device input impedance. The principle has been used for more than half a century. Some advantages of using High Impedance REF are listed below:

- It provides a simple proven algorithm, which is fast, robust and secure
- It is less sensitive to CT saturation

8.2.4.1 LOW IMPEDANCE REF PRINCIPLE

Low Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED is as follows:

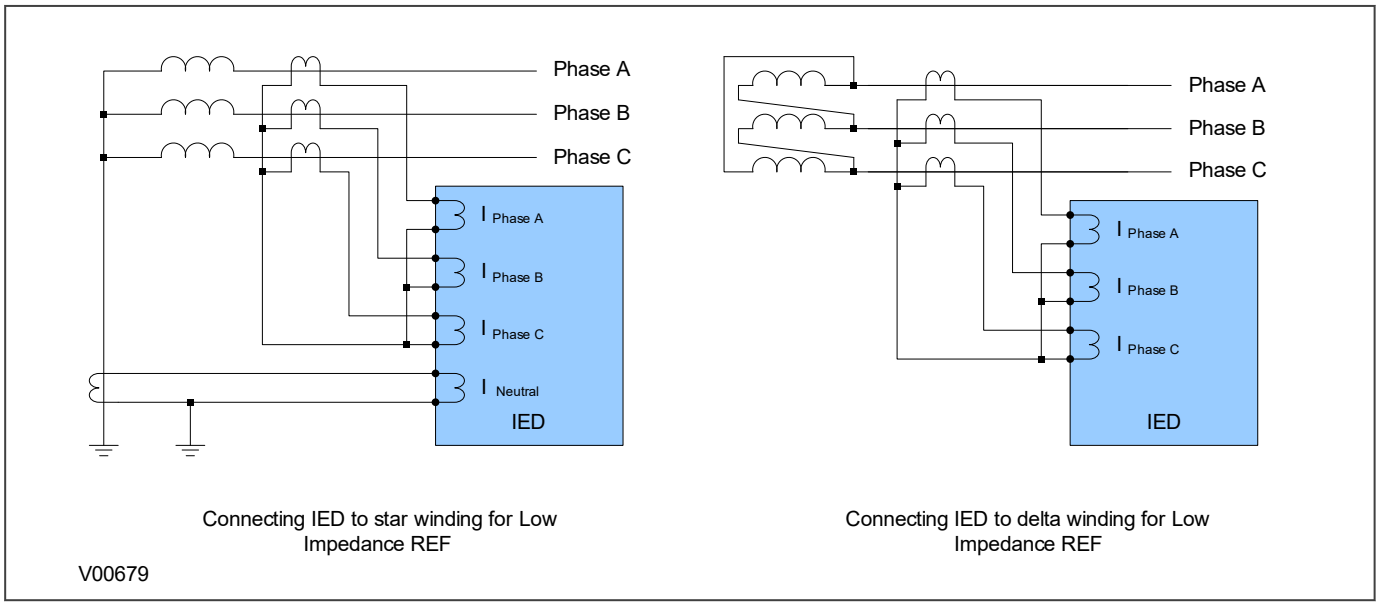


Figure 80: Low impedance REF connection

8.2.4.1.1 LOW IMPEDANCE BIAS CHARACTERISTIC

Usually, a triple slope biased characteristic is used as follows:

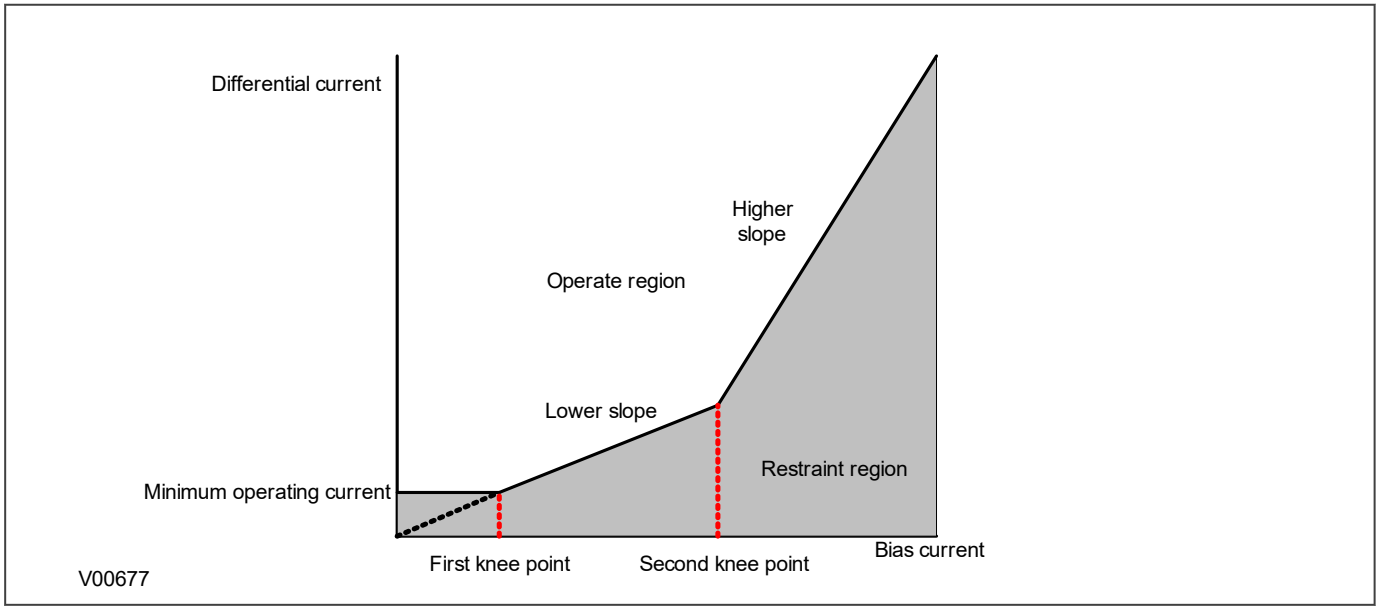


Figure 81: Three-slope REF bias characteristic

The flat area of the characteristic is the minimum differential current required to cause a trip (operate current) at low bias currents. From the first kneepoint onwards, the operate current increases linearly with bias current, as shown by the lower slope on the characteristic. This lower slope provides sensitivity for internal faults. From the second knee point onwards, the operate current further increases linearly with bias current, but at a higher rate. The second slope provides stability under through fault conditions.

Note:
In Restricted Earth Fault applications, Bias Current Compensation is also known as Low Impedance REF.

8.2.4.2 HIGH IMPEDANCE REF PRINCIPLE

This scheme is very sensitive and can protect against low levels of fault current, typical of winding faults.

High Impedance REF protection is based on the differential principle. It works on the circulating current principle as shown in the following diagram.

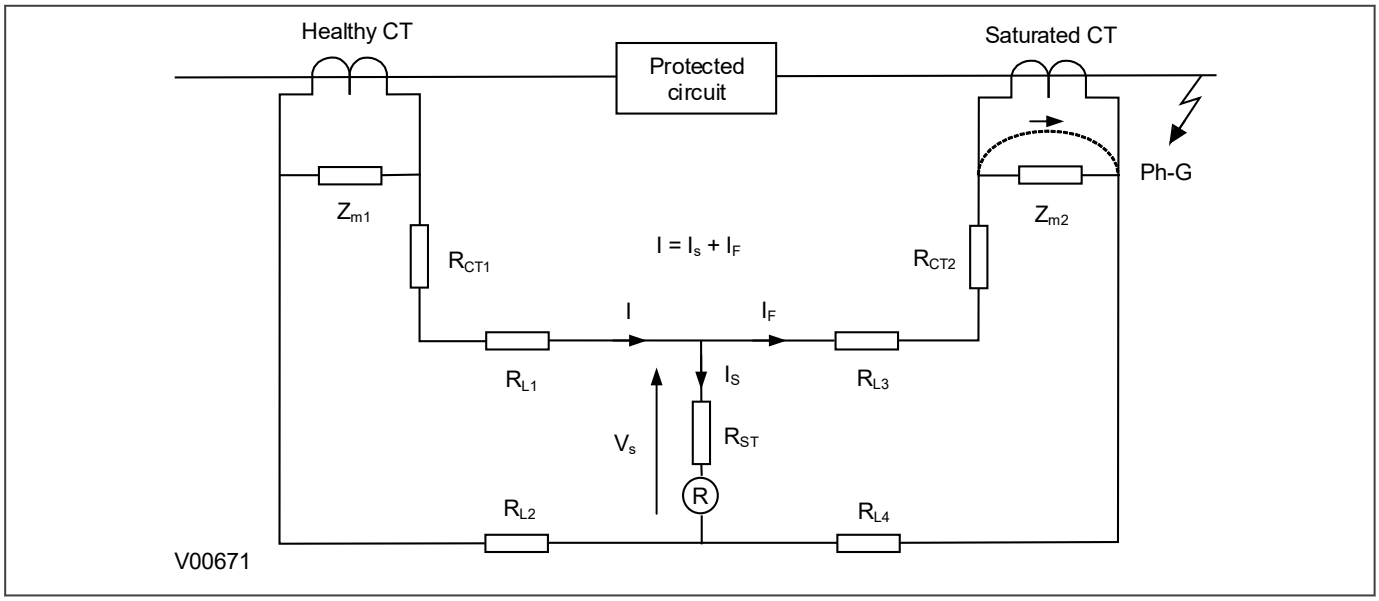


Figure 82: High impedance REF principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in imbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the device will be less than the setting, therefore maintaining stability during external faults.

Voltage across REF element $V_s = I_F (R_{CT2} + R_{L3} + R_{L4})$

Stabilising resistor $R_{ST} = V_s/I_s - R_R$

where:

- I_F = maximum secondary through fault current
- R_R = device burden
- R_{CT} = CT secondary winding resistance
- R_{L2} and R_{L3} = Resistances of leads from the device to the current transformer
- R_{ST} = Stabilising resistor

High Impedance REF can be used for either delta windings or star windings in both solidly grounded and resistance grounded systems. The connection to a modern IED are as follows:

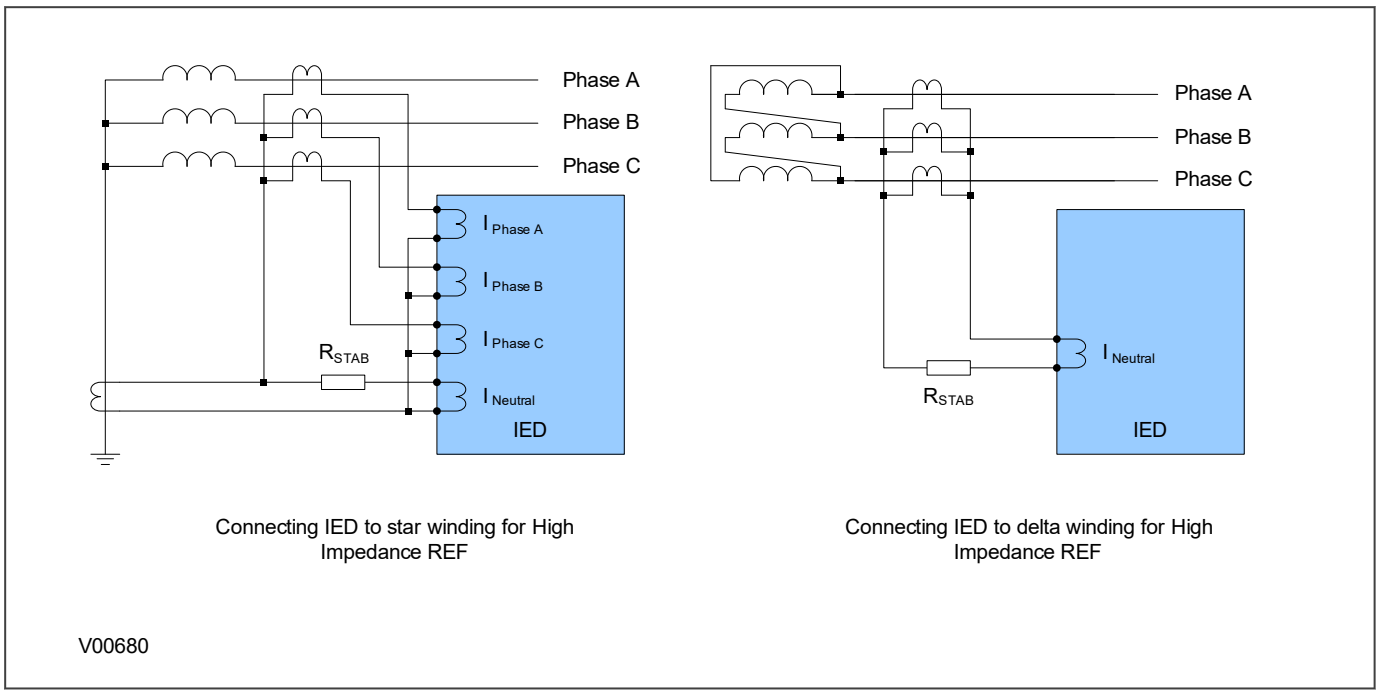


Figure 83: High impedance REF connection

8.3 RESTRICTED EARTH FAULT PROTECTION IMPLEMENTATION

8.3.1 ENABLING REF PROTECTION

A REF element is available for each of the windings (HV, LV, and if applicable, TV) as well as one for Autotransformers. For each of these windings you can disable REF protection or set it to `Low Impedance` or `High Impedance` using the settings ***REF HV Status, REF LV Status, REF TV Status*** and ***REF Auto Status*** in the *REF PROTECTION* column.

Low impedance REF is blocked if:

- Current Transformer Supervision operates
- Stub Bus protection is activated (on a per-winding basis)
- Neutral supervision element is not activated (on a per-winding basis) if Enabled

High impedance REF is not blocked by Current Transformer Supervision or Stub Bus Protection.

8.3.2 NEUTRAL SUPERVISION

A low impedance REF element is available for each of the windings (HV, LV, and if applicable, TV) as well as one for Autotransformers. For each of these windings there is a neutral current supervision element available ***IN Superv HV/LV/TV/AT*** you can enable or disable. If the neutral current is less than the ***IN Set HV/LV/TV/AT*** setting this will block the low impedance REF element. The neutral current supervision element can be used to supervise the REF element to provide additional stability for through faults causing the phase CTs to saturate which can create differential current to the REF element.

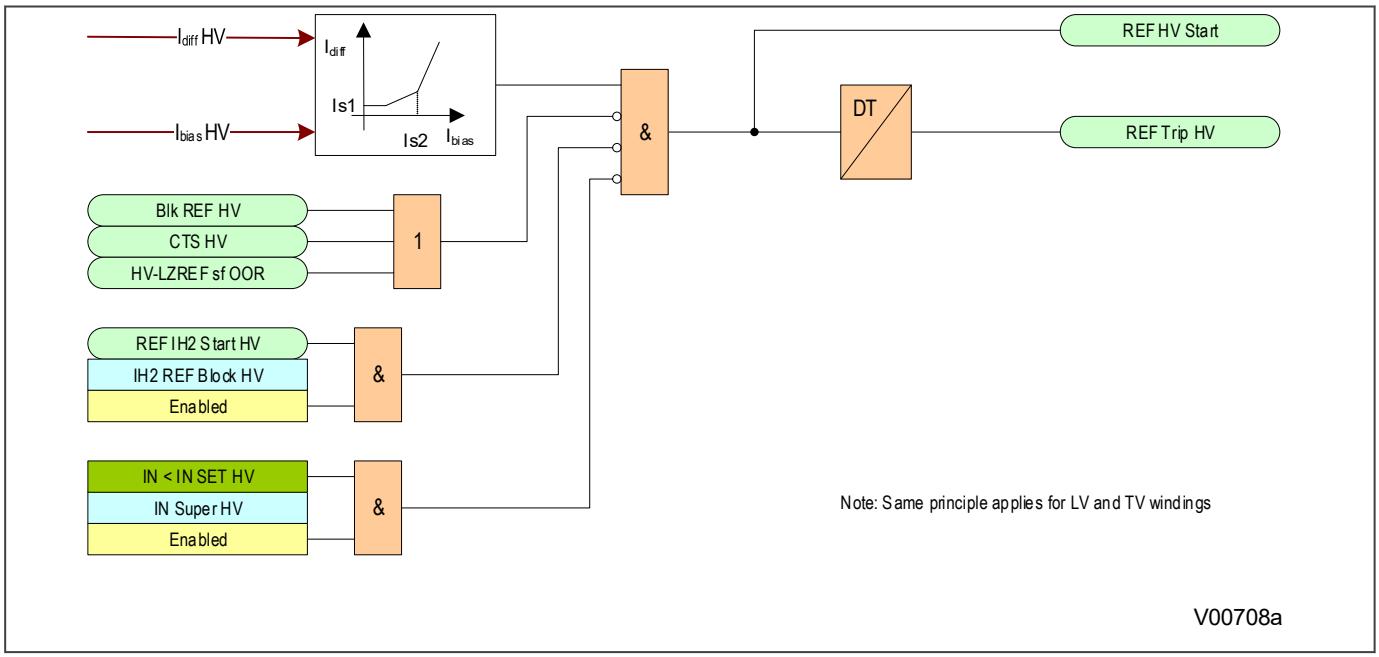


Figure 84: Low impedance restricted Earth Fault logic

8.3.3 SELECTING THE CURRENT INPUTS

The P642 has two current terminal inputs (T1 and T2), the P643 has up to three terminal current inputs (T1 to T3), and the P645 has up to five current terminal inputs (T1 to T5).

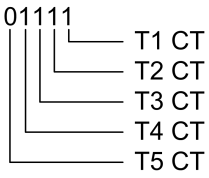
For the P642, you associate one terminal current input with the HV (High Voltage) winding and the other with the LV (Low Voltage) winding.

For the P643 and P645 you can choose to associate more than one terminal current input with particular windings. In cases where more than one terminal CT is associated with a winding, the input to the differential protection function uses the vector sum of the current terminal inputs (on a phase by phase basis) as the input to the calculation for that winding.

You associate these current inputs with the system transformer windings with the settings ***HV CT Terminals***, ***LV CT Terminals*** and ***TV CT Terminals*** in the *SYSTEM CONFIG* column as follows:

Setting	P642	P643	P645
HV CT Terminals	01	001 011	00001 00011 00111 01011 01111
LV CT Terminals	10	100 110	10000 11000 11100 11010 11110
TV CT Terminals		010	00100 01100 00110 01110

Where the terminals T1 to T5 correspond to the bits in the binary string as follows (1 = in use, 0 = not in use). The bit order starts with T1 on the right-hand side. For example:



If a CT is assigned to more than one winding, then an alarm is issued (***CT Selection Alm***). When this DDB signal is asserted, the protection is also blocked.

Winding associations for the P643

You can select the REF element Phase side CT Input for each of the elements:

- For ***HV CT terminals***, select from either HV Winding (Vector sum of multiple CT Input selected in system config HV CT terminals) or T2 input
- For ***LV CT Terminals***, select from either LV Winding (Vector sum of multiple CT Input selected in system config LV CT terminals) or T2 input

Winding associations for the P645

You can select the REF element Phase side CT Input for each of the elements:

- For ***HV CT terminals***, select from either HV Winding (Vector sum of multiple CT Input selected in system config HV CT terminals) or T2, T3 and T4 inputs
- For ***LV CT Terminals***, select from either LV Winding (Vector sum of multiple CT Input selected in system config LV CT terminals) or T2, T3 and T4 inputs
- For ***TV CT Terminals***, select from either TV Winding (Vector sum of multiple CT Input selected in system config TV CT terminals) or T2 and T4 Inputs

8.3.4 LOW IMPEDANCE REF

8.3.4.1 SETTING THE BIAS CHARACTERISTIC

Low impedance REF uses a bias characteristic for increasing sensitivity and stabilising for through faults. The current required to trip the differential IED is called the Operate current. This Operate current is a function of the differential current and the bias current according to the bias characteristic.

The differential current is defined as follows:

$$I_{diff} = \left(\bar{I}_A + \bar{I}_B + \bar{I}_C\right) + K\bar{I}_N$$

The bias current is as follows:

$$I_{bias} = \frac{1}{2}\left\{\max\left[\left|I_A\right|,\left|I_B\right|,\left|I_C\right|\right] + K\left|I_N\right|\right\}$$

where:

- K = Neutral CT ratio / Line CT ratio
- K_A = Neutral CT Primary value / Line CT Primary value
- IN = current measured by the neutral CT

The allowable range for K is:

$0.05 < K < 15$ for standard CTs

$0.05 < K < 20$ for sensitive CTs

Note:
The alarm is raised and the REF element is blocked for K_A when less than 0.05 or greater than 20.

The operate current is calculated according to the following characteristic:

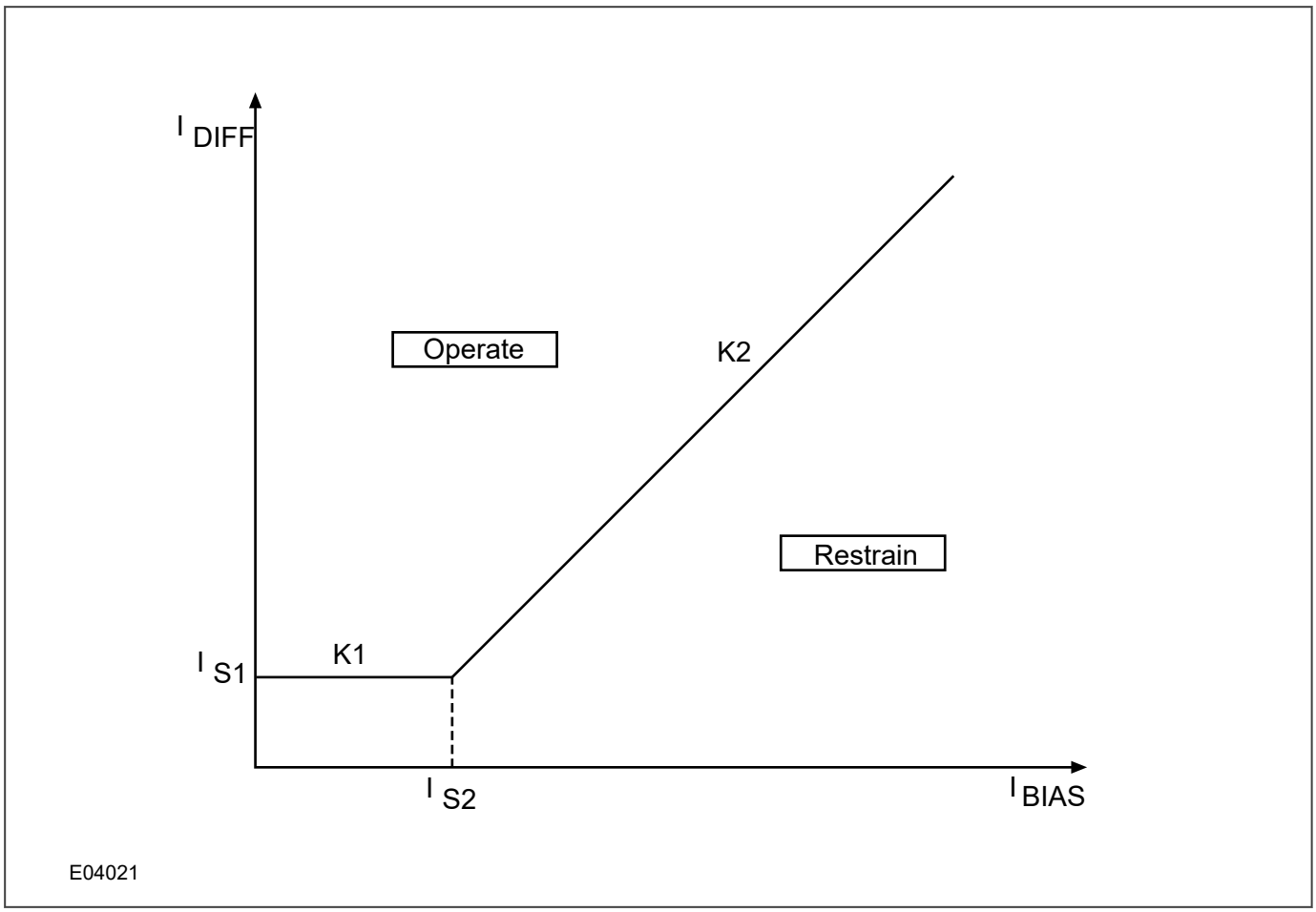


Figure 85: REF bias characteristic

The following settings are provided to define this bias characteristic:

- ***IREF> Is1***: sets the minimum trip threshold
- ***IREF> Is2***: sets the bias current kneepoint whereby the required trip current starts increasing
- ***IREF> k1***: defines the first slope (often set to 0%)
- ***IREF> k2***: defines the second slope

Note:
Is1 and Is2 are relative to the line CT, which is always the reference CT.

8.3.4.2 DELAYED BIAS

To provide further stability when external faults are being cleared, the protection checks for the highest value of bias current calculated during the previous cycle. If that value is higher than the present value, it is used to restrain the tripping decision. This is referred to as the Residual Bias. The Residual Bias technique maintains through fault stability for clearance of external faults.

8.3.4.3 TRANSIENT BIAS

If there is a sudden increase in the mean-bias measurement, an additional bias quantity is introduced in the bias calculation. Transient Bias provides stability for external faults where CT saturation might occur.

The transient bias function enhances the stability of the differential element during external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios.

No transient bias is produced under load switching conditions, or when the CT comes out of saturation.

8.3.4.4 RESTRICTED EARTH FAULT LOGIC

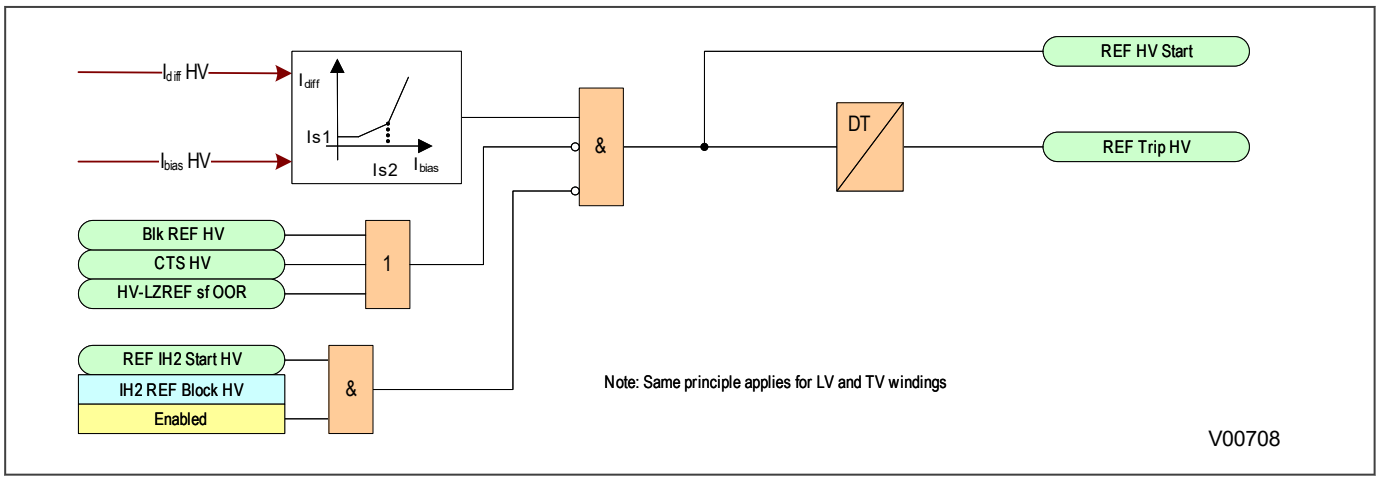


Figure 86: Low impedance restricted Earth Fault logic

8.3.5 HIGH IMPEDANCE REF

A high impedance restricted earth fault protection function is available for up to three windings. An external resistor is required to provide stability in the presence of saturated line current transformers.

TN1 CT is associated with the HV winding high impedance REF, or with the autotransformer high impedance REF. TN2 CT is associated with the LV winding high impedance REF and TN3 CT is associated with the TV winding high impedance REF.

Current transformer supervision, HV StubBus Act, LV StubBus Act or TV StubBus Act signals do not block the high impedance REF protection. You must configure logic in the PSL to block the high impedance REF when any of the above signals are asserted.

8.3.5.1 HIGH IMPEDANCE REF CALCULATION PRINCIPLES

The primary operating current (Iop) is a function of the current transformer ratio, the device operate current (***IREF>Is***), the number of current transformers in parallel with a REF element (n) and the magnetizing current of each current transformer (Ie) at the stability voltage (Vs). This relationship can be expressed in three ways:

1. The maximum current transformer magnetizing current to achieve a specific primary operating current with a particular operating current:

$$I_e < \frac{1}{n}\left(\frac{I_{op}}{CT\ ratio} - [IREF > Is] \right)$$

2. The maximum current setting to achieve a specific primary operating current with a given current transformer magnetizing current:

$$[IREF > Is] < \left(\frac{I_{op}}{CT\ ratio} - nI_e \right)$$

3. The protection primary operating current for a particular operating current with a particular level of magnetizing current:

$$I_{op} = (CT\ ratio)([IREF > Is] + nI_e)$$

To achieve the required primary operating current with the current transformers that are used, you must select a current setting for the high impedance element, as shown in item 2 above. You can calculate the value of the stabilising resistor (R_{ST}) in the following manner.

$$R_{st} = \frac{Vs}{\lceil IREF > Is \rceil} = \frac{I_F \left(R_{CT} + 2R_L \right)}{\lceil IREF > Is \rceil}$$

where:

- R_{CT} = the resistance of the CT winding
- R_L = the resistance of the lead from the CT to the IED.

Note:
The above formula assumes negligible relay burden.

We recommend a stabilizing resistor, which is continuously adjustable up to its maximum declared resistance.

8.4 SECOND HARMONIC BLOCKING

8.4.1 REF 2ND HARMONIC BLOCKING LOGIC

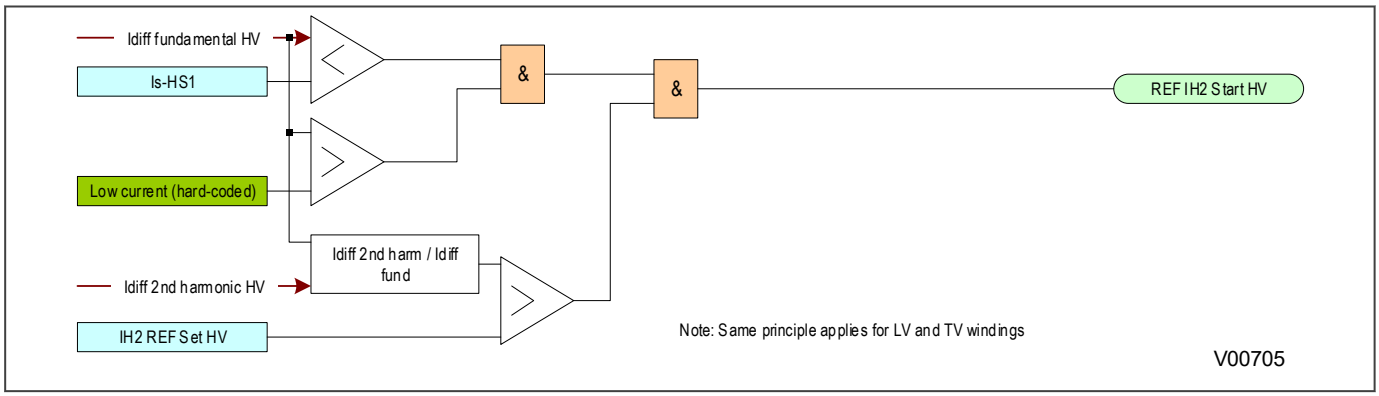


Figure 87: REF 2nd harmonic blocking logic

8.5 APPLICATION NOTES

8.5.1 STAR WINDING RESISTANCE EARTHED

Consider the following resistance earthed star winding below.

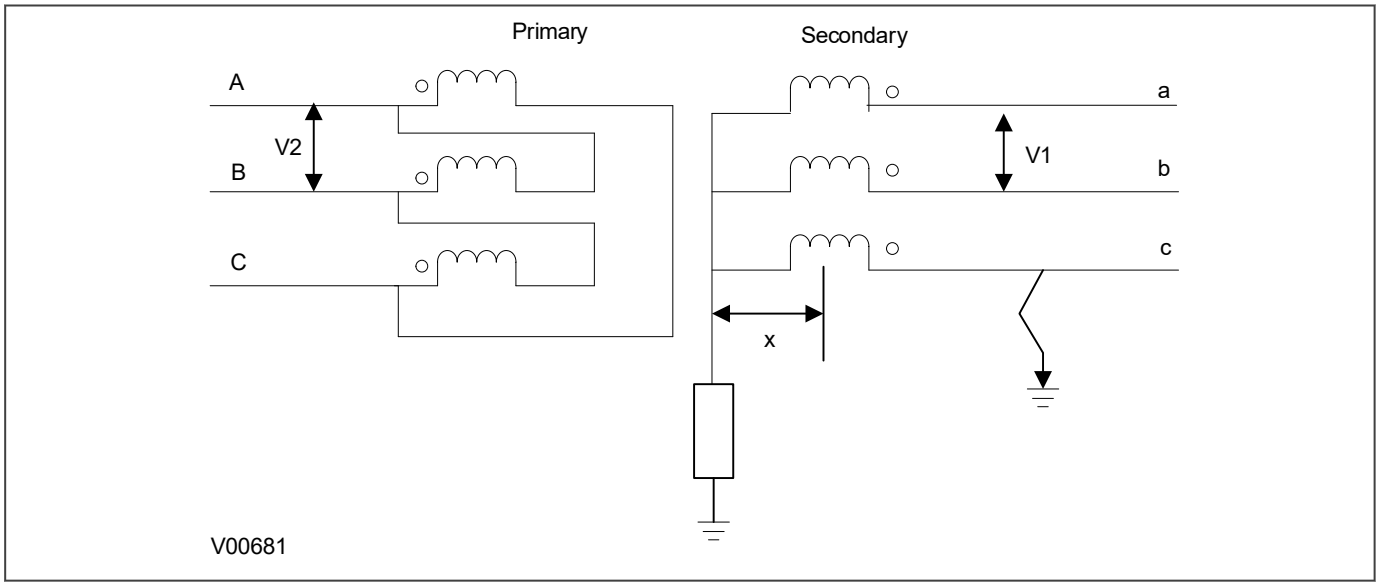


Figure 88: Star winding, resistance earthed

An earth fault on such a winding causes a current which is dependant on the value of earthing impedance. This earth fault current is proportional to the distance of the fault from the neutral point since the fault voltage is directly proportional to this distance.

The ratio of transformation between the primary winding and the short circuited turns also varies with the position of the fault. Therefore the current that flows through the transformer terminals is proportional to the square of the fraction of the winding which is short circuited.

The earthing resistor is rated to pass the full load current $I_{FLC} = V1/\sqrt{3}R$

Assuming that V1 = V2 then $T2 = \sqrt{3}T1$

For a fault at x PU distance from the neutral, the fault current $If = xV1/\sqrt{3}R$

Therefore the secondary fault current referred to the primary is $I_{primary} = x^2.I_{FLC}/\sqrt{3}$

If the fault is a single end fed fault, the primary current should be greater than 0.2 pu (Is1 default setting) for the differential protection to operate. Therefore $x^2/\sqrt{3} > 20\%$

The following diagram shows that 41% of the winding is protected by the differential element.

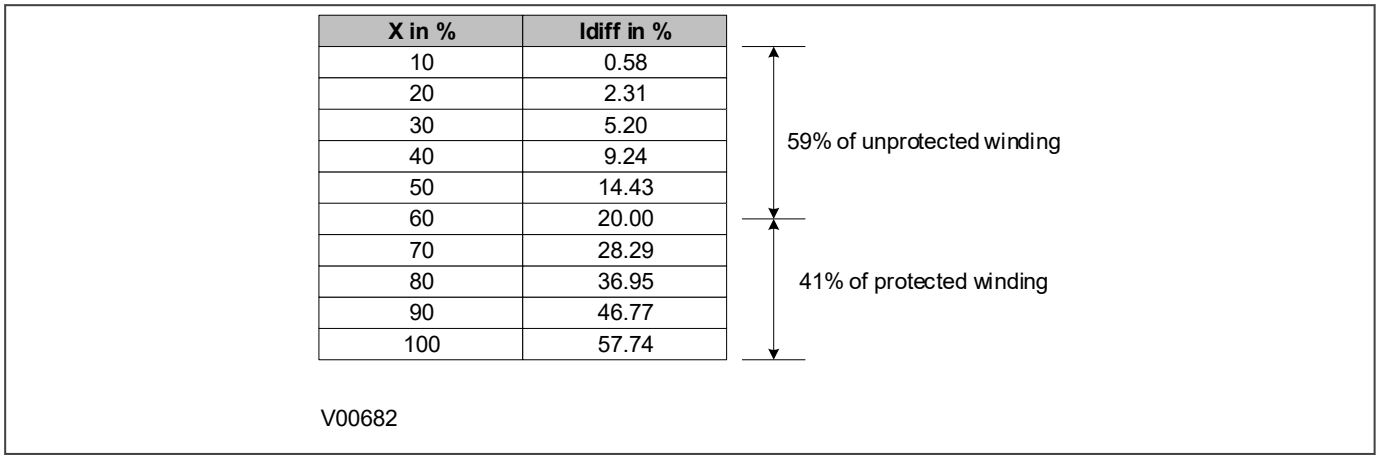


Figure 89: Percentage of winding protected

8.5.2 LOW IMPEDANCE REF PROTECTION APPLICATION

8.5.2.1 SETTING GUIDELINES FOR BIASED OPERATION

Two bias settings are provided in the REF characteristic. The K1 level of bias is applied up to through currents of Is2, which is normally set to the rated current of the transformer. K1 is normally be set to 0% to give optimum sensitivity for internal faults. However, if any CT mismatch is present under normal conditions, then K1 may be increased accordingly, to compensate. We recommend a setting of 20% in this case.

K2 bias is applied for through currents above Is2 and would typically be set to 150%.

According to ESI 48-3 1977, typical settings for the Is1 thresholds are 10-60% of the winding rated current when solidly earthed and 10-25% of the minimum earth fault current for a fault at the transformer terminals when resistance earthed.

8.5.2.2 LOW IMPEDANCE REF SCALING FACTOR

The three line CTs are connected to the three-phase CTs, and the neutral CT is connected to the neutral CT input. These currents are then used internally to derive both a bias and a differential current quantity for use by the low impedance REF protection. The advantage of this mode of connection is that the line and neutral CTs are not differentially connected, so the neutral CT can also be used to provide the measurement for the Standby Earth Fault Protection. Also, no external components such as stabilizing resistors or Metrosils are required.

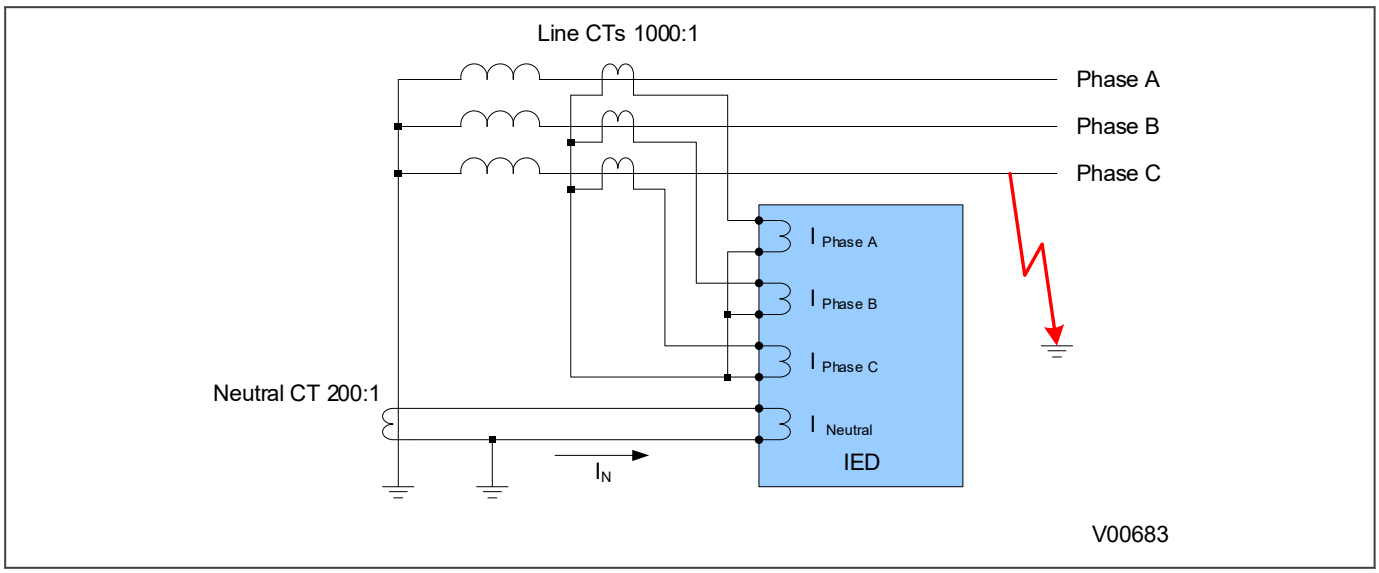


Figure 90: Low impedance REF scaling factor

Another advantage of Low Impedance REF protection is that you can use a neutral CT with a lower ratio than the line CTs in order to provide better earth fault sensitivity. In the bias calculation, the device applies a scaling factor to the neutral current. This scaling factor is as follows:

Scaling factor = K = Neutral CT ratio / Line CT ratio

This results in the following differential and bias current equations:

$$I_{diff} = \left(\bar{I}_A + \bar{I}_B + \bar{I}_C\right) + K\bar{I}_N$$

$$I_{bias} = \frac{1}{2}\left\{\max\left[|I_A|, |I_B|, |I_C|\right] + K|I_N|\right\}$$

8.5.2.3 PARAMETER CALCULATIONS

Consider a solidly earthed 90 MVA 132 kV transformer with a REF-protected star winding. Assume line CTS with a ratio of 400:1.

Is1 is set to 10% of the winding nominal current:

$= (0.1 \times 90 \times 10^6) / (\sqrt{3} \times 132 \times 10^3)$

= 39 Amps primary

= 39/400 = 0.0975 Amps secondary (approx 0.1 A)

Is2 is set to the rated current of the transformer:

$= 90 \times 10^6 / (\sqrt{3} \times 132 \times 10^3)$

= 390 Amps primary

= 390/400 = 0.975 Amps secondary (approx 1 A)

Set ***K1*** to 0% and ***K2*** to 150%

8.5.2.4 DUAL CB APPLICATION WITH DIFFERENT PHASE CT RATIOS

The following diagram shows the situation where low impedance REF is being used in a dual breaker (breaker-and-a-half) application where the phase CT ratios (CT_x and CT_y) are different. In this example, one phase of a conventional transformer is shown, but the explanation is also applicable to autotransformers.

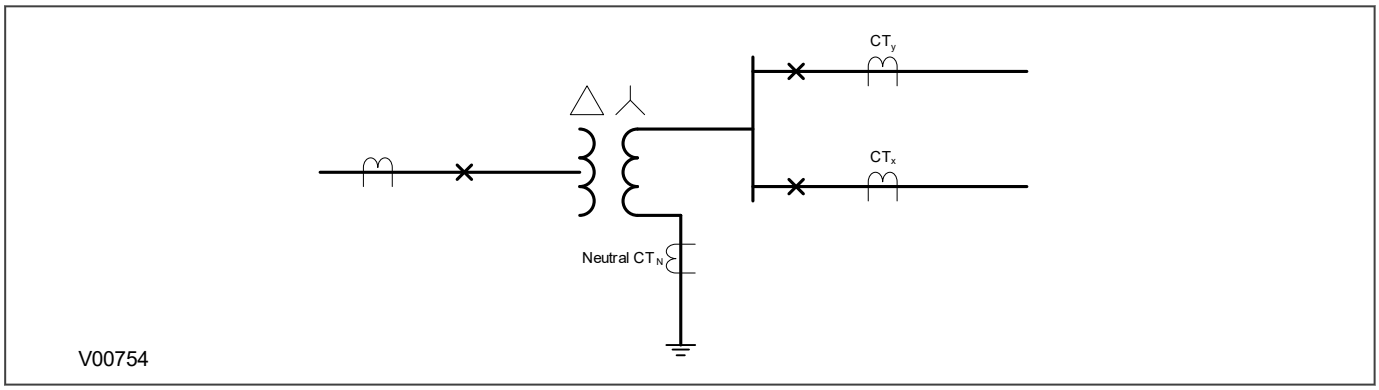


Figure 91: Low-Z REF for dual CB application with different phase CT ratios

The low impedance REF function can be used in dual breaker (breaker-and-a-half) applications. The line CT ratios can be different. In this case the low impedance REF differential and bias current formulae are calculated as follows:

$$I_{diff(REF)} = \left| \left(\overline{IA}_{CTx} + \overline{IB}_{CTx} + \overline{IC}_{CTx} + K_1 \overline{IA}_{CTy} + K_1 \overline{IB}_{CTy} + K_1 \overline{IC}_{CTy} \right) + K_2 \overline{IN} \right|$$

$$I_{bias(REF)} = \frac{1}{2} \left\{ \max \left[\left(\left| \overline{IA}_{CTx} \right| + K_1 \left| \overline{IA}_{CTy} \right| \right), \left(\left| \overline{IB}_{CTx} \right| + K_1 \left| \overline{IB}_{CTy} \right| \right), \left(\left| \overline{IC}_{CTx} \right| + K_1 \left| \overline{IC}_{CTy} \right| \right) \right] + K_2 \overline{IN} \right\}$$

where:

- CT_x and CT_y (T1, T2, T3, T4 or T5) are the current inputs associated with a particular winding (given in the settings ***HV CT Terminals***, ***LV CT Terminals*** and ***TV CT Terminals*** respectively)
- K1 = CT_y Ratio/CT_x Ratio (Scaling Factor K1)
- K2 = Neutral CT Ratio/CT_x Ratio (Scaling Factor K2)
- Reference: CT_x, which is the same as T1-CT

Note:
The above formulae are valid for autotransformers and conventional transformers when the Phase CT Ratios are different (CTx ≠ CTy) and the reference is CTx

8.5.2.5 DUAL CB APPLICATION WITH SAME PHASE CT RATIOS

The following diagram shows the situation where low impedance REF is being used in a dual breaker (breaker-and-a-half) application where the phase CT ratios are identical. In this example, one phase of an autotransformer is shown, but the explanation is also applicable to conventional transformers.

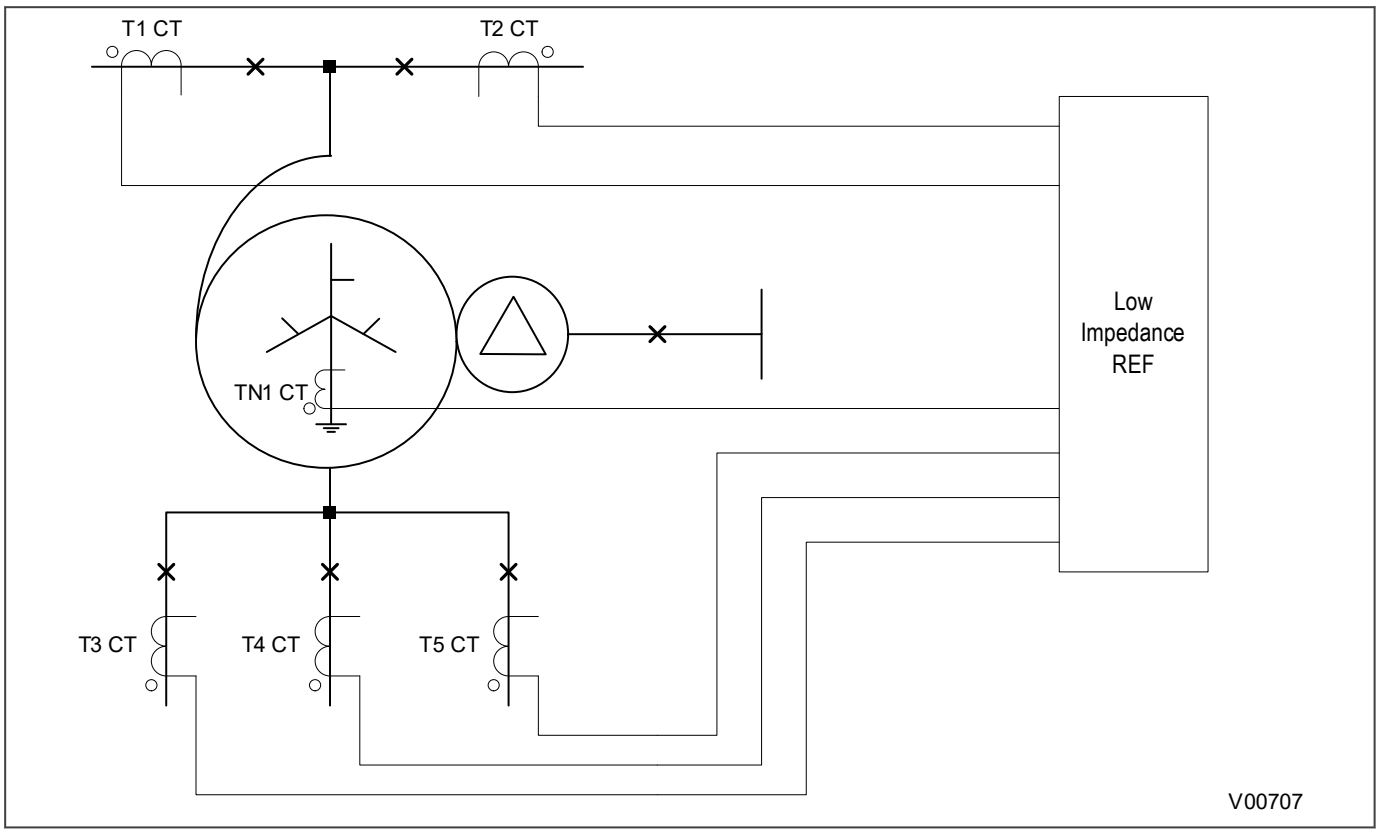


Figure 92: Low-Z REF for dual CB application with same phase CT ratios

The low impedance REF function can be used in dual breaker (breaker-and-a-half) applications. The line CT ratios may be identical. In this case the Restricted Earth Fault (REF) Low Impedance (Z) Differential and Bias current formulae are calculated as follows:

$$I_{diff\,(REF)} = \left| \sum_{n=1}^{n} \left[\left(\overline{IA}_{TxCT} + \overline{IB}_{TxCT} + \overline{IC}_{TxCT} \right) \right] + K_n \overline{I}_{\mathrm{TN1\ CT}} \right|$$

$$I_{bias(REF)} = \frac{1}{2} \left\{ \max \left[\begin{array}{l} \sum_{n=1}^{n} \left| \overline{IA}_{TxCT} \right| \\ \sum_{n=1}^{n} \left| \overline{IB}_{TxCT} \right| \\ \sum_{n=1}^{n} \left| \overline{IC}_{TxCT} \right| \end{array} \right] + K_n \left| \overline{I}_{\mathrm{TN1\ CT}} \right| \right\}$$

where:

- Tx CT = T1, T2, T3, T4 or T5.
- Kn = TN1 CT Ratio/ Tx CT Ratio
- TN1 CT Ratio = Neutral CT Ratio.
- Reference: Tx CT.

8.5.2.6 CT REQUIREMENTS - LOW IMPEDANCE REF

We strongly recommend Class X or Class 5P current transformers for this application.

The CT requirements for low impedance REF protection are generally lower than those for differential protection. As the line CTs for low impedance REF protection are the same as those used for differential protection the differential CT requirements cover both differential and low impedance REF applications.

The current transformer knee-point voltage requirements are based on the following default settings for transformer REF protection; IS1 = 27 A (primary value at 300/1 CT Ratio), IS2 = 270 A (primary value at 300/1 CT ratio), K1 = 0%, K2 = 150%.

The K dimensioning factor for the REF function is smaller than that for the transformer differential protection. Since the highest K factor must be considered, the CT requirements for transformer differential must be considered.

8.5.2.6.1 CT REQUIREMENTS - ONE BREAKER APPLICATION

To achieve through-fault stability, the K dimensioning factor must comply with the following:

System Conditions	K	Kneepoint Voltage (VK)
$2I_n < I_F \leq 64I_n$ $5 \leq X/R \leq 120$	12	$V_K \geq 12I_n(R_{CT} + 2R_L + R_r)$

where:

- V_K = kneepoint voltage
- K = CT dimensioning factor
- I_n = rated current
- R_{CT} = resistance of CT secondary winding
- R_L = Resistance of a single lead from device to current transformer
- R_r = resistance of any other protection devices sharing the current transformer

8.5.2.6.2 CT REQUIREMENTS - ONE-AND-A-HALF BREAKER APPLICATION

According to the test results, to achieve through-fault stability, the K dimensioning factor must comply with the following:

System Conditions	K	Kneepoint Voltage (VK)
$2I_n < I_F \leq 64I_n$ $5 \leq X/R \leq 20$	27	$V_K \geq 27I_n(R_{CT} + 2R_L + R_r)$

where:

- V_K = kneepoint voltage
- K = CT dimensioning factor
- I_n = rated current
- R_{CT} = resistance of CT secondary winding
- R_L = Resistance of a single lead from device to current transformer
- R_r = resistance of any other protection devices sharing the current transformer

8.5.3 HIGH IMPEDANCE REF PROTECTION APPLICATION

8.5.3.1 HIGH IMPEDANCE REF OPERATING MODES

In the examples below, the respective Line CTS and measurement CTs must have the same CT ratios and similar magnetising characteristics.

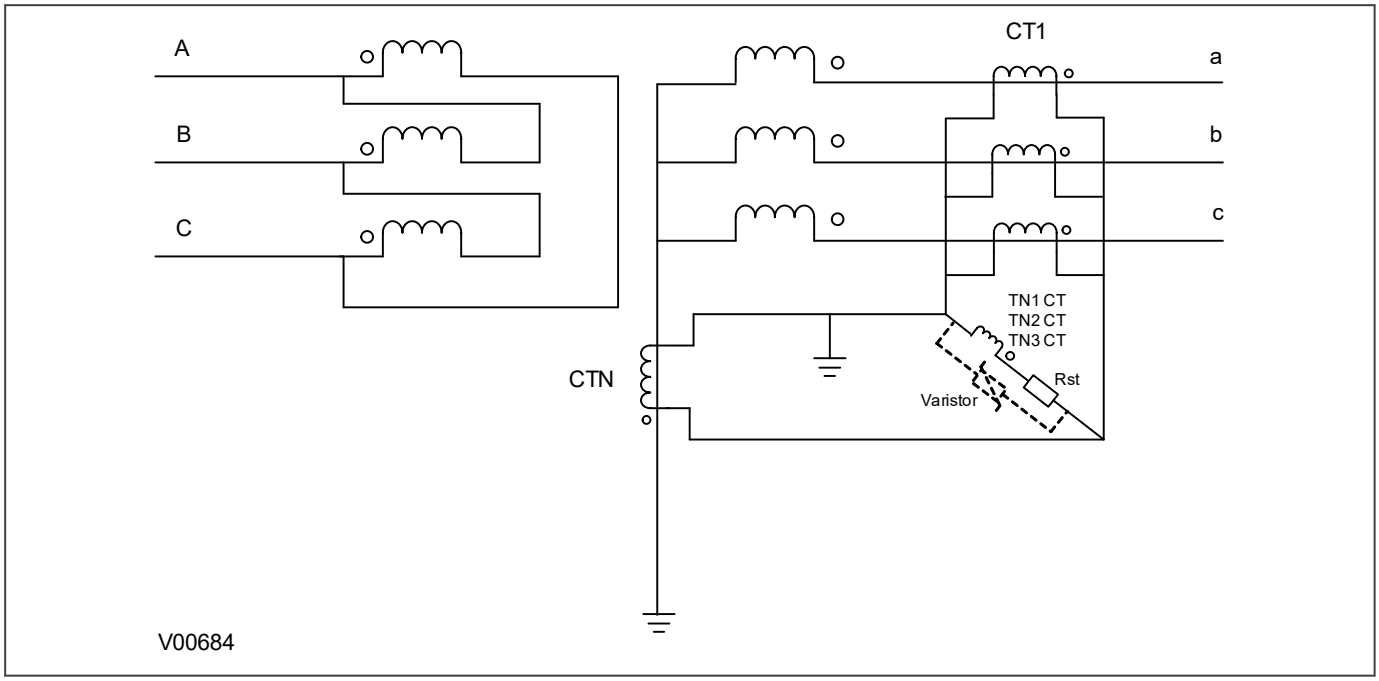


Figure 93: Hi-Z REF protection for a grounded star winding

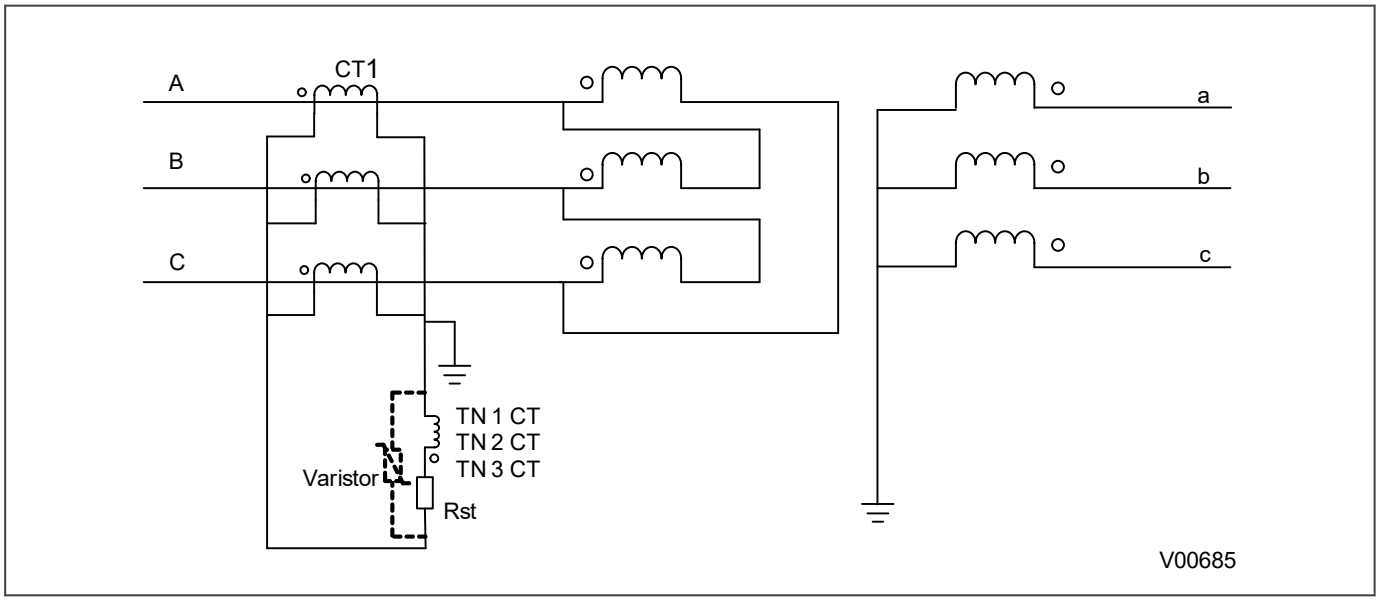


Figure 94: Hi-Z REF protection for a delta winding

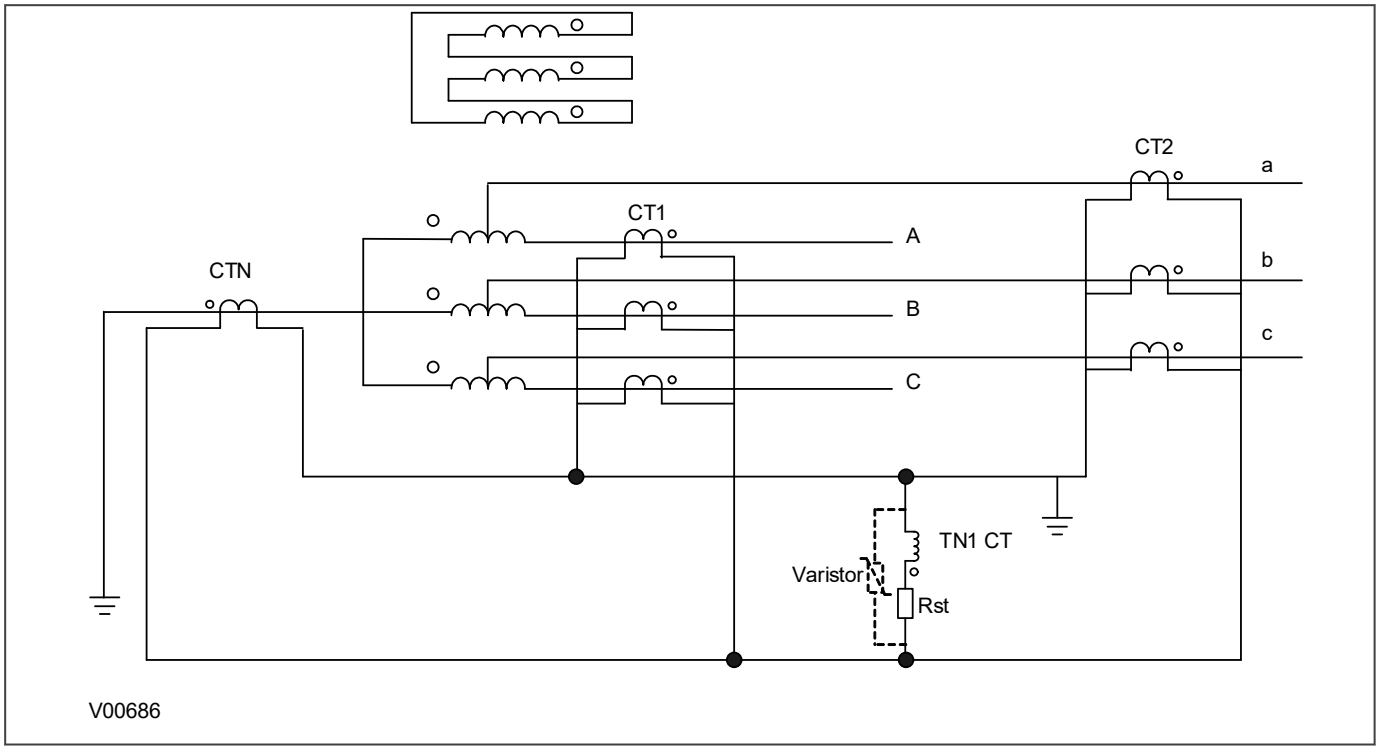


Figure 95: Hi-Z REF protection for autotransformer configuration

8.5.3.2 SETTING GUIDELINES FOR HIGH IMPEDANCE OPERATION

This scheme is very sensitive and can protect against low levels of fault current in resistance grounded systems. In this application, the ***IREF>Is*** settings should be chosen to provide a primary operating current less than 10-25% of the minimum earth fault level.

This scheme can also be used in a solidly grounded system. In this application, the ***IREF>Is*** settings should be chosen to provide a primary operating current between 10% and 60 % of the winding rated current.

The following diagram shows the application of a high impedance REF element to protect the LV winding of a power transformer.

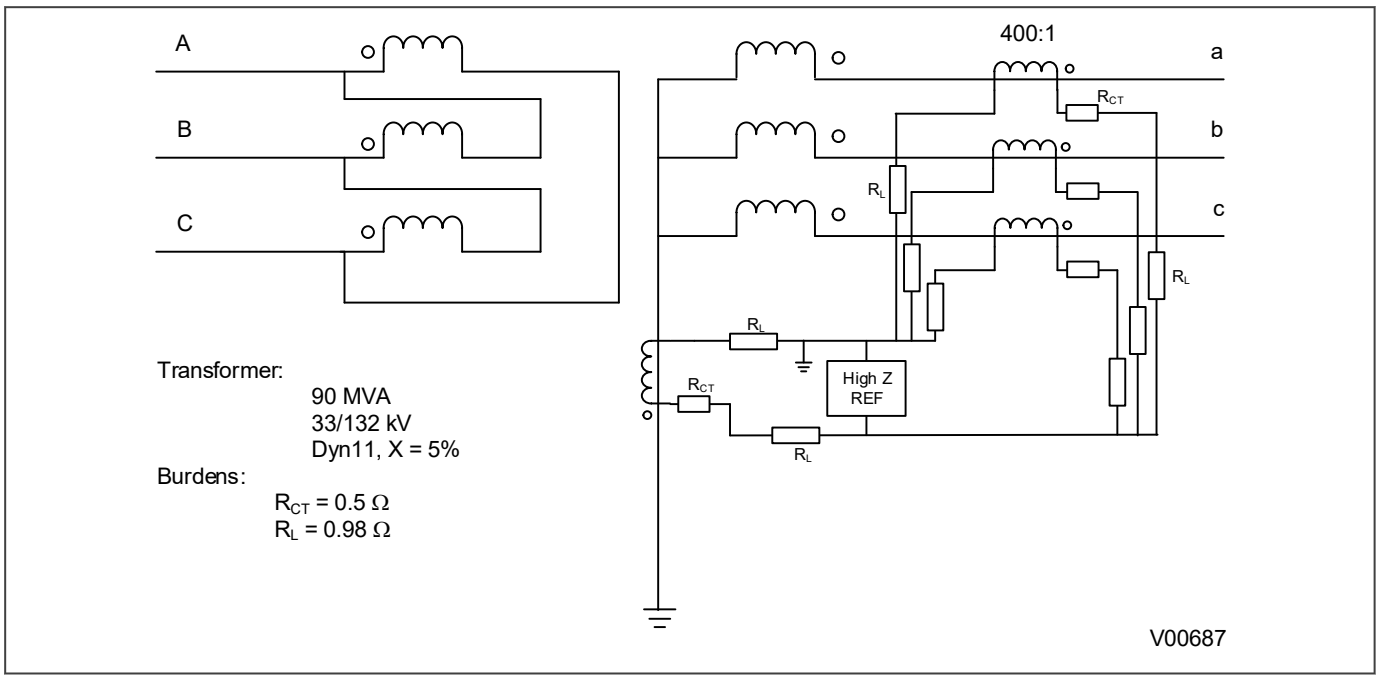


Figure 96: High impedance REF for the LV winding

8.5.3.2.1 STABILITY VOLTAGE CALCULATION

The transformer full load current, IFLC, is:

$$I_{FLC} = (90 \times 10^6)/32 \times 10^3 \times \sqrt{3}) = 394 \text{ A}$$

To calculate the stability voltage the maximum through fault level should be considered. The maximum through fault level, ignoring the source impedance, I_F, is:

$$I_F = I_{FLC}/_{TX} = 394/.05 = 7873 \text{ A}$$

The required stability voltage, VS, and assuming one CT saturated is:

$$V_s = KI_F(R_{CT} + 2R_L)$$

The following figure can be used to determine the K factor and the operating time. The K factor is valid when:

- 5 ≤ X/R ≤ 120

and

- 0.5In ≤ I f ≤ 40In

We recommend a value of VK/VS = 4.

With the transformer at full load current and percentage impedance voltage of 394A and 5% respectively, the prospective fault current is 7873 A and the required stability voltage Vs (assuming that one CT is saturated) is:

$$V_s = 0.9 \times 7873 \times (0.5 + 2 \times 0.98)/400 = 45.5 \text{ V}$$

The CTs knee point voltage should be at least 4 times Vs so that an average operating time of 40 ms is achieved.

8.5.3.2.2 PRIMARY CURRENT CALCULATION

The primary operating current should be between 10 and 60 % of the winding rated current. Assuming that the relay effective setting or primary operating current is approximately 30% of the full load current, the calculation below shows that a setting of less than 0.3 A is required.

$$\text{Effective setting} = 0.3I_{FLC} / \text{CT Ratio} = 0.3 \times 394 / 400 = \text{approximately } 0.3 \text{ A}$$

8.5.3.2.3 STABILISING RESISTOR CALCULATION

Assuming that a setting of 0.1A is selected the value of the stabilizing resistor, R_{ST}, required is

$$R_{ST} = V_s/(\text{IREF} > \text{Is1 (HV)}) = 45.5/0.1 = 455 \text{ ohms}$$

To achieve an average operating time of 40 ms, Vk/Vs should be 3.5.

The Kneepoint voltage is:

$$V_K = 4V_s = 4 \times 45.5 = 182 \text{ V.}$$

If the actual V_K is greater than 4 times V_s, then the K factor increases. In this case, V_s should be recalculated.

Note:
K can reach a maximum value of approximately 1.

8.5.3.2.4 CURRENT TRANSFORMER CALCULATION

The effective primary operating current setting is:

$$I_P = N(I_s + nI_e)$$

By re-arranging this equation, you can calculate the excitation current for each of the current transformers at the stability voltage. This turns out to be:

$$I_e = (0.3 - 0.1) / 4 = 0.05 \text{ A}$$

In summary, the current transformers used for this application must have a kneepoint voltage of 182 V or higher (note that maximum Vk/Vs that may be considered is 16 and the maximum K factor is 1), with a secondary winding resistance of 0.5 ohms or lower and a magnetizing current at 45.5 V of less than 0.05 A.

Assuming a CT kneepoint voltage of 200 V, the peak voltage can be estimated as:

$$V_P = 2\sqrt{2V_K(V_F - V_K)} = 2\sqrt{2(200)(9004-200)} = 3753 \text{ V}$$

This value is above the peak voltage of 3000 V and therefore a non-linear resistor is required.

Note:
The kneepoint voltage value used in the above formula should be the actual voltage obtained from the CT magnetizing characteristic and not a calculated value.

Note:
One stabilizing resistor, part No. ZB9016 756, and one varistor, part No. 600A/S1/S256 might be used.

8.5.3.3 USE OF METROSIL NON-LINEAR RESISTORS

Current transformers can develop high peak voltages under internal fault conditions. Metrosils are used to limit these peak voltages to a value below the maximum withstand voltage (usually 3 kV).

You can use the following formulae to estimate the peak transient voltage that could be produced for an internal fault. The peak voltage produced during an internal fault is a function of the current transformer kneepoint voltage and the prospective voltage that would be produced for an internal fault if current transformer saturation did not occur.

$$Vp = 2\sqrt{(2VK(V_F - V_K))}$$

$$Vf = I'f(R_{CT}+2_{RL}+R_{ST})$$

where:

- Vp = Peak voltage developed by the CT under internal fault conditions
- Vk = Current transformer kneepoint voltage
- Vf = Maximum voltage that would be produced if CT saturation did not occur
- I'f = Maximum internal secondary fault current
- R_{CT} = Current transformer secondary winding resistance
- R_L = Maximum lead burden from current transformer to relay
- R_{ST} = Relay stabilising resistor

You should always use Metrosils when the calculated values are greater than 3000 V. Metrosils are connected across the circuit to shunt the secondary current output of the current transformer from the device to prevent very high secondary voltages.

Metrosils are externally mounted and take the form of annular discs. Their operating characteristics follow the expression:

$$V = CI^{0.25}$$

where:

- V = Instantaneous voltage applied to the Metrosil
- C = Constant of the Metrosil
- I = Instantaneous current through the Metrosil

With a sinusoidal voltage applied across the Metrosil, the RMS current would be approximately 0.52 x the peak current. This current value can be calculated as follows:

$$I_{RMS} = 0.52\left(\frac{\sqrt{2}V_{S(RMS)}}{C}\right)^4$$

where:

- $V_{S(RMS)}$ = RMS value of the sinusoidal voltage applied across the metrosil.

This is due to the fact that the current waveform through the Metrosil is not sinusoidal but appreciably distorted.

The Metrosil characteristic should be such that it complies with the following requirements:

- The Metrosil current should be as low as possible, and no greater than 30 mA RMS for 1 A current transformers or 100 mA RMS for 5 A current transformers.
- At the maximum secondary current, the Metrosil should limit the voltage to 1500 V RMS or 2120 V peak for 0.25 second. At higher device voltages it is not always possible to limit the fault voltage to 1500 V rms, so higher fault voltages may have to be tolerated.

The following tables show the typical Metrosil types that will be required, depending on relay current rating, REF voltage setting etc.

Metrosils for devices with a 1 Amp CT

The Metrosil units with 1 Amp CTs have been designed to comply with the following restrictions:

- The Metrosil current should be less than 30 mA rms.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms if possible.

The Metrosil units normally recommended for use with 1Amp CTs are as shown in the following table:

	Nominal Characteristic		Recommended Metrosil Type	
Device Voltage Setting	**C**	**β**	**Single Pole Relay**	**Triple Pole Relay**
Up to 125 V RMS	450	0.25	600A/S1/S256	600A/S3/1/S802
125 to 300 V RMS	900	0.25	600A/S1/S1088	600A/S3/1/S1195

Note:
Single pole Metrosil units are normally supplied without mounting brackets unless otherwise specified by the customer.

Metrosils for devices with a 5 Amp CT

These Metrosil units have been designed to comply with the following requirements:

- The Metrosil current should be less than 100 mA rms (the actual maximum currents passed by the devices shown below their type description.
- At the maximum secondary internal fault current the Metrosil should limit the voltage to 1500 V rms for 0.25secs. At the higher relay settings, it is not possible to limit the fault voltage to 1500 V rms so higher fault voltages have to be tolerated.

The Metrosil units normally recommended for use with 5 Amp CTs and single pole relays are as shown in the following table:

Secondary Internal Fault Current	Recommended Metrosil Types for Various Voltage Settings			
Amps RMS	Up to 200 V RMS	250 V RMS	275 V RMS	300 V RMS
50A	600A/S1/S1213 C = 540/640 35 mA RMS	600A/S1/S1214 C = 670/800 40 mA RMS	600A/S1/S1214 C =670/800 50 mA RMS	600A/S1/S1223 C = 740/870 50 mA RMS
100A	600A/S2/P/S1217 C = 470/540 70 mA RMS	600A/S2/P/S1215 C = 570/670 75 mA RMS	600A/S2/P/S1215 C =570/670 100 mA RMS	600A/S2/P/S1196 C =620/740 100 mA RMS
150A	600A/S3/P/S1219 C = 430/500 100 mA RMS	600A/S3/P/S1220 C = 520/620 100 mA RMS	600A/S3/P/S1221 C = 570/670 100 mA RMS	600A/S3/P/S1222 C =620/740 100 mA RMS

In some situations single disc assemblies may be acceptable, contact GE Vernova for detailed applications.

Note:
The Metrosils recommended for use with 5 Amp CTs can also be used with triple pole devices and consist of three single pole units mounted on the same central stud but electrically insulated from each other. To order these units please specify "Triple pole Metrosil type", followed by the single pole type reference. Metrosil for higher voltage settings and fault currents are available if required.

8.5.3.4 CT REQUIREMENTS - HIGH IMPEDANCE REF

In a high impedance REF scheme, the required stability voltage requirement is described in terms of an external fault (I_F), burden ($2R_L + R_{CT}$) and a stability factor (K), as follows:

$$V_s => KI_F(2R_L + R_{CT})$$

where:

- I_F = maximum external fault level
- R_{CT} = resistance of CT secondary winding
- R_L = resistance of a single lead from device to current transformer

The assumption that one CT is completely saturated for an external fault does not describe what actually happens when asymmetric CT saturation occurs. The CT that saturates will only saturate during parts of each current waveform cycle. This means that the spill current waveform seen by the differential element will be highly non-sinusoidal. The sensitivity to non-sinusoidal spill waveforms for through-faults will be a function of the REF frequency response, the REF operating time, the REF current setting and the wave shapes.

The frequency response and the operating speed are factors that are inherent to the design. Spill current wave shapes will be related to the ratio of the CT kneepoint voltage (V_K) to the circuit impedance. The stability voltage is determined by the current setting and the stabilising resistor. The stability of the High Impedance REF function during through faults is determined by the ratio V_K/V_S. Where V_K is the CT knee point voltage and V_S is the stability voltage.

The relationship between the V_K/V_S ratio and the required stability factor K has been found to be of a general form for various designs that have undergone conjunctive testing. It is the absolute values of V_K/V_S and K that vary in the relationship for different device designs.

Once stability has been considered, the next performance factor to take into account is the operating time for internal faults. The CT kneepoint voltage as a multiple of the protection stability voltage setting (V_K/V_S) will govern the operating time of a differential relay element for heavy internal faults with transiently offset fault current waveforms. With the aid of the operating time curves derived for the device, it is possible to identify the ratio V_K/V_S that is required to achieve a desired average operating speed for internal faults.

The approach with older electromechanical high impedance relays was to use an universally safe K factor of 1.0, but the older relays operated quickly with a lower V_K/V_s ratio. With more modern IEDs, it is desirable to identify the optimum K factor for stability, so that the required V_K/V_s ratio for stability and operating speed will not make CT kneepoint voltage requirements worse than traditional requirements.

The high impedance REF CT requirements are shown in the following figure. They are valid for:

$5 \leq X/R \leq 120$ and $0.5In \leq 40In$

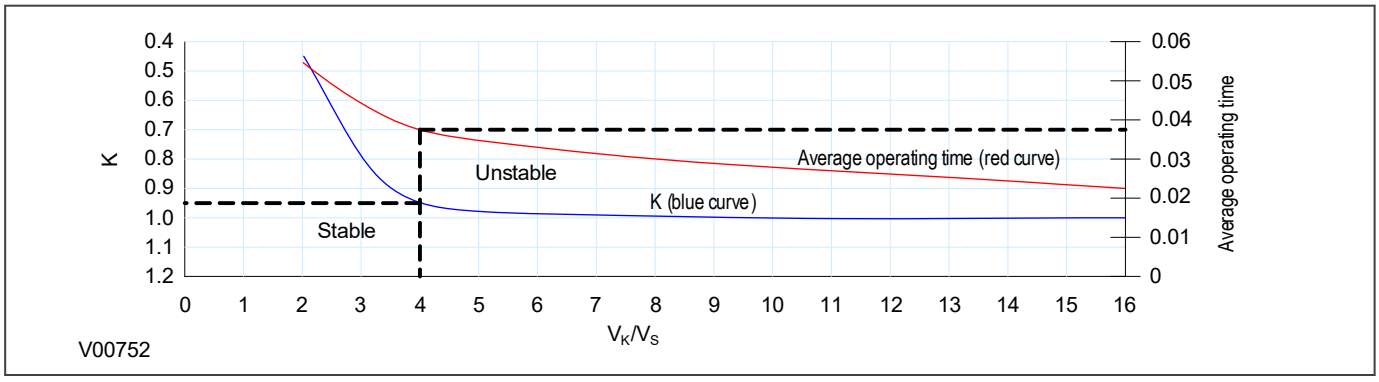


Figure 97: High Impedance REF CT requirement

Using the above graphical tool:

1. Locate the required average operation time on the right-hand side of the vertical axis.
2. Draw a horizontal line across until it intersects the red curve
3. Draw a vertical line from the above intersection point
4. Read off the the Vk/Vs value from the horizontal axis
5. Where this vertical line intersects the blue curve, read off the K value on the left hand side of the vertical axis

If we take the example where the average operating time is 38 ms, the above graphical operations reveal that Vk/Vs = 4 and K = 0.95.

For best accuracy we recommend class X or class 5P current transformers (CTs). The CT requirements for high impedance REF protection are generally lower than those for differential protection. If the line CTs for high impedance REF protection are the same as those used for differential protection, the differential CT requirements cover both differential and high impedance REF applications. However if the line CTs for high impedance REF are not the same as those used for differential protection, the high impedance REF CT requirements can be obtained by using the graph shown above.

CHAPTER 9

CURRENT PROTECTION FUNCTIONS

9.1 CHAPTER OVERVIEW

The 5th Generation provides a wide range of current protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 200
Overcurrent Protection Principles 201
Phase Overcurrent Protection 213
Voltage Dependent Overcurrent Element 221
Negative Sequence Overcurrent Protection 224
Earth Fault Protection 228
Second Harmonic Blocking 234

9.2 OVERCURRENT PROTECTION PRINCIPLES

Most electrical power system faults result in an overcurrent of one kind or another. It is the job of protection devices, formerly known as 'relays' but now known as Intelligent Electronic Devices (IEDs) to protect the power system from faults. The general principle is to isolate the faults as quickly as possible to limit the danger and prevent fault currents flowing through systems, which can cause severe damage to equipment and systems. At the same time, we wish to switch off only the parts of the power grid that are absolutely necessary, to prevent unnecessary blackouts. The protection devices that control the tripping of the power grid's circuit breakers are highly sophisticated electronic units, providing an array of functionality to cover the different fault scenarios for a multitude of applications.

The described products offer a range of overcurrent protection functions including:

- Phase Overcurrent protection
- Earth Fault Overcurrent protection
- Negative Sequence Overcurrent protection
- Sensitive Earth Fault protection

To ensure that only the necessary circuit breakers are tripped and that these are tripped with the smallest possible delay, the IEDs in the protection scheme need to co-ordinate with each other. Various methods are available to achieve correct co-ordination between IEDs in a system. These are:

- By means of time alone
- By means of current alone
- By means of a combination of both time and current.

Grading by means of current alone is only possible where there is an appreciable difference in fault level between the two locations where the devices are situated. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest.

For these reasons the most commonly applied characteristic in co-ordinating overcurrent devices is the IDMT (Inverse Definite Minimum Time) type.

9.2.1 IDMT CHARACTERISTICS

There are two basic requirements to consider when designing protection schemes:

- All faults should be cleared as quickly as possible to minimise damage to equipment
- Fault clearance should result in minimum disruption to the electrical power grid.

The second requirement means that the protection scheme should be designed such that only the circuit breaker(s) in the protection zone where the fault occurs, should trip.

These two criteria are actually in conflict with one another, because to satisfy (1), we increase the risk of shutting off healthy parts of the grid, and to satisfy (2) we purposely introduce time delays, which increase the amount of time a fault current will flow. With IDMT protection applied to radial feeders, this problem is exacerbated by the nature of faults in that the protection devices nearest the source, where the fault currents are largest, actually need the longest time delay.

IDMT characteristics are described by operating curves. Traditionally, these were defined by the performance of electromechanical relays. In numerical protection, equations are used to replicate these characteristics so that they can be used to grade with older equipment.

The old electromechanical relays countered this problem somewhat due to their natural operate time v. fault current characteristic, whereby the higher the fault current, the quicker the operate time. The characteristic typical of these electromechanical relays is called Inverse Definite Minimum Time or IDMT for short.

9.2.1.1 IEC 60255 IDMT CURVES

There are four well-known variants of this characteristic:

- Standard Inverse
- Very inverse
- Extremely inverse
- UK Long Time inverse

These equations and corresponding curves governing these characteristics are very well known in the power industry.

Standard Inverse

This characteristic is commonly known as the 3/10 characteristic, i.e. at ten times setting current and TMS of 1 the relay will operate in 3 seconds.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{0.14}{\left(\frac{I}{I_s}\right)^{0.02} - 1}$$

The standard inverse time characteristic is widely applied at all system voltages – as back up protection on EHV systems and as the main protection on HV and MV distribution systems.

In general, the standard inverse characteristics are used when:

- There are no co-ordination requirements with other types of protective equipment further out on the system, e.g. Fuses, thermal characteristics of transformers, motors etc.
- The fault levels at the near and far ends of the system do not vary significantly.
- There is minimal inrush on cold load pick up. Cold load inrush is that current which occurs when a feeder is energised after a prolonged outage. In general the relay cannot be set above this value but the current should decrease below the relay setting before the relay operates.

Very Inverse

This type of characteristic is normally used to obtain greater time selectivity when the limiting overall time factor is very low, and the fault current at any point does not vary too widely with system conditions. It is particularly suitable, if there is a substantial reduction of fault current as the distance from the power source increases. The steeper inverse curve gives longer time grading intervals. Its operating time is approximately doubled for a reduction in setting from 7 to 4 times the relay current setting. This permits the same time multiplier setting for several relays in series.

The characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{13.5}{\left(\frac{I}{I_s}\right) - 1}$$

Extremely Inverse

With this characteristic the operating time is approximately inversely proportional to the square of the current. The long operating time of the relay at peak values of load current make the relay particularly suitable for grading with fuses and also for protection of feeders which are subject to peak currents on switching in, such as feeders supplying refrigerators, pumps, water heaters etc., which remain connected even after a prolonged interruption of supply.

For cases where the generation is practically constant and discrimination with low tripping times is difficult to obtain, because of the low impedance per line section, an extremely inverse relay can be very useful since only a small difference of current is necessary to obtain an adequate time difference.

Another application for this relay is with auto reclosers in low voltage distribution circuits. As the majority of faults are of a transient nature, the relay is set to operate before the normal operating time of the fuse, thus preventing perhaps unnecessary blowing of the fuse.

Upon reclosure, if the fault persists, the recloser locks itself in the closed position and allows the fuse to blow to clear the fault.

This characteristic is also widely used for protecting plant against overheating since overheating is usually an I2t function.

This characteristic curve can be defined by the mathematical expression:

$$t_{op} = T \frac{80}{\left(\frac{I}{I_s}\right)^2 - 1}$$

UK Long Time Inverse

This type of characteristic has a long time characteristic and may be used for protection of neutral earthing resistors (which normally have a 30 second rating). The relay operating time at 5 times current setting is 30 seconds at a TMS of 1.

This can be defined by:

$$t_{op} = T \frac{120}{\left(\frac{I}{I_s}\right) - 1}$$

In the above equations:

- t_{op} is the operating time
- T is the time multiplier setting
- I is the measured current
- I_s is the current threshold setting.

The ratio I/I_s is sometimes defined as ‘M’ or ‘PSM’ (Plug Setting Multiplier).

These curves are plotted as follows:

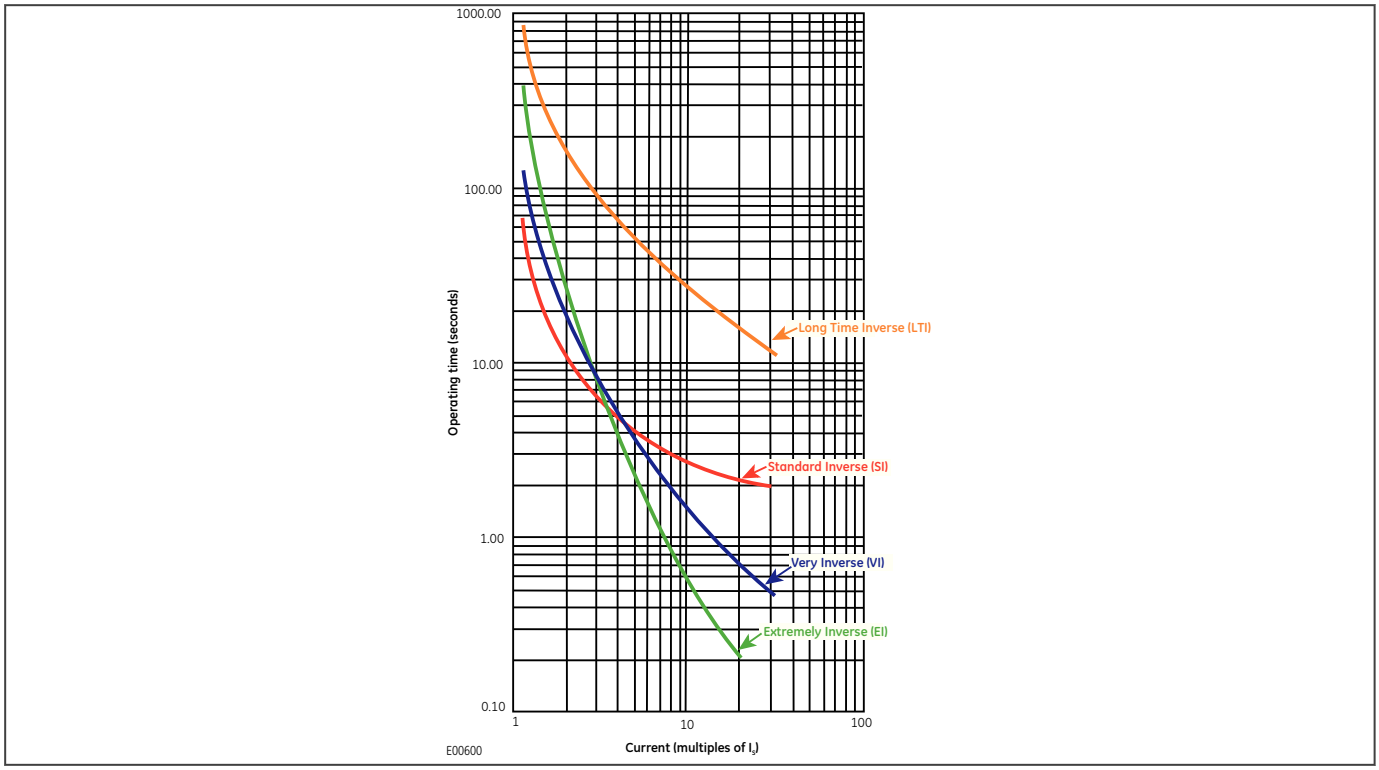


Figure 98: IEC 60255 IDMT curves

9.2.1.2 EUROPEAN STANDARDS

The IEC 60255 IDMT Operate equation is:

$$t_{op} = T\left(\frac{\beta}{M^{\alpha} - 1} + L \right) + C$$

and the IEC 60255 IDMT Reset equation is:

$$t_r = T\left(\frac{\beta}{1 - M^{\alpha}} \right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- T is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/Is)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEC IDMT curves are as follows:

Curve Description	β constant	α constant	L constant
IEC Standard Inverse Operate	0.14	0.02	0
IEC Standard Inverse Reset	8.2	6.45	0

Curve Description	β constant	α constant	L constant
IEC Very Inverse Operate	13.5	1	0
IEC Very Inverse Reset	50.92	2.4	0
IEC Extremely Inverse Operate	80	2	0
IEC Extremely Inverse Reset	44.1	3.03	0
UK Long Time Inverse Operate*	120	1	0
UK Rectifier Operate*	45900	5.6	0

Rapid Inverse (RI) characteristic

The RI operate curve is represented by the following equation:

$$t_{op} = K\left(\frac{1}{0.339 - \frac{0.236}{M}}\right)$$

where:

- t_{op} is the operating time
- K is the Time Multiplier setting
- M is the ratio of the measured current divided by the threshold current (I/I_s)

Note:
** When using UK Long Time Inverse, UK Rectifier or RI for the Operate characteristic, DT (Definite Time) is always used for the Reset characteristic.*

9.2.1.3 NORTH AMERICAN STANDARDS

The IEEE IDMT Operate equation is:

$$t_{op} = TD\left(\frac{\beta}{M^{\alpha} - 1} + L\right) + C$$

and the IEEE IDMT Reset equation is:

$$t_r = TD\left(\frac{\beta}{1 - M^{\alpha}}\right)$$

where:

- t_{op} is the operating time
- t_r is the reset time
- TD is the Time Dial setting
- M is the ratio of the measured current divided by the threshold current (I/I_s)
- β is a constant, which can be chosen to satisfy the required curve characteristic
- α is a constant, which can be chosen to satisfy the required curve characteristic
- C is a constant for adding Definite Time (Definite Time adder)
- L is a constant (usually only used for ANSI/IEEE curves)

The constant values for the IEEE curves are as follows:

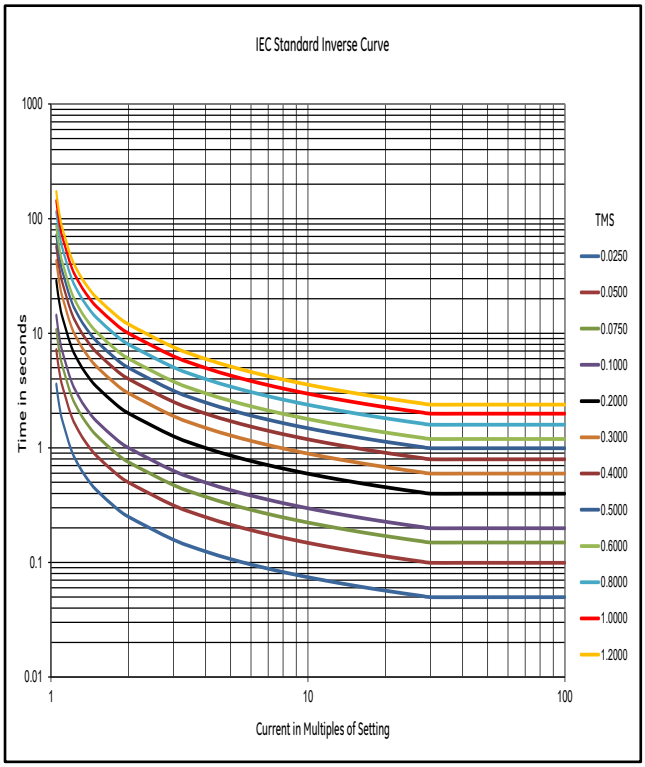
Curve Description	β constant	α constant	L constant
IEEE Moderately Inverse Operate	0.0515	0.02	0.114
IEEE Moderately Inverse Reset	4.85	2	0
IEEE Very Inverse Operate	19.61	2	0.491
IEEE Very Inverse Reset	21.6	2	0
IEEE Extremely Inverse Operate	28.2	2	0.1217
IEEE Extremely Inverse Reset	29.1	2	0
CO8 US Inverse Operate	5.95	2	0.18
CO8 US Inverse Reset	5.95	2	0
CO2 US Short Time Inverse Operate	0.16758	0.02	0.11858
CO2 US Short Time Inverse Reset	2.261	2	0

The constant values for the ANSI curves are as follows:

Curve Description	β constant	α constant	L constant
ANSI Normally Inverse Operate	8.9341	2.0938	0.17966
ANSI Normally Inverse Reset	9	2	0
ANSI Short Time Inverse Operate	0.03393	1.2969	0.2663
ANSI Short Time Inverse Reset	0.5	2	0
ANSI Long Time Inverse Operate	2.18592	1	5.6143
ANSI Long Time Inverse Reset	15.75	2	0

Note:
** When using UK Long Time Inverse or UK Rectifier for the Operate characteristic, DT is always used for the Reset characteristic.*

9.2.1.4 IEC AND IEEE INVERSE CURVES



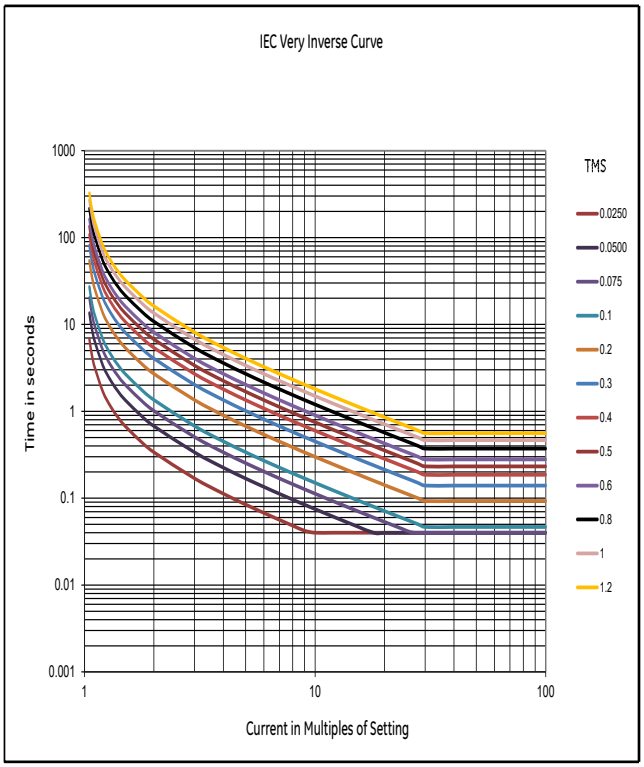


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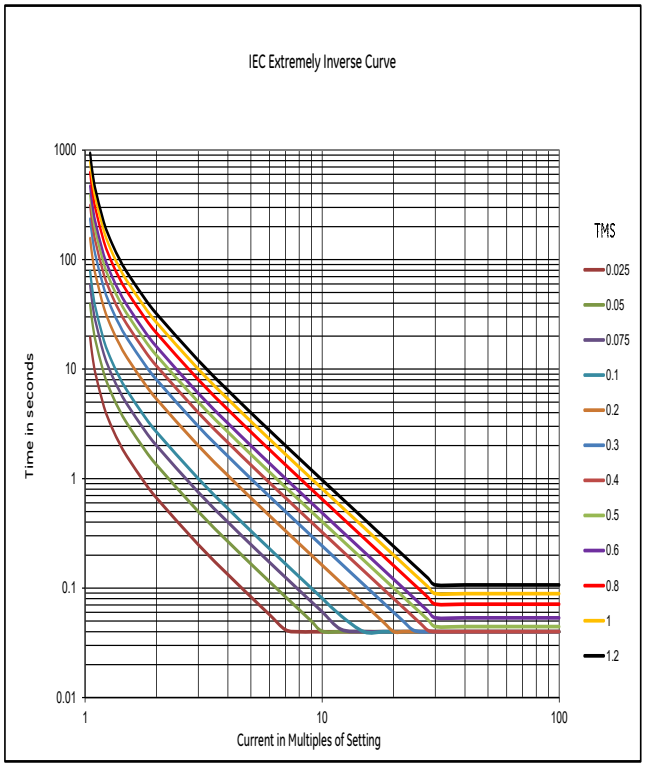
Figure 99: IEC standard and very inverse curves



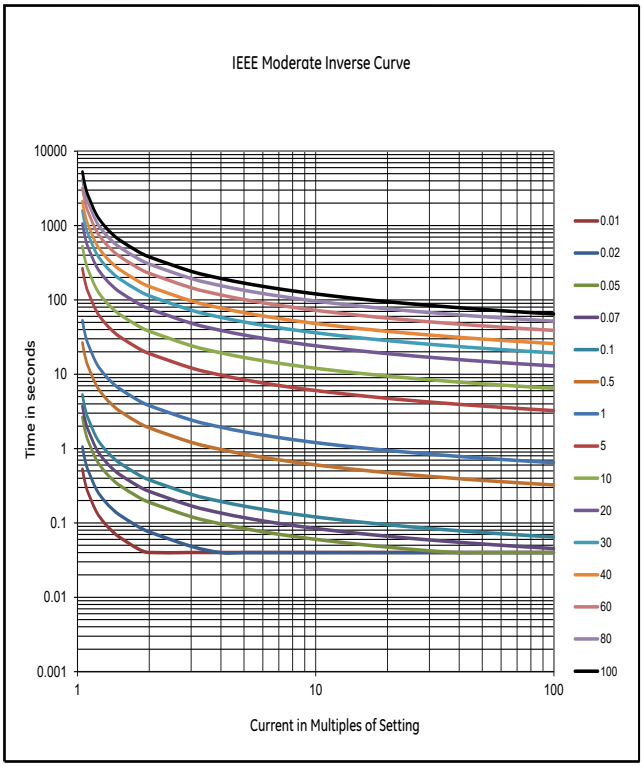


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Figure 100: IEC Extremely inverse and IEEE moderate inverse curves

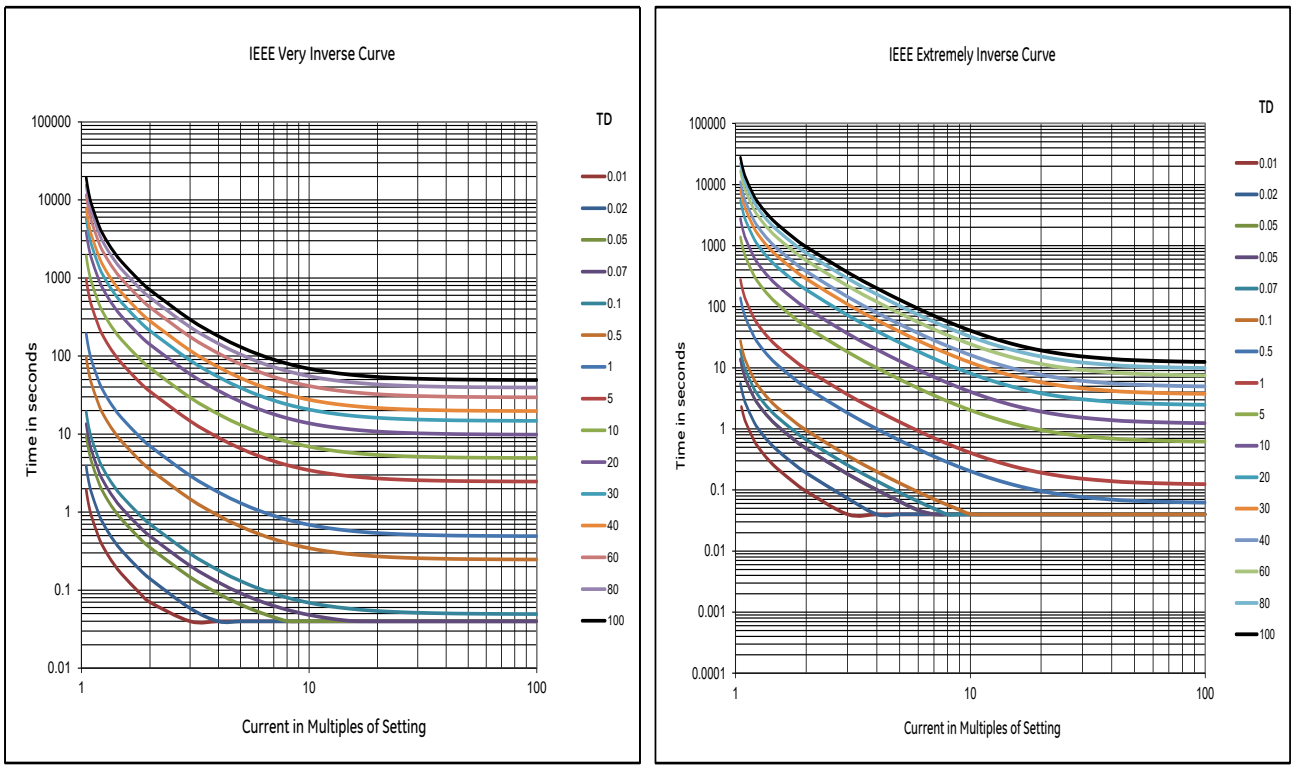

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Figure 101: IEEE very and extremely inverse curves

9.2.1.5 DIFFERENCES BETWEEN THE NORTH AMERICAN AND EUROPEAN STANDARDS

The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A time multiplier setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is used for the IEEE/US curves. The menu is arranged such that if an IEC/UK curve is selected, the ***I> Time Dial*** cell is not visible and vice versa for the TMS setting. For both IEC and IEEE/US type curves, a definite time adder setting is available, which will increase the operating time of the curves by the set value.

9.2.2 PRINCIPLES OF IMPLEMENTATION

The range of protection products provides a very wide range of protection functionality. Despite the diverse range of functionality provided, there is some commonality between the way many of the protection functions are implemented. It is important to describe some of these basic principles before going deeper into the individual protection functions.

A simple representation of protection functionality is shown in the following diagram:

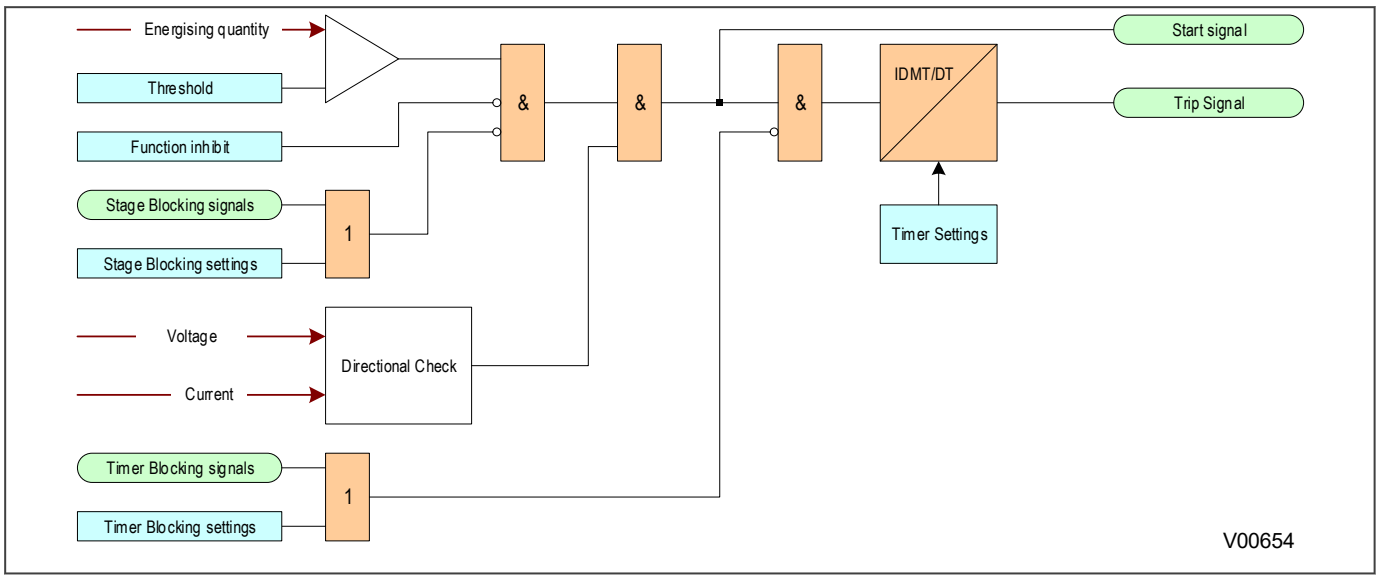


Figure 102: Principle of protection function implementation

An energising quantity is either a voltage input from a system voltage transformer, a current input from a system current transformer or another quantity derived from one or both of these. The energising quantities are extracted from the power system. The signals are converted to digital quantities where they can be processed by the IEDs internal processor.

In general, an energising quantity, be it a current, voltage, power, frequency, or phase quantity, is compared with a threshold value, which may be settable, or hard-coded depending on the function. If the quantity exceeds (for overvalues) or falls short of (for undervalues) the threshold, a signal is produced, which when gated with the various inhibit and blocking functions becomes the Start signal for that protection function. This Start signal is generally made available to Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL) for further processing. It is also passed through a timer function to produce the Trip signal. The timer function may be an IDMT curve, or a Definite Time delay, depending on the function. This timer may also be blocked with timer blocking signals and settings. The timer can be configured by a range of settings to define such parameters as the type of curve, The Time Multiplier Setting, the IDMT constants, the Definite Time delay etc.

In GE Vernova products, there are usually several independent stages for each of the functions, and for three-phase functions, there are usually independent stages for each of the three phases.

Typically some stages use an Inverse Definite Minimum time (IDMT) timer function, and others use a Definite Time timer (DT) function. If the DT time delay is set to '0', then the function is known to be "instantaneous". In many instances, the term 'instantaneous protection" is used loosely to describe Definite Time protection stages, even when the stage may not theoretically be instantaneous.

Many protection functions require a direction-dependent decision. Such functions can only be implemented where both current and voltage inputs are available. For such functions, a directional check is required, whose output can block the Start signal should the direction of the fault be wrong.

Note:
In the logic diagrams and descriptive text, it is usually sufficient to show only the first stage, as the design principles for subsequent stages are usually the same (or at least very similar). Where there are differences between the functionality of different stages, this is clearly indicated.

9.2.2.1 TIMER HOLD FACILITY

The Timer Hold facility is available for stages with IDMT functionality , and is controlled by the timer reset settings for the relevant stages (e.g. ***I>1 tReset***, ***I>2 tReset***). These cells are not visible for the IEEE/US curves if an

inverse time reset characteristic has been selected, because in this case the reset time is determined by the time dial setting (TDS).

This feature may be useful in certain applications, such as when grading with upstream electromechanical overcurrent relays, which have inherent reset time delays. If you set the hold timer to a value other than zero, the resetting of the protection element timers will be delayed for this period. This allows the element to behave in a similar way to an electromechanical relay. If you set the hold timer to zero, the overcurrent timer for that stage will reset instantaneously as soon as the current falls below a specified percentage of the current setting (typically 95%).

Another situation where the timer hold facility may be used to reduce fault clearance times is for intermittent faults. An example of this may occur in a plastic insulated cable. In this application it is possible that the fault energy melts and reseals the cable insulation, thereby extinguishing the fault. This process repeats to give a succession of fault current pulses, each of increasing duration with reducing intervals between the pulses, until the fault becomes permanent.

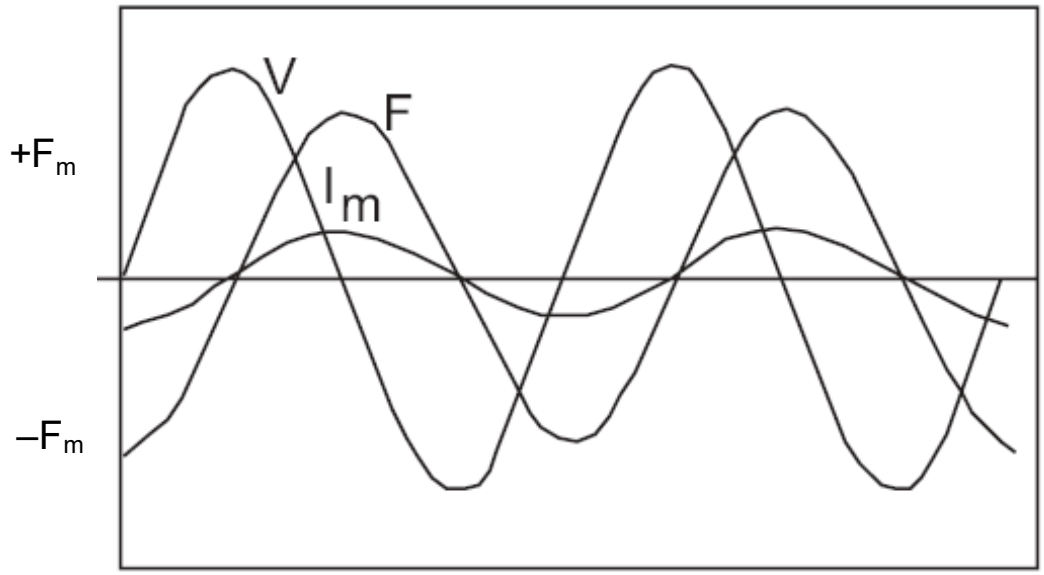
When the reset time is instantaneous, the device will repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the device will integrate the fault current pulses, thereby reducing fault clearance time.

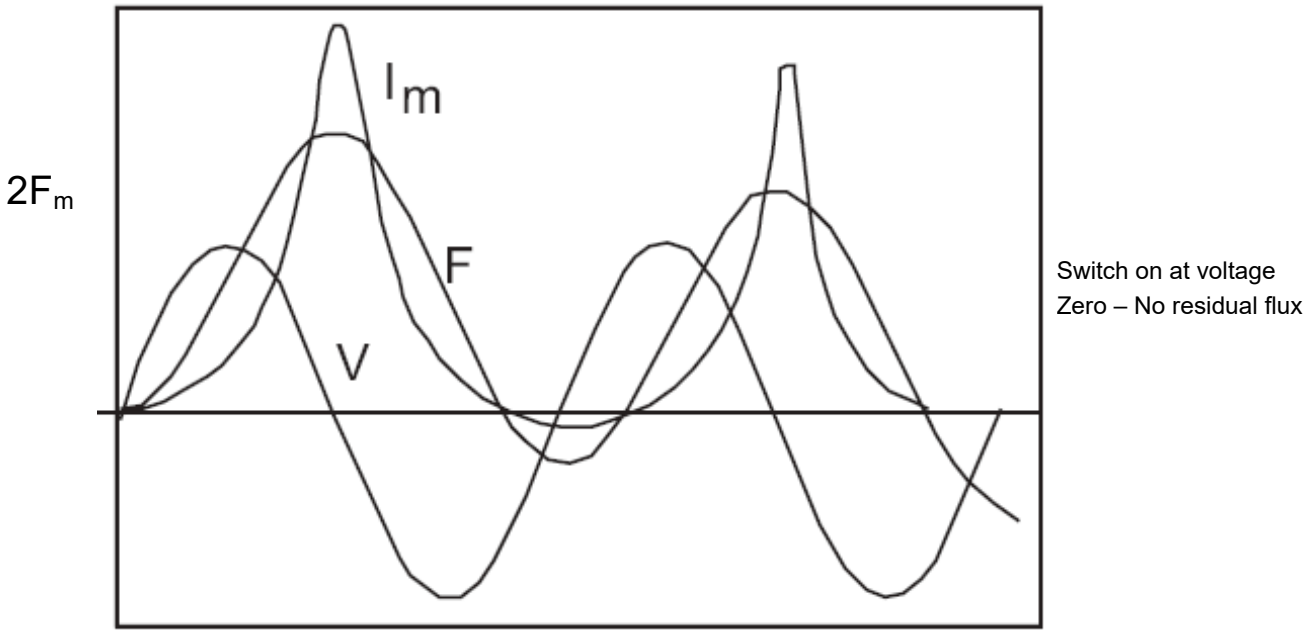
9.2.3 MAGNETISING INRUSH RESTRAINT

Whenever there is an abrupt change of magnetising voltage (e.g. when a transformer is initially connected to a source of AC voltage), there may be a substantial surge of current through the primary winding called inrush current.

In an ideal transformer, the magnetizing current would rise to approximately twice its normal peak value as well, generating the necessary MMF to create this higher-than-normal flux. However, most transformers are not designed with enough of a margin between normal flux peaks and the saturation limits to avoid saturating in a condition like this, and so the core will almost certainly saturate during this first half-cycle of voltage. During saturation, disproportionate amounts of MMF are needed to generate magnetic flux. This means that winding current, which creates the MMF to cause flux in the core, could rise to a value way in excess of its steady state peak value. Furthermore, if the transformer happens to have some residual magnetism in its core at the moment of connection to the source, the problem could be further exacerbated.

The following figure shows the magnetizing inrush phenomenon:





V = Voltage, F = Flux, Im = magnetising current, Fm = maximum flux

E03123

Figure 103: Magnetising inrush phenomenon

The main characteristics of magnetising inrush currents are:

- Higher magnitude than the transformer rated current magnitude
- Containing harmonics and DC offset
- Much longer time constant than that of the DC offset component of fault current

We can see that inrush current is a regularly occurring phenomenon and should not be considered a fault, as we do not wish the protection device to issue a trip command whenever a transformer is switched on at an inconvenient point during the input voltage cycle. This presents a problem to the protection device, because it should always trip

on an internal fault. The problem is that typical internal transformer faults may produce overcurrents which are not necessarily greater than the inrush current. Furthermore, faults tend to manifest themselves on switch on, due to the high inrush currents. For this reason, we need to find a mechanism that can distinguish between fault current and inrush current. Fortunately, this is possible due to the different natures of the respective currents. An inrush current waveform is rich in harmonics, especially 2nd harmonics, whereas an internal fault current consists only of the fundamental. We can therefore develop a restraining method based on the 2nd harmonic content of the inrush current. The mechanism by which this is achieved, is called second harmonic blocking.

9.3 PHASE OVERCURRENT PROTECTION

Phase current faults are faults where fault current flows between two or more phases of a power system. The fault current may be between the phase conductors only or, between two or more phase conductors and earth.

Although not as common as earth faults (single phase to earth), phase faults are typically more severe.

9.3.1 PHASE OVERCURRENT PROTECTION FOR POWER TRANSFORMERS

A fault external to a power transformer can result in damage to the transformer. If the fault is not cleared promptly, the resulting overload on the transformer can cause severe overheating and failure. Overcurrent elements may be used to clear the transformer from a faulted bus or line before the transformer is damaged.

For faults internal to the transformer, the overcurrent protection is less effective because sensitive settings and fast operation times are usually not possible.

Sensitive settings are not possible because the pickup should allow overloading of the transformer when required. Fast operating times are not possible because of the grading required with respect to downstream overcurrent relays.

9.3.2 PHASE OVERCURRENT PROTECTION IMPLEMENTATION

The product provides three overcurrent elements for backup phase overcurrent protection. Each element provides four-stages of non-directional or directional three-phase overcurrent protection with independent time delay characteristics. You can select the overcurrent element operating quantity for each of the elements with the setting cells ***Overcurrent 1***, ***Overcurrent 2*** and ***Overcurrent 3*** in the *OVERCURRENT* column of the relevant settings group. You can set each element as `T1`, `T2`, `T3`, `T4`, `T5`, `HV winding`, `LV winding` or `TV winding`. The HV, LV and TV windings comprise the vector sums of the CT inputs assigned to that particular winding.

All overcurrent and directional settings apply to all three phases but are independent for each of the four stages. You may set the overcurrent element as directional only if the three phase VT input is available in the P643/5 and if the two single phase VT inputs are available in the P642. You may assign the VT to either of the HV, LV or TV windings. Therefore, overcurrent directional elements are available for the current inputs associated with the winding that has the VT input assigned.

The first two stages of overcurrent protection have time-delayed characteristics which you can set as IDMT or DT. The third and fourth stages have definite time characteristics only.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***I>(n) Function*** for the overcurrent operate characteristic
- ***I>(n) Reset Char*** for the overcurrent reset characteristic (IEEE curves only)

where (n) is the number of the stage.

The IDMT-capable stages (1 and 2) also provide a Timer Hold facility. This is configured using the cells ***I>(n) tReset***, where (n) is the number of the stage. This is not applicable for curves based on the IEEE standard.

> *Note:*
> *Stages 3 and 4 can have definite time characteristics only.*

9.3.3 SELECTING THE CURRENT INPUTS

The P642 has two current terminal inputs (T1 and T2), the P643 has up to three terminal current inputs (T1 to T3), and the P645 has up to five current terminal inputs (T1 to T5).

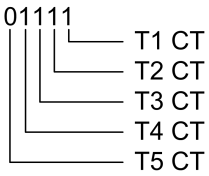
For the P642, you associate one terminal current input with the HV (High Voltage) winding and the other with the LV (Low Voltage) winding.

For the P643 and P645 you can choose to associate more than one terminal current input with particular windings. In cases where more than one terminal CT is associated with a winding, the input to the differential protection function uses the vector sum of the current terminal inputs (on a phase by phase basis) as the input to the calculation for that winding.

You associate these current inputs with the system transformer windings with the settings ***HV CT Terminals***, ***LV CT Terminals*** and ***TV CT Terminals*** in the *SYSTEM CONFIG* column as follows:

Setting	P642	P643	P645
HV CT Terminals	01	001 011	00001 00011 00111 01011 01111
LV CT Terminals	10	100 110	10000 11000 11100 11010 11110
TV CT Terminals		010	00100 01100 00110 01110

Where the terminals T1 to T5 correspond to the bits in the binary string as follows (1 = in use, 0 = not in use). The bit order starts with T1 on the right-hand side. For example:



If a CT is assigned to more than one winding, then an alarm is issued (***CT Selection Alm***). When this DDB signal is asserted, the protection is also blocked.

Winding associations for the P643

If an overcurrent element is assigned to the HV winding then the associated setting ***I>(n) Current Set*** is relative to the T1 CT. Therefore if if the T1 CT setting is changed, then ***I>(n) Current Set*** will be affected accordingly.

The same is true for the LV winding and its associated T3 CT as well as for the TV winding and its associated T2 CT.

Winding associations for the P645

If an overcurrent element is assigned to the HV winding then the associated setting ***I>(n) Current Set*** is relative to the T1 CT. Therefore if the T1 CT setting is changed, then ***I>(n) Current Set*** will be affected accordingly.

The same is true for the LV winding and its associated T5 CT as well as for the TV winding and its associated T3 CT.

9.3.4 NON-DIRECTIONAL OVERCURRENT LOGIC

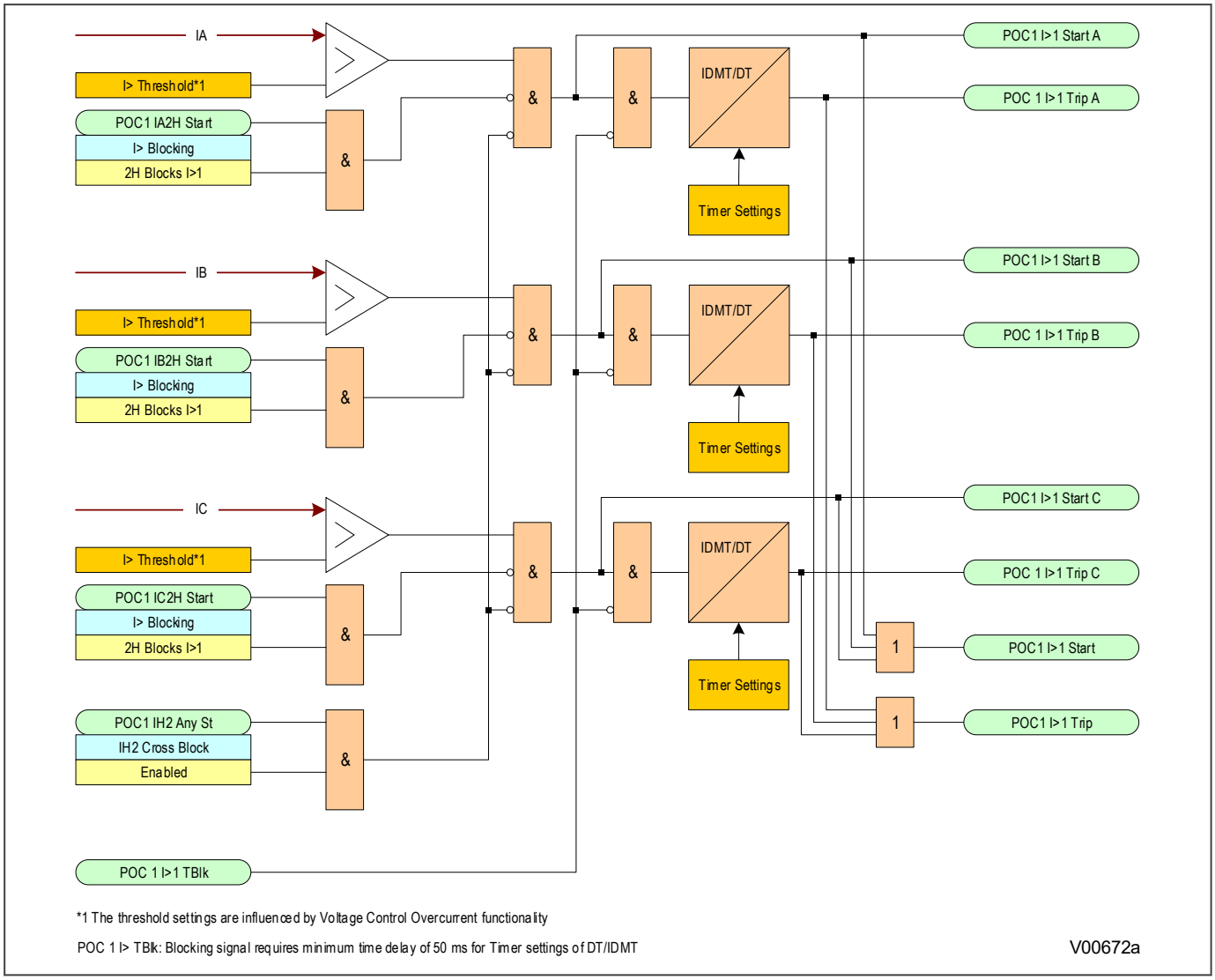


Figure 104: Non-directional overcurrent logic diagram

Phase Overcurrent Modules are level detectors that detect when the current magnitude exceeds a set threshold. When this happens, the Phase Overcurrent Module in question issues a signal, which is gated with some blocking signals to produce the ***Start*** signal. This ***Start*** signal is gated with other blocking signals and applied to the IDMT/DT timer module. It is also made available directly to the user for use in the PSL. For each stage, there are three Phase Overcurrent Modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal.

The outputs of the IDMT/DT timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal.

The IDMT/DT timer modules can be blocked by:

- A Phase Overcurrent Timer Block (***I>(n) Timer Block***)

If any one of the above signals is high, or goes high before the timer has counted out, the IDMT/DT timer module is inhibited (effectively reset) until the blocking signal goes low again. There are separate phase overcurrent timer block signals, which are independent for each overcurrent stage.

The start signal can be blocked by:

- The Second Harmonic blocking function on a per phase basis or for all three phases. The relevant bits are set in the ***I> Blocking*** cell and this is combined with the relevant second harmonic blocking DDBs.

The G14 Data type is used for the ***I>Blocking*** setting:

Bit number	I> Blocking function
Bit 0	VTS Blocks I>1
Bit 1	VTS Blocks I>2
Bit 2	VTS Blocks I>3
Bit 3	VTS Blocks I>4
Bit 4	2H Blocks I>1
Bit 5	2H Blocks I>2
Bit 9	2H Blocks I>3
Bit 10	2H Blocks I>4

These can be set via the Front panel HMI or with the settings application software.

The Phase Overcurrent threshold setting can be influenced by the Voltage Controlled Overcurrent functions, if this functionality is available and used.

9.3.5 DIRECTIONAL ELEMENT

If fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Once the direction has been determined the device can decide whether to allow tripping or to block tripping. To determine the direction of a phase overcurrent fault, the device must compare the phase angle of the fault current with that of a known reference quantity. The phase angle of this known reference quantity must be independent of the faulted phase. Typically this will be the line voltage between the other two phases.

The phase fault elements of the IEDs are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of Protection	Operate Current	Polarising Voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Under system fault conditions, the fault current vector lags its nominal phase voltage by an angle depending on the system X/R ratio. The IED must therefore operate with maximum sensitivity for currents lying in this region. This is achieved by using the IED characteristic angle (RCA). This is the is the angle by which the current applied to the IED must be displaced from the voltage applied to the IED to obtain maximum sensitivity.

The device provides a setting ***I> Char Angle***, which is set globally for all overcurrent stages. It is possible to set characteristic angles anywhere in the range –95° to +95°.

A directional check is performed based on the following criteria:

Directional forward

$$-90° < (\text{angle}(I) - \text{angle}(V) - RCA) < 90°$$

Directional reverse

$$-90° > (\text{angle}(I) - \text{angle}(V) - RCA) > 90°$$

9.3.5.1 IMPLEMENTING DIRECTIONALISATION

A directional element is available for all of the phase overcurrent stages in this device. These are found in the direction setting cells for the relevant stage (e.g. ***I>1 Direction***, ***I>2 Direction***). They can be set to non-directional, directional forward, or directional reverse.

Under system fault conditions, the fault current vector will lag its nominal phase voltage by an angle dependent upon the system X/R ratio. Therefore the device must operate with maximum sensitivity for currents lying in this region. This is achieved by means of the characteristic angle (RCA) setting, which defines the angle by which the applied current must be displaced from the applied voltage in order to obtain maximum sensitivity. This is set in cell ***I>Char Angle***. You can set characteristic angles anywhere in the range from –95° to +95°.

In the P642, the standard single-phase VT input cam be complemented by an optional single-phase VT that can be used to directionalise some of the overcurrent protection elements. This connection is shown on the wiring diagrams and labelled as '$V_{bc\ OPTIONAL}$'. The settings for the optional VT input that can be used to directionalise overcurrent elements are the same as those for the overfluxing input and are described by the ***Aux' VT Location, Aux' VT Primary*** and ***Aux' VT Sec'y*** settings in the *CT AND VT RATIOS* column.

In the P643 and P645, the standard single-phase VT input can be complemented by an optional three-phase VT input that can be used to directionalise some of the overcurrent protection elements. This connection is shown on the wiring diagrams and labelled as ‘OPTIONAL”. The settings for the optional VT input that can be used to directionalise overcurrent elements are those described by the ***’Main VT Location, Main VT Primary*** and ***Main VT Sec'y*** settings settings in the *CT AND VT RATIOS* column.

The overcurrent elements that can be directionalised are those associated with the windings to which the optional VTs are assigned. You can only directionalise overcurrent elements associated with the winding to which the optional input is assigned.

So, to provide directional overcurrent you need:

- To have the appropriate VT option
- Connect the VT input to the winding that you want directional protection for AND assign the optional VT input to that winding in the *CT AND VT RATIOS* column
- Set the overcurrent to directional (either forward or reverse).

As well as directionalising a particular winding current, for models with more than two winding inputs, you can directionalise individual inputs if they are associated with that winding.

For close up three-phase faults, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the device includes a synchronous polarisation feature that stores the pre-fault voltage information and continues to apply this to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time-delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

9.3.5.2 DIRECTIONAL OVERCURRENT LOGIC

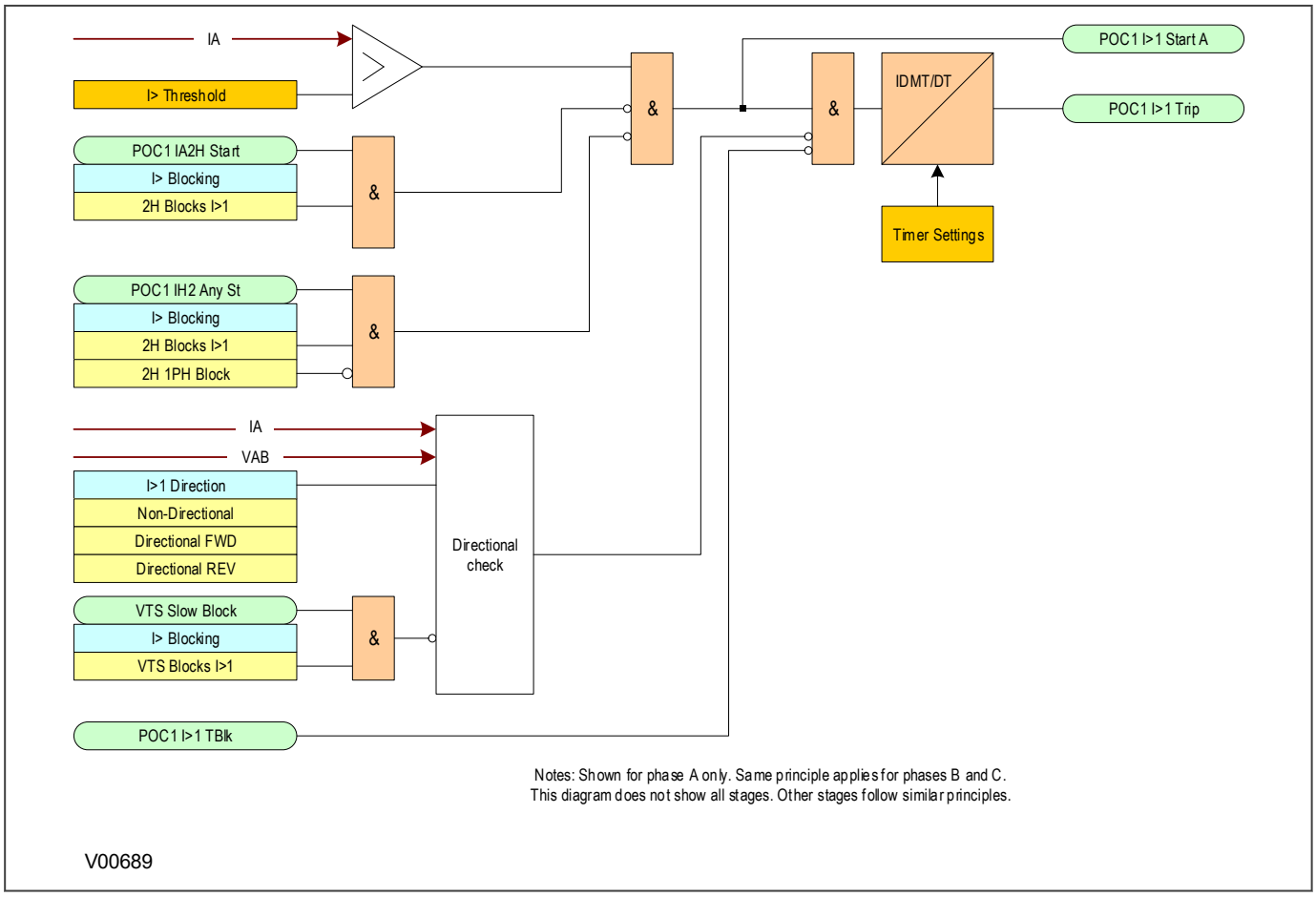


Figure 105: Directional overcurrent logic diagram

The directional overcurrent logic works the same way as non-directional logic except that there is a Directional Check function, based on the following criteria:

- Directional forward: -90° < (angle(I) - angle(V) - RCA) < 90°
- Directional reverse: -90° > (angle(I) - angle(V) - RCA) > 90°

The polarising voltages for each phase are as follows:

Phase of Protection	Operate Current	Polarising Voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

When the element is selected as directional, blocking of the Voltage Transformer Supervision (VTS Block) is available (***I>Blocking*** cell). When the relevant bit is set to 1, operation of the VTS will block the stage if directionalised. When set to 0, the stage will revert to non-directional on operation of the VTS.

9.3.6 APPLICATION NOTES

9.3.6.1 SETTING GUIDELINES

The overcurrent inverse time characteristic on the HV side of the transformer must grade with the overcurrent inverse time characteristic on the LV side which in turn must grade with the LV outgoing circuits. The overcurrent function provides limited protection for internal transformer faults because sensitive settings and fast operation times are usually not possible. Sensitive settings are not possible because the pickup should allow overloading of the transformer when required. Fast operating times are not possible because of the grading required with respect to downstream overcurrent relays. To allow fast operating times, phase instantaneous overcurrent functions with low transient overreach are required.

The pickup of the time delayed overcurrent element can be set to 125-150% of the maximum MVA rating to allow overloading of the transformer according to IEEE Std. C37.91-2000.

As recommended by IEEE Std. C37.91-2000, you should set the instantaneous overcurrent element to pick up at a value higher than the maximum asymmetrical through fault current. This is usually the fault current through the transformer for a low-side three-phase fault. For instantaneous elements, variations in settings of 125–200% are common. For elements subject to transient overreach, a pickup of 175% of the calculated maximum low-side three-phase symmetrical fault current generally provides sufficient margin to avoid false tripping for a low-side bus fault, while still providing protection for severe internal faults. Due to low transient overreach of the third and fourth overcurrent stages, you may set the instantaneous overcurrent element to 120-130% of the through-fault level, thus ensuring stability for through faults. The instantaneous pickup setting should also consider the effects of transformer magnetising inrush current.

In summary, there are a few application considerations to make when applying overcurrent devices to protect a transformer:

- When applying overcurrent protection to the HV side of a power transformer it is usual to apply a high set instantaneous overcurrent element in addition to the time delayed low-set, to reduce fault clearance times for HV fault conditions. Typically, this will be set to approximately 1.3 times the LV fault level, so that it will only operate for HV faults. A 30% safety margin is sufficient due to the low transient overreach of the third and fourth overcurrent stages. Transient overreach defines the response of a relay to DC components of fault current and is quoted as a percentage. A device with a low transient overreach will be largely insensitive to a DC offset and may therefore be set more closely to the steady state AC waveform.
- The second requirement for this element is that it should remain inoperative during transformer energisation, when a large primary current flows for a transient period. In most applications, the requirement to set the device above the LV fault level will automatically result in settings that will be above the level of magnetising inrush current.

With the third and fourth overcurrent stages, it is possible to apply settings corresponding to 40% of the peak inrush current while maintaining stability for the condition.

Where an instantaneous element is required to accompany the time delayed protection, as described above, you should use the third or fourth overcurrent stages as these have wider setting ranges.

9.3.6.2 PARALLEL FEEDERS

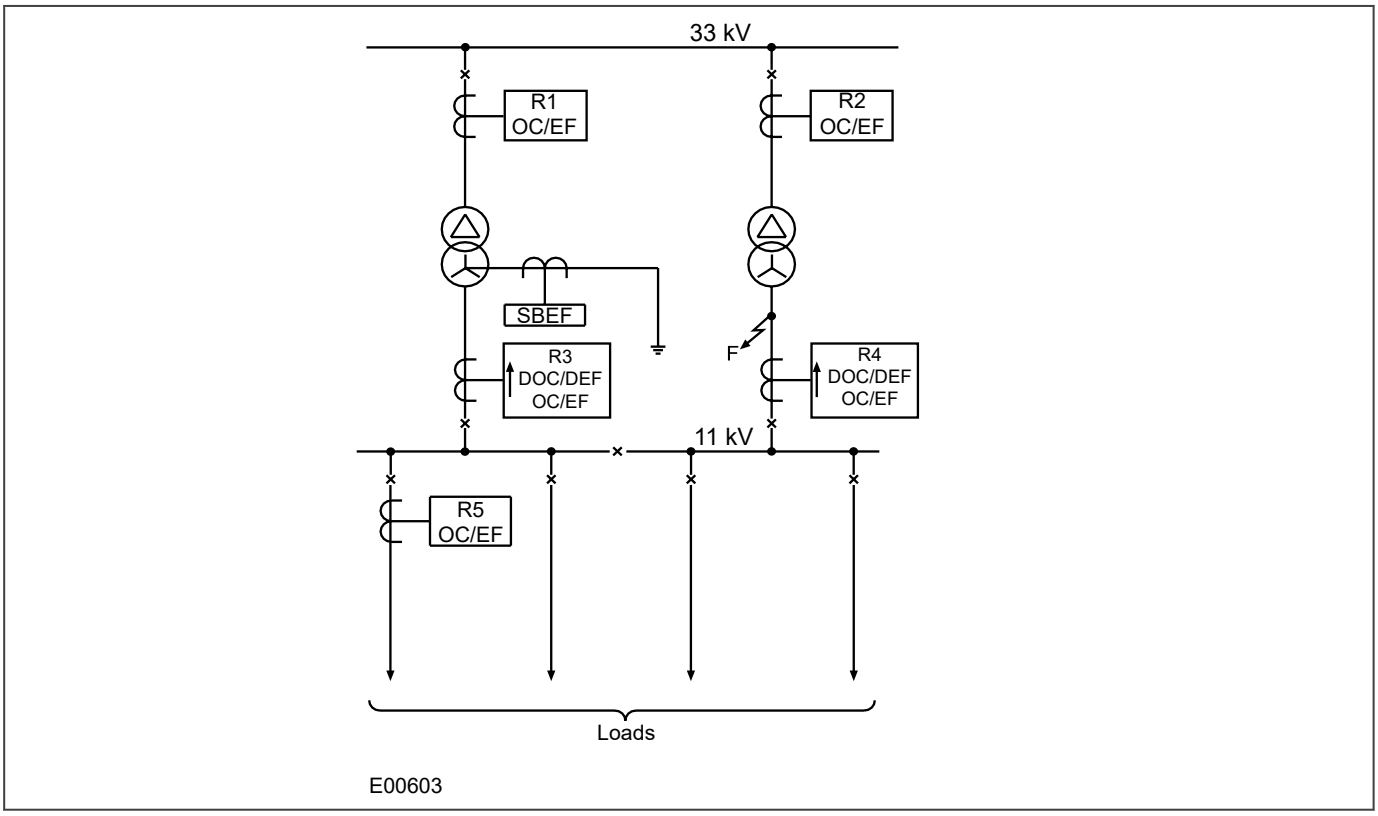


Figure 106: Typical distribution system using parallel transformers

In the application shown in the diagram, a fault at 'F' could result in the operation of both R3 and R4 resulting in the loss of supply to the 11 kV busbar. Hence, with this system configuration, it is necessary to apply directional protection devices at these locations set to 'look into' their respective transformers. These devices should co-ordinate with the non-directional devices, R1 and R2, to ensure discriminative operation during such fault conditions.

In such an application, R3 and R4 may commonly require non-directional overcurrent protection elements to provide protection to the 11 kV busbar, in addition to providing a back-up function to the overcurrent devices on the outgoing feeders (R5).

For this application, stage 1 of the R3 and R4 overcurrent protection would be set to non-directional and time graded with R5, using an appropriate time delay characteristic. Stage 2 could then be set to directional (looking back into the transformer) and also have a characteristic which provides correct co-ordination with R1 and R2. Directionality for each of the applicable overcurrent stages can be set in the directionality cells (***I>1 Direction***).

Note:
The principles outlined for the parallel transformer application are equally applicable for plain feeders that are operating in parallel.

9.4 VOLTAGE DEPENDENT OVERCURRENT ELEMENT

Where long feeders are protected by overcurrent devices, the detection of remote phase-to-phase faults may prove difficult due to the fact that the current pick-up of phase overcurrent elements must be set above the maximum load current, thereby limiting the element's minimum sensitivity.

If the current seen by a local device for a remote fault condition is below its overcurrent setting, a voltage dependent element may be used to increase the sensitivity to such faults. As a reduction in system voltage will occur during overcurrent conditions, this may be used to enhance the sensitivity of the overcurrent protection by reducing the pick up level.

The voltage dependant overcurrent element (either voltage controlled or voltage restrained) remains blocked unless the associated breaker is closed. However, even when this element is blocked due to the breaker being opened, the undervoltage element settings, ***V<1 Poledead Inh*** or ***V<2 Poledead Inh***, can be used to block the undervoltage element.

The voltage dependant overcurrent element is also provided with a timer hold setting, which, if set to a value other than zero, delays the resetting of the protection element timers for this period.

9.4.1 CURRENT SETTING THRESHOLD SELECTION

The threshold setting used in the level detector depends on whether there is a Voltage Dependent condition. The Overcurrent function selects the threshold setting according to the following diagram:

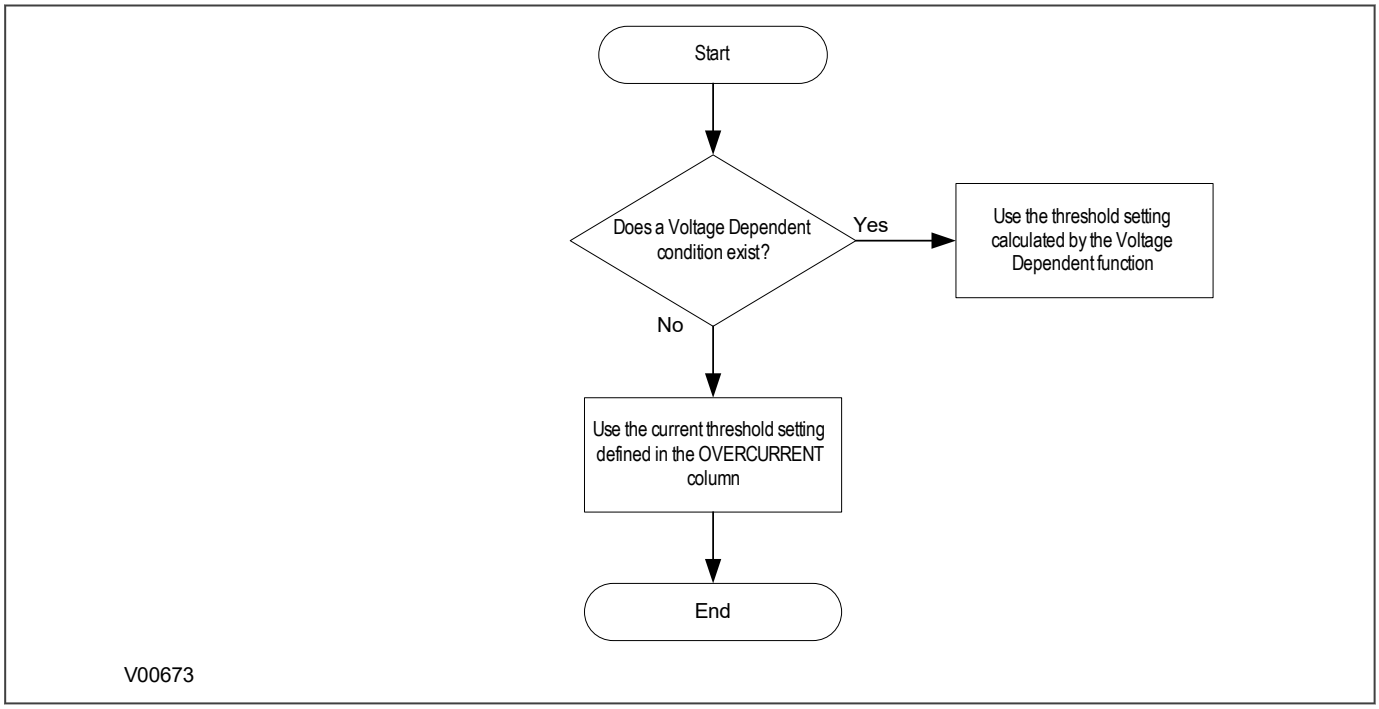


Figure 107: Selecting the current threshold setting

9.4.2 VCO IMPLEMENTATION

Voltage Controlled Overcurrent Protection is implemented in the *OVERCURRENT* column of the relevant settings group, under the sub-heading *VCONTROLED O/C*.

The function is available for in two stages, 1 and 2. When VCO is enabled, the under voltage detector is used to produce a step change in the current setting, when the voltage falls below the voltage setting ***VCO>1 V<Setting*** for stage 1 and ***VCO>2 V<Setting*** for stage 2. To achieve this, the current setting is multiplied by a constant, which is less than 1, set by ***VCO>1 k Setting*** for stage 1 and ***VCO>2 k Setting*** for stage 2.

Each of the stages can be set to HV Winding, LV Winding, TV Winding, T1, T2, T3, T4, or T5. If the current signal chosen for a VCO stage does not belong to the winding where the VT is located, then the VCO element is blocked and a configuration error alarm is asserted.

The operating characteristic of the current setting when voltage controlled mode is selected is as follows:

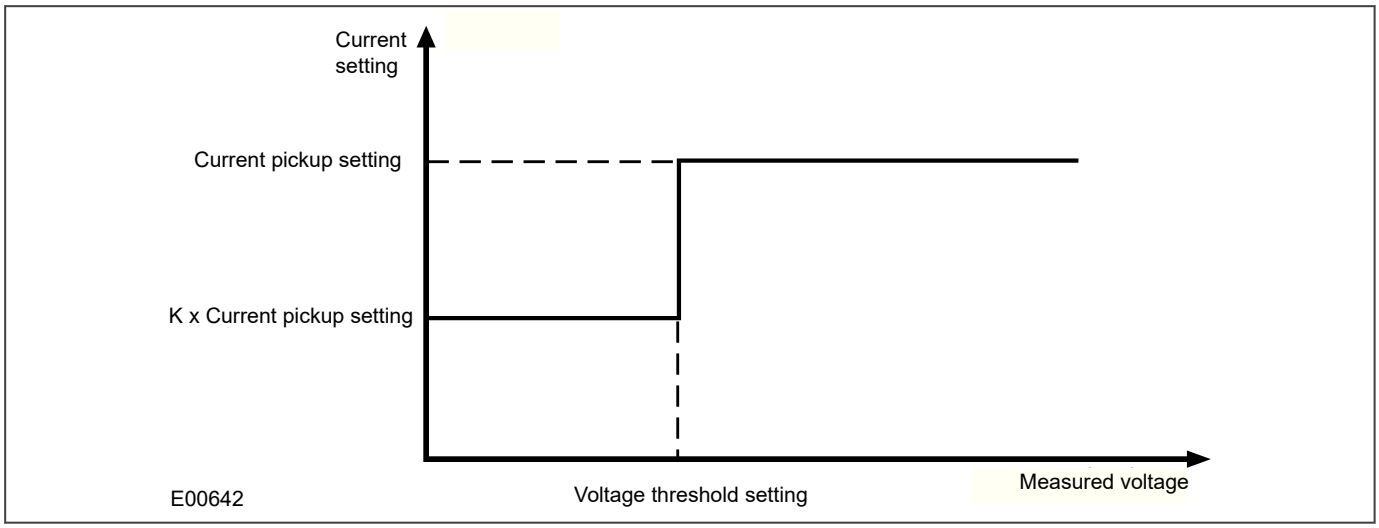


Figure 108: Modification of current pickup level for voltage controlled overcurrent protection

In the P643 and P645, VCO requires an optional three-phase VT to be fitted, and in the P642 it requires that two single-phase VTs are fitted. In P643/5, the phase-to-phase voltages are derived from the measured phase-to-neutral voltages. In the P642, two phase-to-phase voltages are measured and the third one is calculated. In the P642 Vab and Vbc are measured, then Vca is calculated.

9.4.3 VRO IMPLEMENTATION

Voltage Restrained Overcurrent protection is implemented in the *OVERCURRENT* column of the relevant settings group, under the sub-heading *V DEPENDANT O/C*. The function is available in two stages 1 and 2. In voltage restrained mode the effective operating current of the protection element is continuously variable as the applied voltage varies between two voltage thresholds, ***VRO>1 V1<Setting*** and ***VRO>1 V2<Setting***, as shown in the figure below.

Each of the stages can be set to HV Winding, LV Winding, TV Winding, T1, T2, T3, T4, or T5. If the current signal chosen for a VRO stage does not belong to the winding where the VT is located, then the VRO element is blocked and a configuration error alarm is asserted. The operating characteristic of the current setting when voltage restrained mode is selected is as follows:

For V > Vs1: Current setting (IS) = I>
For Vs2< V < Vs1: Current setting (IS) = K I> + (I> - K I>) {(V- Vs2) / (Vs1- Vs2)}
For V < Vs2: Current setting (IS) = K I>

Where:

I> = VRO> Curr' Set
IS = Current setting at voltage V
V = Voltage applied to relay element
Vs1 = V<1 Set
Vs2 = V<2 Set

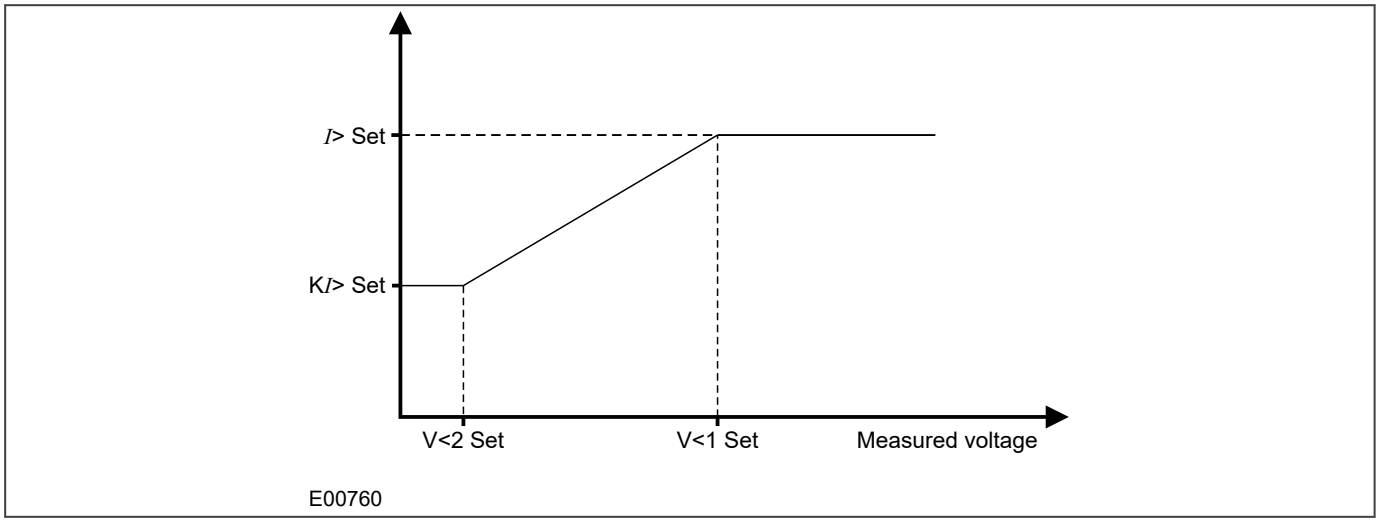


Figure 109: Modification of current pickup level for voltage restrained overcurrent protection

In P643 and P645 models, VRO requires an optional three-phase VT to be fitted, whereas, the P642 model requires that two single-phase VTs are fitted. Also, in P643 and P645 models, the phase-to-phase voltages are derived from the measured phase-to-neutral voltages. In the P642, two phase-to-phase voltages are measured and the third one is calculated. In the P642 Vab and Vbc are measured, then Vca is calculated.

This protection mode is considered to be better suited to Generator-Transformer applications.

9.5 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

When applying standard phase overcurrent protection, the overcurrent elements must be set significantly higher than the maximum load current. This limits the element's sensitivity. Most protection schemes also use an earth fault element operating from residual current, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes. Negative Phase Sequence Overcurrent elements can help in such cases.

Any unbalanced fault condition will produce a negative sequence current component. Therefore, a negative phase sequence overcurrent element can be used for both phase-to-phase and phase-to-earth faults. Negative Phase Sequence Overcurrent protection offers the following advantages:

- Negative phase sequence overcurrent elements are more sensitive to resistive phase-to-phase faults, where phase overcurrent elements may not operate.
- In certain applications, residual current may not be detected by an earth fault element due to the system configuration. For example, an earth fault element applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element may be used to provide time-delayed back-up protection for any uncleared asymmetrical faults downstream.

9.5.1 NPSOC PROTECTION IMPLEMENTATION

The product provides three overcurrent elements for backup negative phase sequence overcurrent protection. Each element provides four-stages of negative sequence overcurrent protection with independent time delay characteristics. You can select the overcurrent element operating quantity for each of the elements with the setting cells ***NPS O/C 1***, ***NPS O/C 2*** and ***NPS O/C 3*** in the *NEG SEQ O/C* column of the relevant settings group. You can set each element as `T1`, `T2`, `T3`, `T4`, `T5`, `HV winding`, `LV winding` or `TV winding`. The HV, LV and TV windings comprise the vector sums of the CT inputs associated with a particular winding.

Stages 1, 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells

- ***I2>(n) Function*** for the overcurrent operate characteristic
- ***I2>(n) Reset Char*** for the overcurrent reset characteristic (IEEE only)

where (n) is the number of the stage.

The IDMT-capable stages, (1 and 2) also provide a Timer Hold facility. This is configured using the cells ***I2>(n) tReset***, where (n) is the number of the stage. This is not applicable for curves based on the IEEE standard.

Stages 3 and 4 can have definite time characteristics only.

9.5.2 NON-DIRECTIONAL NPSOC LOGIC

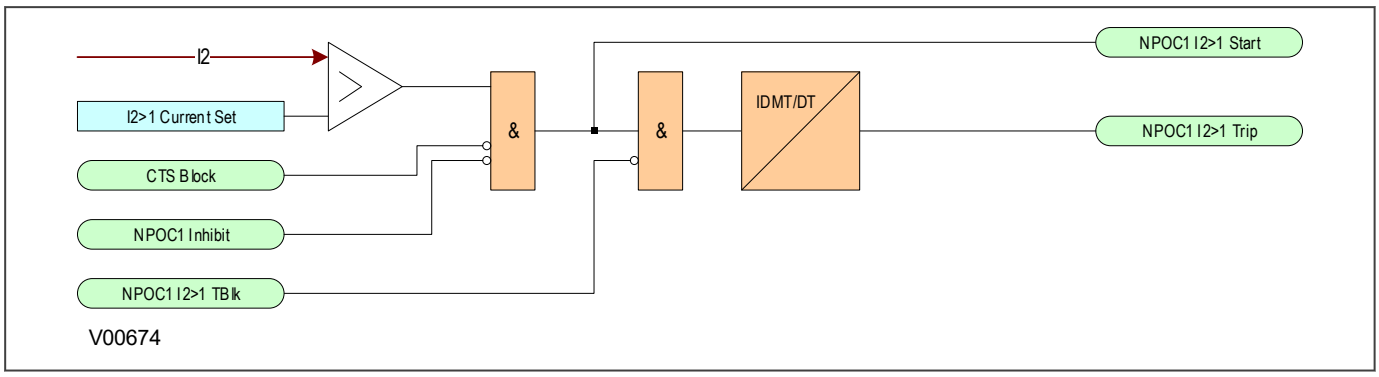


Figure 110: Negative Sequence Overcurrent logic - non-directional operation

For Negative Phase Sequence Overcurrent Protection, the energising quanitity ***I2>*** is compared with the threshold voltage ***I2>1 Current Set***. If the value exceeds this setting a start signal is generated, provided there are no blocks. 5% hysteresis is built into the comparator such that the drop-off value is 0.95 x of the current set threshold.

The function can be blocked by an Inhibit signal or by a CTS blocking signal.

The start signal is fed into a timer to produce the trip signal. The timer can be blocked by the timer block signal

This diagram and description applies to each stage of each element, where x is the number of the element and n is the number of the stage.

9.5.3 DIRECTIONAL ELEMENT

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control should be used.

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. A directional element is available for all of the negative sequence overcurrent stages. This is found in the ***I2>(n) Direction*** cell for the relevant stage for the relevant element. It can be set to non-directional, directional forward, or directional reverse.

A suitable characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (**–V2**), in order to be at the centre of the directional characteristic.

9.5.3.1 DIRECTIONAL NPSOC LOGIC

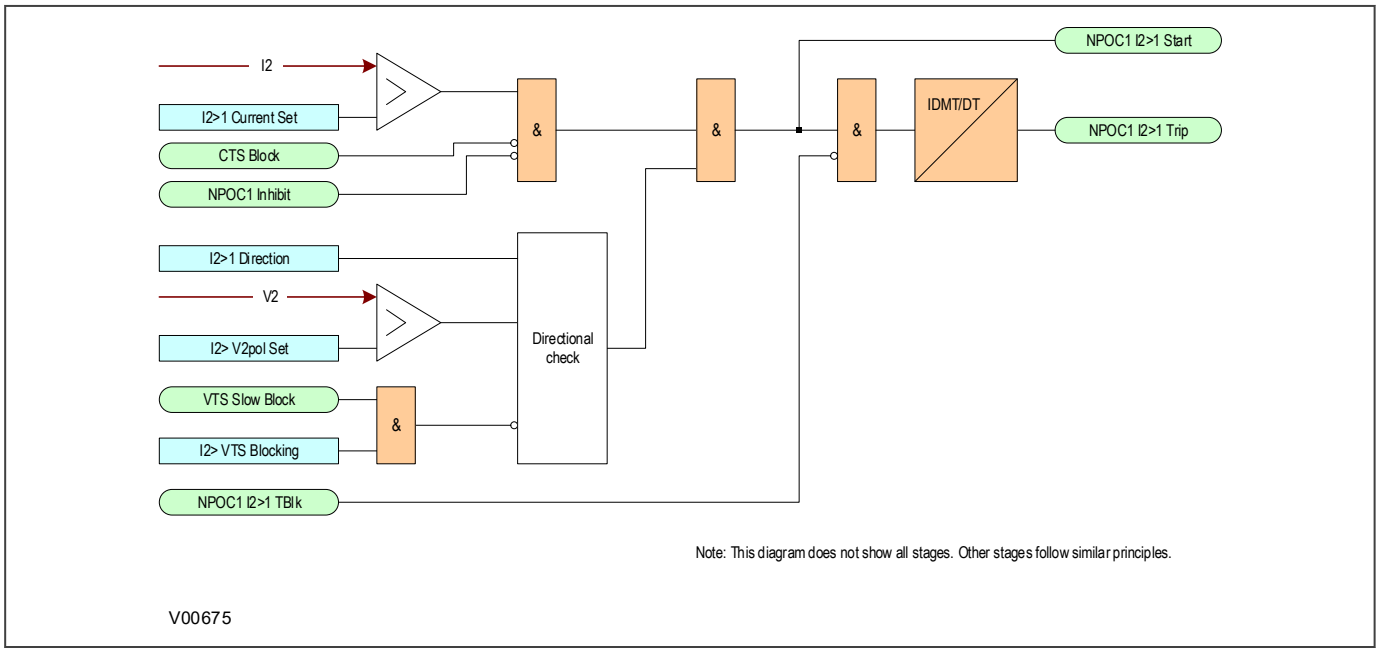


Figure 111: Negative Phase Sequence Overcurrent logic - directional operation

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current. The element may be selected to operate in either the forward or reverse direction. A suitable characteristic angle setting (***I2>Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2>V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

When the element is selected as directional (directional devices only), a VTS blocking option is available. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS) will block the stage. When set to 0, the stage will revert to non-directional.

9.5.4 APPLICATION NOTES

9.5.4.1 SETTING GUIDELINES (GENERAL)

Since the negative phase sequence overcurrent protection does not respond to balanced-load or three-phase faults, negative sequence overcurrent elements may provide the desired overcurrent protection. This is particularly applicable to Δ−Y grounded transformers where only 58% of the secondary per unit phase-to-ground fault current appears in any one primary phase conductor. Backup protection can be particularly difficult when the Y is impedance-grounded.

9.5.4.2 SETTING GUIDELINES (CURRENT THRESHOLD)

A negative phase sequence element can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-earth or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and earth elements for phase-to-earth and phase-to-phase faults.

The current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load imbalance. This can be set practically at the commissioning stage, making use of the measurement function to display the standing negative phase sequence current. The setting should be at least 20% above this figure.

Where the negative phase sequence element needs to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

9.5.4.3 SETTING GUIDELINES (TIME DELAY)

Correct setting of the time delay for this function is vital. You should also be very aware that this element is applied primarily to provide back-up protection to other protection devices or to provide an alarm. It would therefore normally have a long time delay.

The time delay set must be greater than the operating time of any other protection device (at minimum fault level) that may respond to unbalanced faults such as phase overcurrent elements and earth fault elements.

9.5.4.4 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

Where negative phase sequence current may flow in either direction through an IED location, such as parallel lines or ring main systems, directional control of the element should be employed (VT models only).

Directionality is achieved by comparing the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (***I2> Char Angle***) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), in order to be at the centre of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the relay characteristic angle (RCA) should be set equal to –60°
- For a distribution system the relay characteristic angle (RCA) should be set equal to –45°

For the negative phase sequence directional elements to operate, the device must detect a polarising voltage above a minimum threshold, ***I2> V2pol Set***. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the device.

9.6 EARTH FAULT PROTECTION

Earth faults are overcurrent faults where the fault current flows to earth. Earth faults are the most common type of fault.

Earth faults can be measured directly from the system by means of:

- A separate current Transformer (CT) located in a power system earth connection
- A residual connection of the three line CTs, where the Earth faults can be derived mathematically by summing the three measured phase currents.

Depending on the device model, it will provide one or more of the above means for Earth fault protection.

9.6.1 EARTH FAULT PROTECTION ELEMENTS

The product provides two (P642) or four (P643/P645) earth fault elements for earth fault protection backup. Each element provides four-stages of non-directional or directional three-phase overcurrent protection with independent time delay characteristics. You can select the overcurrent element operating quantity for each of the elements with the setting cells ***Earth Fault 1***, ***Earth Fault 2*** , ***Earth Fault 3*** and ***Earth Fault 4*** in the *EARTH FAULT* column of the relevant settings group. You can set each element as `T1`, `T2`, `T3`, `T4`, `T5`, `HV winding`, `LV winding` or `TV winding`.

Earth Fault 1, ***Earth Fault 2*** and ***Earth Fault 3*** can either measure the earth fault directly or derive it by summing the phase currents, ***Earth Fault 4*** (P643/P645 only) may only derive the earth fault. This depends on the settings: ***EF 1 Input***, ***EF 2 Input***, ***EF 3 Input***, which you can set to `Measured` or `Derived` and, ***EF 4 Input*** (P643/P645 only), which may only be `Derived`. For the derived element, the HV, LV and TV windings comprise the vector sums of the CT inputs associated with a particular winding. For the measured elements TN1, TN2 and TN3 are used.

Each earth fault element provides four stages of Earth Fault protection with independent time delay characteristics.

Stages 1 and 2 provide a choice of operate and reset characteristics, where you can select between:

- A range of standard IDMT (Inverse Definite Minimum Time) curves
- DT (Definite Time)

This is achieved using the cells:

- ***IN>(n) Function*** for the overcurrent operate characteristics
- ***IN>(n) Reset Char*** for the overcurrent reset characteristic (IEEE only)

where (n) is the number of the stage.

Stages 1 and 2 provide a Timer Hold facility. This is configured using the cells ***IN>(n) tReset.***

Stages 3 and 4 can have definite time characteristics only.

9.6.2 NON-DIRECTIONAL EARTH FAULT LOGIC

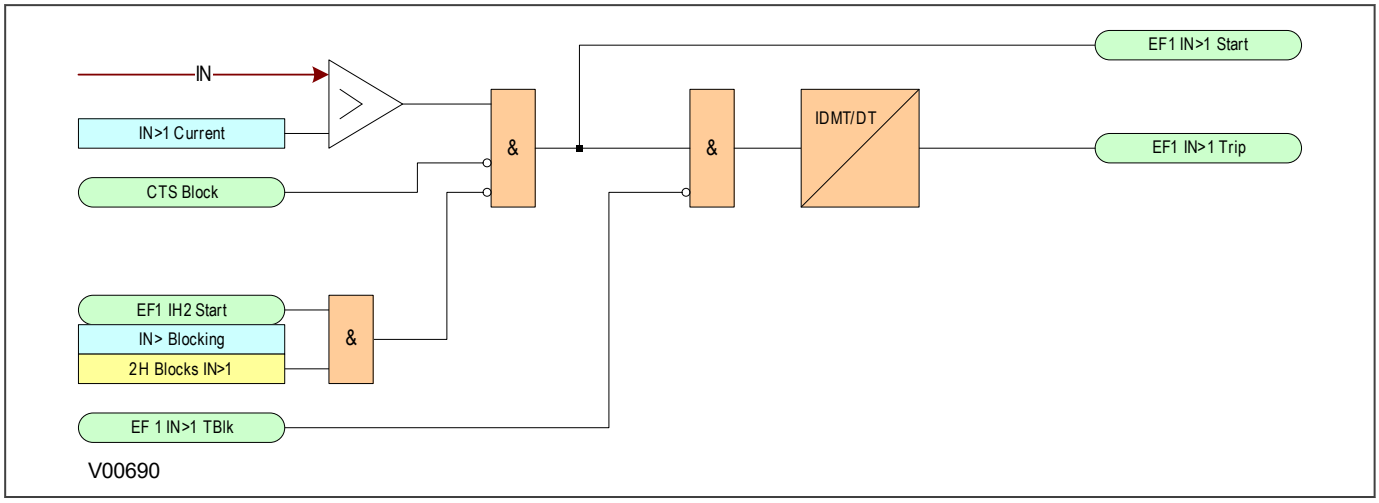


Figure 112: Non-directional EF logic (single stage)

The Earth Fault current is compared with a set threshold for each stage of each element. If it exceeds this threshold, a Start signal is triggered, providing it is not blocked. This can be blocked by the second harmonic blocking function, or an Inhibit Earth Fault DDB signal.

The timer can be blocked by the relevant timer block signal.

Earth Fault protection can follow the same IDMT characteristics as described in the Overcurrent Protection Principles section. Please refer to this section for details of IDMT characteristics.

The diagram and description applies to all stages of all earth fault elements.

9.6.3 IDG CURVE

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.

The IDG curve is represented by the following equation:

$$t_{op} = 5.8 - 1.35 log_e \left(\frac{I}{IN > Setting} \right)$$

where:

t_{op} is the operating time

I is the measured current

IN> Setting is an adjustable setting, which defines the start point of the characteristic

Note:
Although the start point of the characteristic is defined by the "IN>" setting, the actual current threshold is a different setting called "IDG Is". The "IDG Is" setting is set as a multiple of "IN>".

Note:
When using an IDG Operate characteristic, DT is always used with a value of zero for the Rest characteristic.

An additional setting "IDG Time" is also used to set the minimum operating time at high levels of fault current.

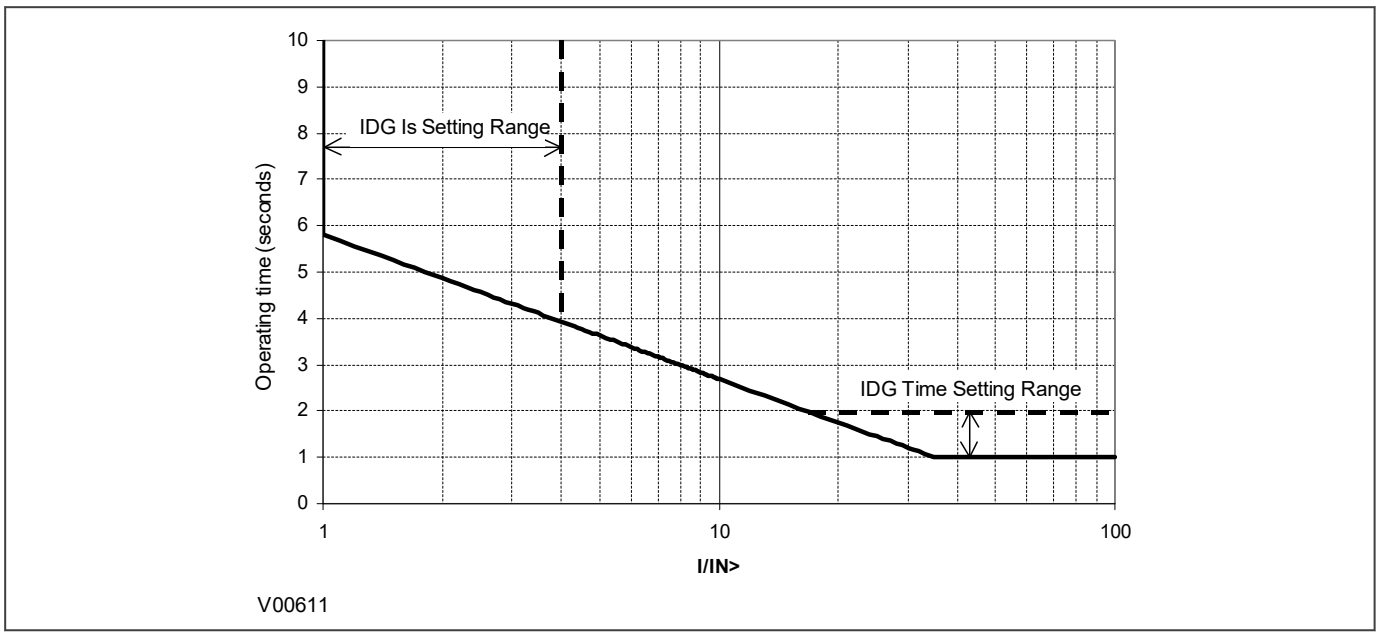


Figure 113: IDG Characteristic

9.6.4 DIRECTIONAL ELEMENT

If Earth fault current can flow in both directions through a protected location, you will need to use a directional overcurrent element to determine the direction of the fault. Typical systems that require such protection are parallel feeders (both plain and transformer) and ring main systems, each of which are relatively common in distribution networks.

A directional element is available for all of the Earth Fault stages for both Earth fault columns. These are found in the direction setting cells for the relevant stage. They can be set to non-directional, directional forward, or directional reverse.

The P642 has two neutral current inputs (TN1 and TN2). The P643 and P645 have three terminal current inputs (TN1, TN2 and TN3). The earth fault overcurrent elements can be directionalised if the TN input is associated with the winding to which the optional VT input has been connected and assigned.

For standard earth fault protection, two options are available for polarisation; Residual Voltage or Negative Sequence.

9.6.4.1 RESIDUAL VOLTAGE POLARISATION

With earth fault protection, the polarising signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarise directional earth fault elements. This is known as Zero Sequence Voltage polarisation, Residual Voltage polarisation or Neutral Displacement Voltage (NVD) polarisation.

Small levels of residual voltage could be present under normal system conditions due to system imbalances, VT inaccuracies, device tolerances etc. For this reason, the device includes a user settable threshold (***IN> VNPol set***), which must be exceeded in order for the DEF function to become operational. The residual voltage measurement provided in the *MEASUREMENTS 1* column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note:
Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the "-Vres" quantity. This 180° phase shift is automatically introduced within the device.

The directional criteria with residual voltage polarisation is given below:

- Directional forward: -90° < (angle(IN) - angle(VN + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(IN) - angle(VN + 180°) - RCA) > 90°

The device derives this voltage internally from the 3-phase voltage input tha must be supplied from either a 5-limb VT or three single-phase VTs. A three-limb VT has no path for residual flux and is therefore unsuitable to supply the device.

9.6.4.1.1 DIRECTIONAL EARTH FAULT LOGIC WITH RESIDUAL VOLTAGE POLARISATION

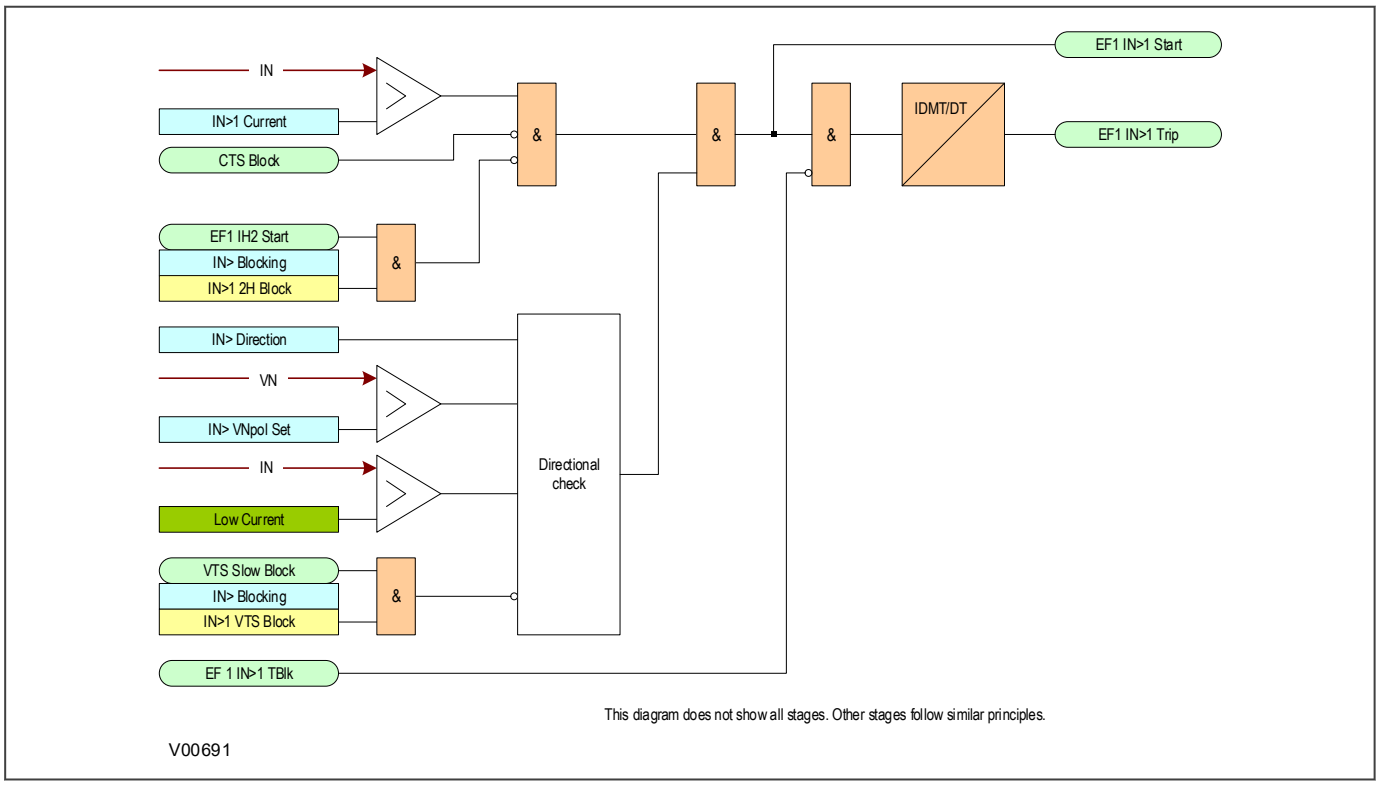


Figure 114: Directional EF logic with neutral voltage polarization (single stage)

Voltage Transformer Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the Start outputs as well.

9.6.4.2 NEGATIVE SEQUENCE POLARISATION

In some applications, the use of residual voltage polarisation may not be possible to achieve or it can be problematic. For example, a suitable type of VT may be unavailable, or an HV/EHV parallel line application may present problems with zero sequence mutual coupling.

In such situations, the problem may be solved by using Negative Phase Sequence (NPS) quantities for polarisation. This method determines the fault direction by comparing the NPS voltage with the NPS current. The operating quantity, however, is still residual current.

This can be used for both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells ***IN> V2pol set*** and ***IN> I2pol set*** respectively.

Negative phase sequence polarising is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance to negligible levels. If this voltage is less than 0.5 volts the device will stop providing directionalisation.

The directional criteria with negative sequence polarisation is given below:

- Directional forward: -90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

9.6.4.2.1 DIRECTIONAL EARTH FAULT LOGIC WITH NPS POLARISATION

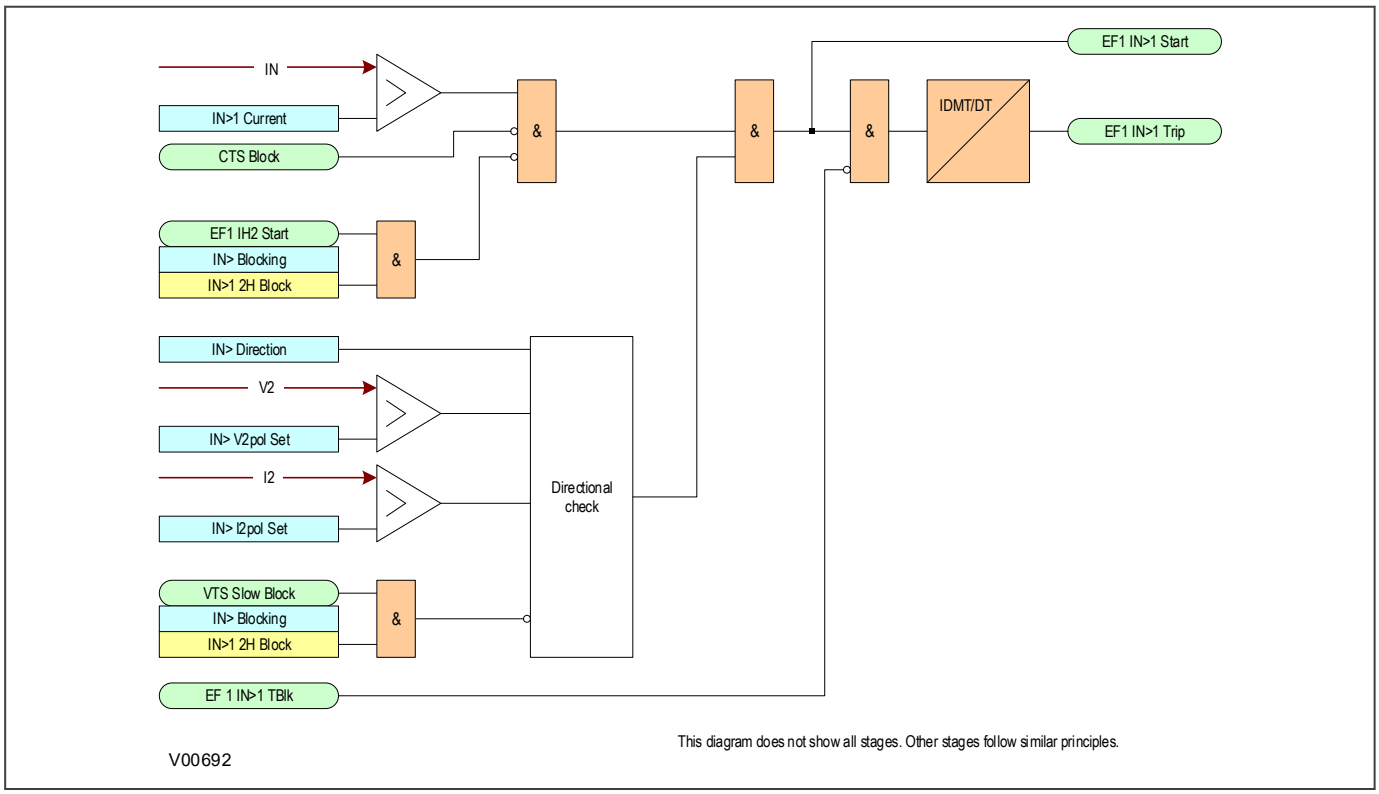


Figure 115: Directional Earth Fault logic with negative phase sequence polarisation (single stage)

Voltage Transformer Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the Start outputs as well.

The directional criteria with negative sequence polarisation is given below:

- Directional forward: -90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°
- Directional reverse : -90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

9.6.5 APPLICATION NOTES

9.6.5.1 SETTING GUIDELINES (NON-DIRECTIONAL)

To provide backup protection for downstream equipment such as the power transformer and busbar, Standby Earth Fault (SBEF) protection is commonly applied. This function is fulfilled by a separate earth fault current input, fed from a single CT in the transformer earth connection. The earth fault elements may be used to provide the SBEF function.

A Neutral Earthing Resistor (NER) is used to limit the earth fault level to a particular value. It is possible that under an earth fault condition a flashover of the NER could occur, which could lead to a dramatic increase in the earth fault current. For this reason, it may be appropriate to apply two-stage SBEF protection. The first stage should have suitable current and time characteristics which coordinate with downstream earth fault protection. The second stage

may then be set with a higher current setting but with zero time delay, providing fast clearance of an earth fault which gives rise to an NER flashover.

The remaining two stages are available for customer-specific applications.

9.6.5.2 SETTING GUIDELINES (DIRECTIONAL ELEMENT)

With directional earth faults, the residual current under fault conditions lies at an angle lagging the polarising voltage. Hence, negative RCA settings are required for DEF applications. This is set in the cell ***I> Char Angle*** in the relevant earth fault menu.

We recommend the following RCA settings:

- Resistance earthed systems: 0°
- Distribution systems (solidly earthed): -45°
- Transmission systems (solidly earthed): -60°

9.7 SECOND HARMONIC BLOCKING

9.7.1 SECOND HARMONIC BLOCKING IMPLEMENTATION

A separate second harmonic blocking function is applied to the following overcurrent protection types:

- Phase Overcurrent protection (Overcurrent 1, Overcurrent 2 and Overcurrent 3)
- Earth Fault protection elements (Earth Fault 1, Earth Fault 2 and Earth Fault 3)
- There is no second harmonic blocking for Negative Phase Sequence Overcurrent protection

Second harmonic blocking is applicable to all stages of each of the elements. For POC, 2nd harmonic blocking can be applied to each phase individually (phase segregated), or to all three phases at once (cross-block).

The function works by identifying and measuring the inrush currents present at switch on. It does this by comparing the value of the second harmonic current components to the value of the fundamental component. If this ratio exceeds the set thresholds, then the blocking signal is generated. The threshold is defined by the settings ***IH2 I> Set*** and ***IH2 IN> Set*** for Phase Overcurrent protection and Earth Fault protection respectively.

We only want the function to block the protection if the fundamental current component is within the normal range. If this exceeds the normal range, then this is indicative of a fault, which must be protected. For this reason there is another settable trigger ***IH2 IN> Unblock*** for Phase Overcurrent protection and ***IH2 I> Unblock*** for Earth fault protection, which when exceeded, stops the 2nd harmonic blocking function.

Each overcurrent protection element has an ***I>Blocking*** setting with which the stages to be blocked can be selected.

9.7.2 SECOND HARMONIC BLOCKING LOGIC

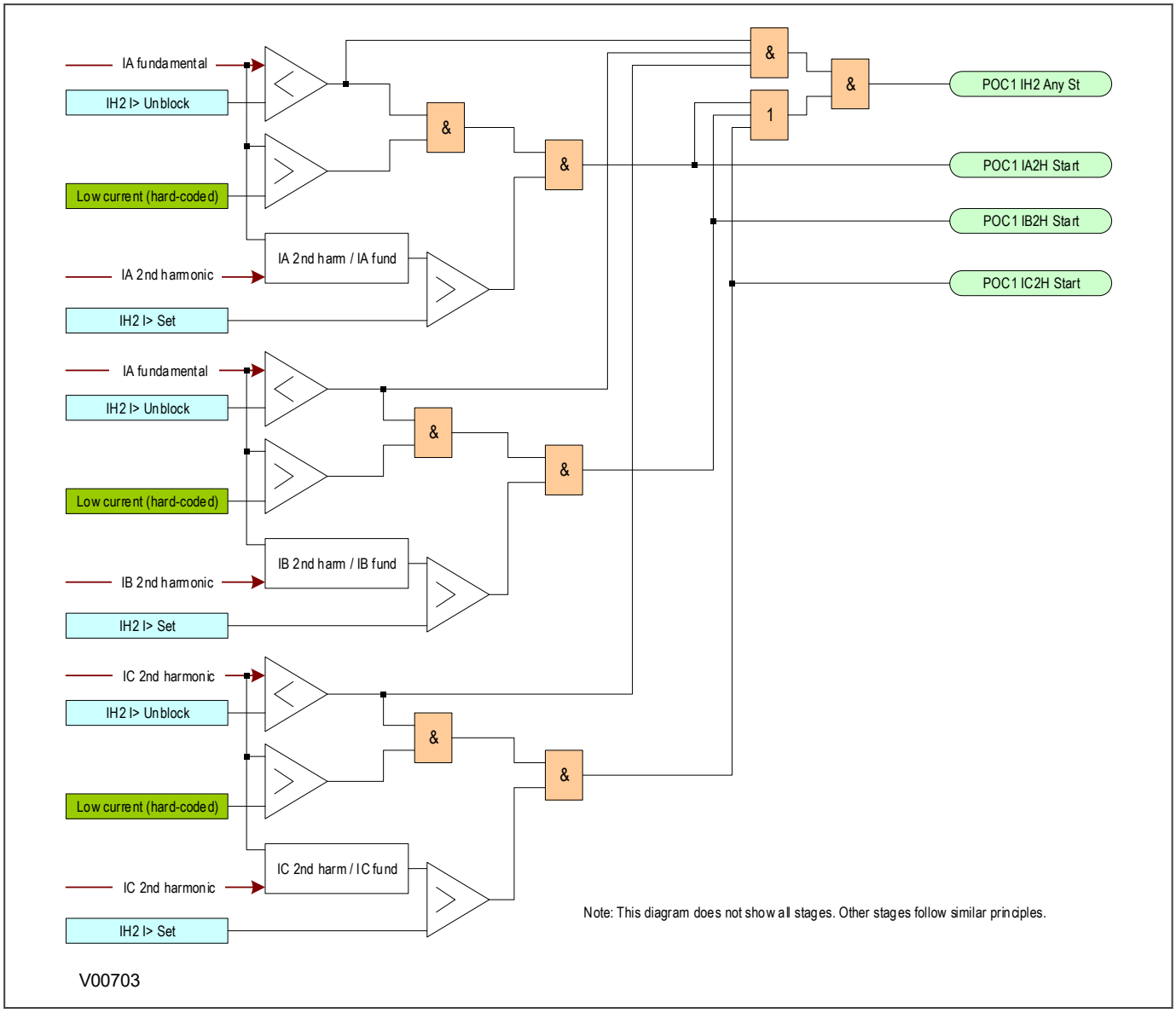


Figure 116: Phase overcurrent 2nd harmonic blocking Logic

9.7.3 EF SECOND HARMONIC BLOCKING LOGIC

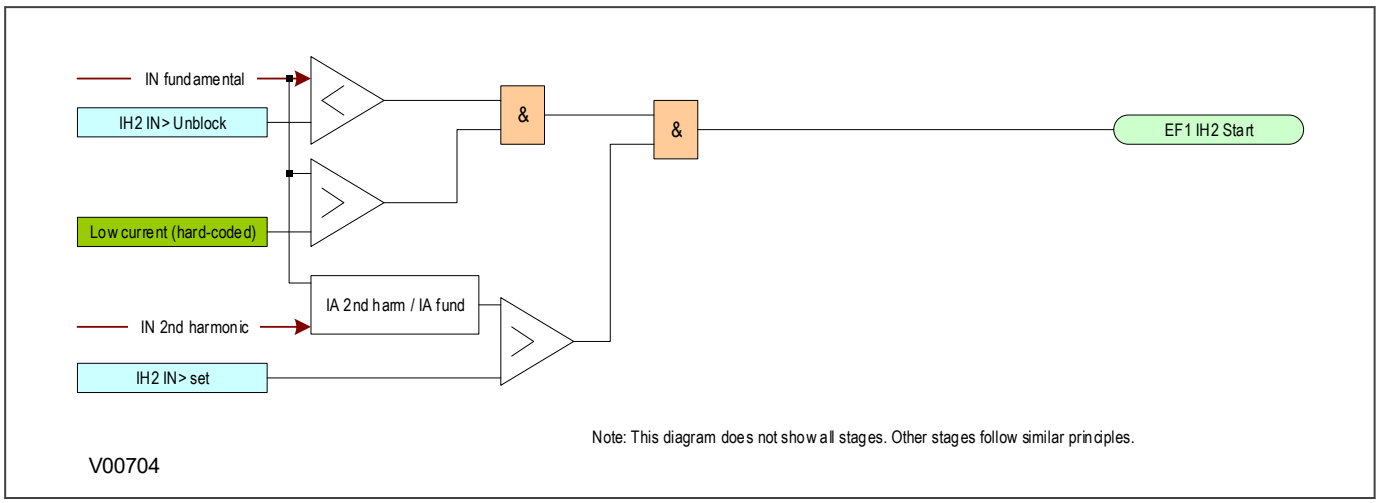


Figure 117: Earth fault 2nd harmonic blocking Logic

9.7.4 APPLICATION NOTES

9.7.4.1 SETTING GUIDELINES

During the energization period, the second harmonic component of the inrush current may be as high as 70%. The second harmonic level may be different for each phase, which is why phase segregated blocking is available.

If the setting is too low, the 2nd harmonic blocking may prevent tripping during some internal transformer faults. If the setting is too high, the blocking may not operate for low levels of inrush current which could result in undesired tripping of the overcurrent element during the energization period. In general, a setting of 15% to 20% is suitable.

CHAPTER 10

CB FAIL PROTECTION

10.1 CHAPTER OVERVIEW

The device provides a Circuit Breaker Fail Protection function. This chapter describes the operation of this function including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 238
Circuit Breaker Fail Protection 239
Circuit Breaker Fail Implementation 240
Circuit Breaker Fail Logic 242
Application Notes 244

10.2 CIRCUIT BREAKER FAIL PROTECTION

When a fault occurs, one or more protection devices will operate and issue a trip command to the relevant circuit breakers. Operation of the circuit breaker is essential to isolate the fault and prevent, or at least limit, damage to the power system. For transmission and sub-transmission systems, slow fault clearance can also threaten system stability.

For these reasons, it is common practice to install Circuit Breaker Failure protection (CBF). CBF protection monitors the circuit breaker and establishes whether it has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, the CBF protection will operate, whereby the upstream circuit breakers are back-tripped to ensure that the fault is isolated.

CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

10.3 CIRCUIT BREAKER FAIL IMPLEMENTATION

Depending on the P64 model (P642, P643, P645), up to five independent sets of circuit breaker failure settings are available, supporting one phase current and one earth undercurrent function for each set. Each CB Failure set can be enabled or disabled by the settings ***T1 CBF Status***, ***T2 CBF Status***, ***T3 CBF Status***, ***T4 CBF Status*** and ***T5 CBF Status*** respectively.

You can enable or disable each Earth undercurrent element with the ***IN< Status*** setting. If enabled, you can set each earth undercurrent element as measured or derived using the ***IN< Input*** setting. When enabled, it can be set as measured or derived. Depending on the model, you can use single phase CTs connected to the three neutral CT connections TN1, TN2 and TN3 for CB failure function (see wiring diagram). You define this with the ***IN< Terminal*** setting.

10.3.1 CIRCUIT BREAKER FAIL TIMERS

The circuit breaker failure protection incorporates two timers, ***CB Fail 1 Timer*** and ***CB Fail 2 Timer***, allowing configuration for the following scenarios:

- Simple CBF, where only ***CB Fail 1 Timer*** is enabled. For any protection trip, the **CB Fail 1** ***Timer*** is started, and normally reset when the circuit breaker opens to isolate the fault. If breaker opening is not detected, the CB Fail 1 Timer times out and closes an output contact assigned to breaker fail (using the programmable scheme logic). This contact is used to back-trip upstream switchgear, generally tripping all infeeds connected to the same busbar section.
- A retripping scheme, plus delayed back-tripping. Here, ***CB Fail 1 Timer*** is used to issue a trip command to a second trip circuit of the same circuit breaker. This requires the circuit breaker to have duplicate circuit breaker trip coils. This mechanism is known as retripping. If retripping fails to open the circuit breaker, a back-trip may be issued following an additional time delay. The back-trip uses ***CB Fail 2 Timer***, which was also started at the instant of the initial protection element trip.

You can configure the CBF elements ***CB Fail 1 Timer*** and ***CBF Fail 2 Timer*** to operate for trips triggered by protection elements within the device. Alternatively you can use an external protection trip by allocating one of the opto-inputs to the ***External Trip*** DDB signal in the PSL.

You can reset the CBF from a breaker open indication (from the pole dead logic) or from a protection reset. In these cases resetting is only allowed if the undercurrent elements have also been reset. The resetting mechanism is determined by the settings ***NonIProt Rst*** and ***Ext Prot Rst***.

The resetting options are summarised in the following table:

Initiation (Menu Selectable)	CB Fail Timer Reset Mechanism
Current based protection (e.g.50/51/46/21/87)	IA< operates AND IB< operates AND IC< operates AND IN< operates or through Ext Rst DDB in PSL
Sensitive Earth Fault element	ISEF< Operates or Ext Rst SEF DDB
Non-current based protection (e.g. 27/59/81/32L)	Three options are available: All I< and IN< elements operate or Ext Rst CBF DDB Protection element reset AND (all I< and IN< elements operate or Ext Rst DDB CB open (all 3 poles) AND all I< and IN< elements operate
External protection	Three options are available. All I< and IN< elements operate External trip reset AND all I< and IN< elements operate CB open (all 3 poles) AND all I< and IN< elements operate

10.3.2 ZERO CROSSING DETECTION

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is to its saturation point, the higher the subsidence current.

The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the protection clears the fault, the CB Fail function should reset fast to avoid maloperation due to the subsidence current. To compensate for this the device includes a zero-crossing detection algorithm, which ensures that the CB Fail re-trip and back-trip signals are not asserted while subsidence current is flowing. If all the samples within half a cycle are greater than or smaller than 0 A (10 mS for a 50 Hz system), then zero crossing detection is asserted, thereby blocking the operation of the CB Fail function. The zero-crossing detection algorithm is used after the circuit breaker in the primary system has opened ensuring that the only current flowing in the AC secondary circuit is the subsidence current.

This zero-crossing detection algorithm considers the current inputs T1, T2, T3, T4 and T5 on a per phase basis. If ***IN< Input*** is set as `measured`, the zero crossing detection algorithm considers the current inputs TN1, TN2 and TN3. If ***IN< Input*** is set as `derived`, the zero crossing detection algorithm considers the current inputs T1, T2, T3, T4 and T5. If more than 12 consecutive samples are greater than 0A or more than 12 consecutive samples are smaller than 0A, then a zero crossing detection condition is asserted, which blocks the operation of the circuit breaker failure function. The zero crossing detection is asserted after the breaker in the primary system has opened to ensure that the current flowing in the AC secondary circuit is just the subsidence current.

10.4 CIRCUIT BREAKER FAIL LOGIC

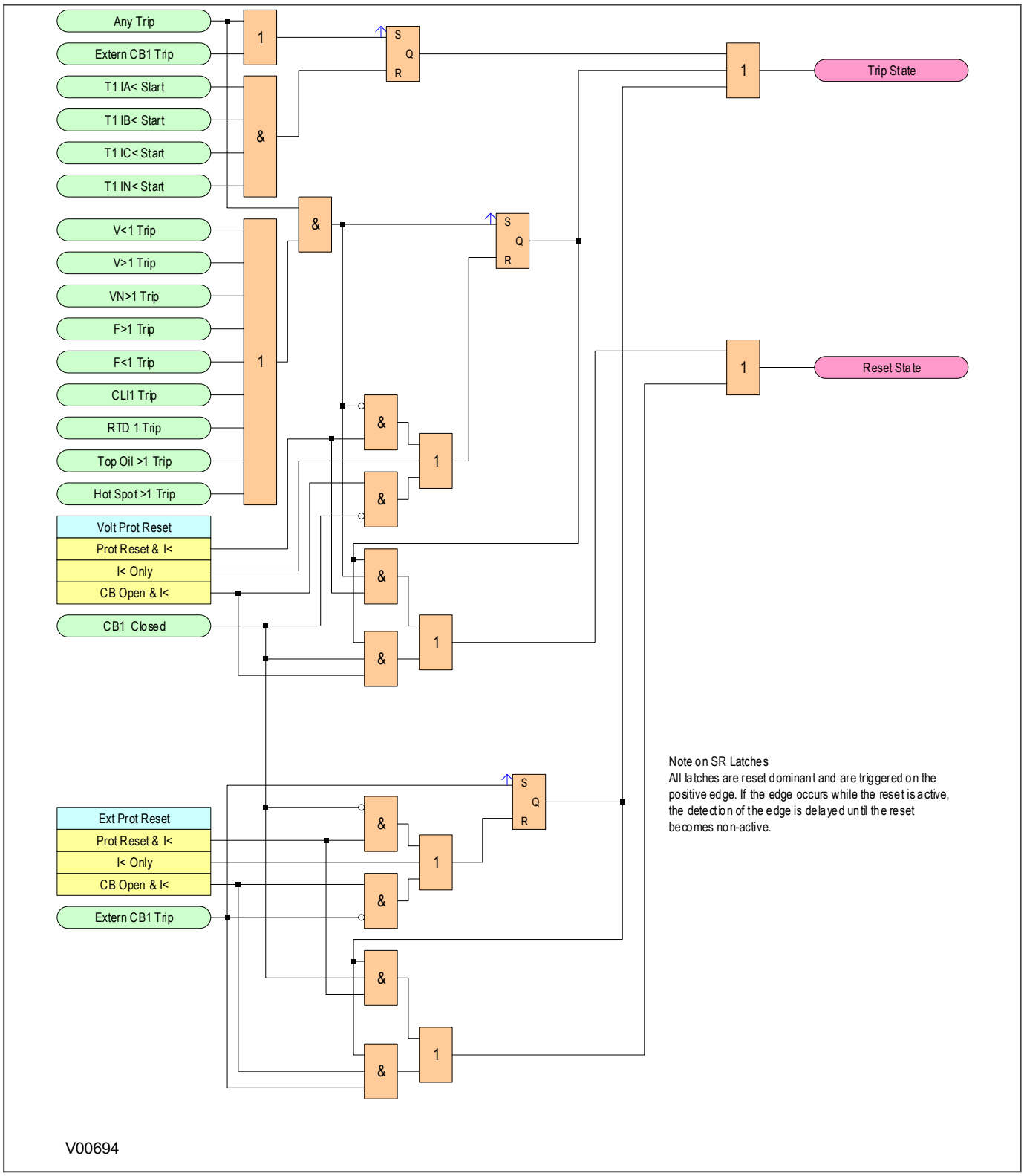


Figure 118: Circuit Breaker Fail Logic - part 1

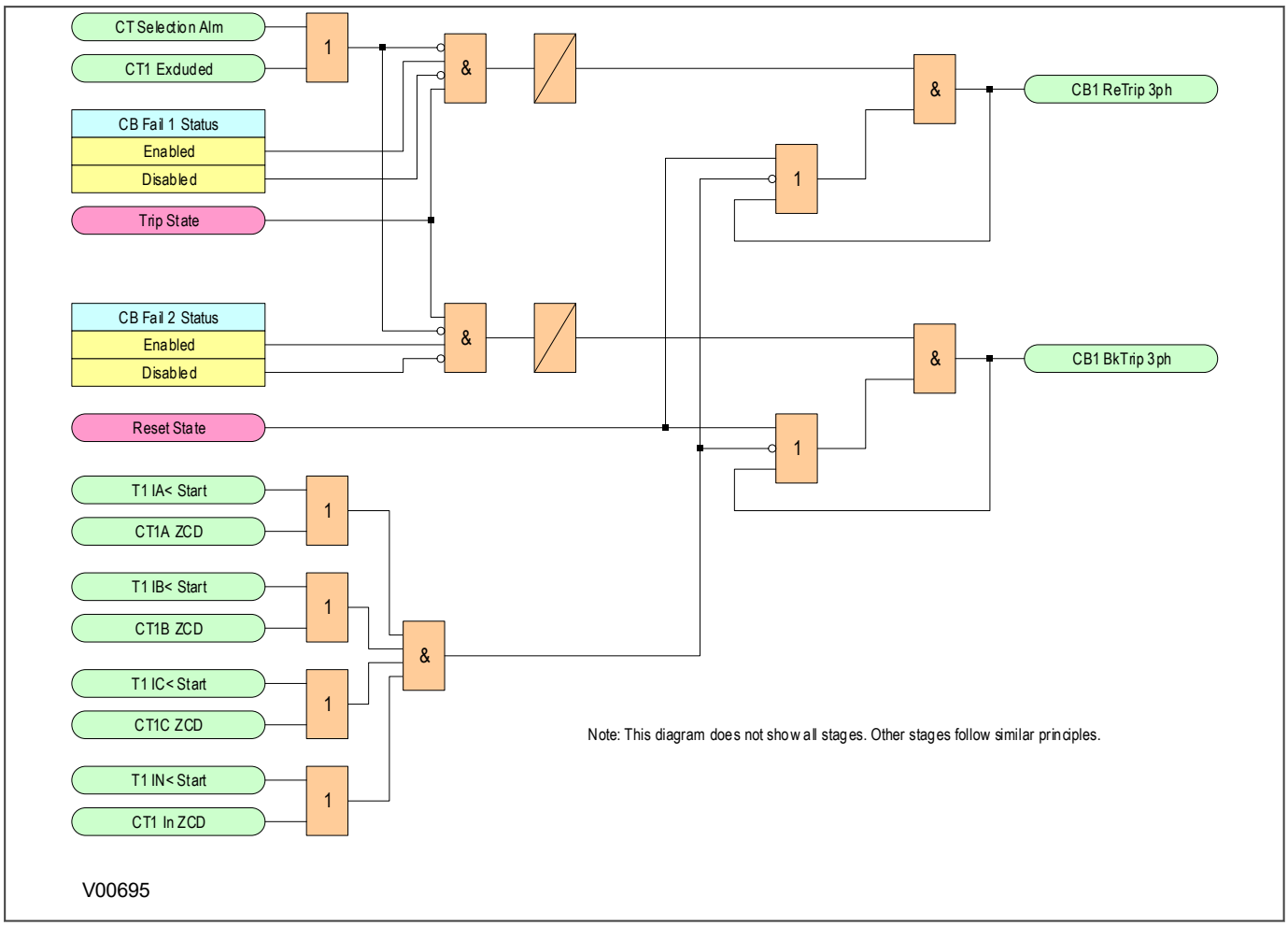


Figure 119: Circuit Breaker Fail Logic - part 2

10.5 APPLICATION NOTES

10.5.1 RESET MECHANISMS FOR CB FAIL TIMERS

It is common practise to use low set undercurrent elements to indicate that circuit breaker poles have interrupted the fault or load current. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore, reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the device uses operation of undercurrent elements to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting CBF in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. In this case, detecting drop-off of the initiating protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, and so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

10.5.2 SETTING GUIDELINES (CB FAIL TIMER)

The following timing chart shows the CB Fail timing during normal and CB Fail operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CB Fail back-up trip time delay considers the maximum CB clearing time, the CB Fail reset time plus a safety margin. Typical CB clearing times are 1.5 or 3 cycles. The CB Fail reset time should be short enough to avoid CB Fail back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CB Fail to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit.

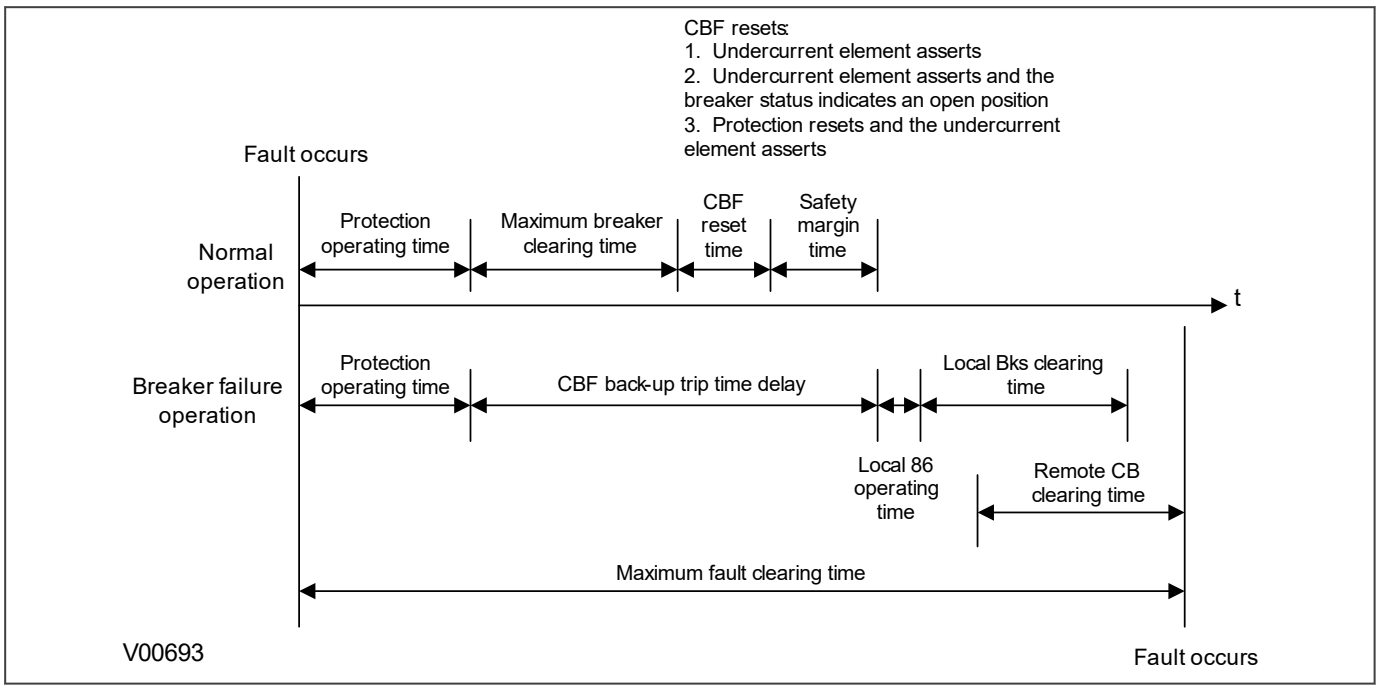


Figure 120: CB Fail timing

The following examples consider direct tripping of a 2-cycle circuit breaker. Typical timer settings to use are as follows:

CB Fail Reset Mechanism	tBF Time Delay	Typical Delay For 2 Cycle Circuit Breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Note:
All CB Fail resetting involves the operation of the undercurrent elements. Where element resetting or CB open resetting is used, the undercurrent time setting should still be used if this proves to be the worst case.
Where auxiliary tripping relays are used, an additional 10-15 ms must be added to allow for trip relay operation.

10.5.3 SETTING GUIDELINES (UNDERCURRENT)

The phase undercurrent settings (I<) must be set less than load current to ensure that I< operation correctly indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20%In. Settings of 5% of In are common for generator CB Fail.

The earth fault undercurrent elements must be set less than the respective trip. For example:

$$IN< = (IN> \text{ trip})/2$$

CHAPTER 11

VOLTAGE PROTECTION FUNCTIONS

11.1 CHAPTER OVERVIEW

The device provides a wide range of voltage protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 248
Undervoltage Protection 249
Overvoltage Protection 252
Residual Overvoltage Protection 255
Negative Sequence Overvoltage Protection 259

11.2 UNDERVOLTAGE PROTECTION

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Undervoltage conditions can be related to increased loads, whereby the supply voltage will decrease in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an undervoltage condition, which must be cleared.
- If the regulating equipment is unsuccessful in restoring healthy system voltage, then tripping by means of an undervoltage element is required.
- Faults occurring on the power system result in a reduction in voltage of the faulty phases. The proportion by which the voltage decreases is dependant on the type of fault, method of system earthing and its location. Consequently, co-ordination with other voltage and current-based protection devices is essential in order to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be necessary to isolate each of the outgoing circuits, such that when supply voltage is restored, the load is not connected. Therefore, the automatic tripping of a feeder on detection of complete loss of voltage may be required. This can be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions that last longer than a pre-determined time.

11.2.1 UNDERVOLTAGE PROTECTION IMPLEMENTATION

Undervoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Undervoltage parameters are contained within the sub-heading *UNDERVOLTAGE*.

The product provides two stages of Undervoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V<1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M-1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage / IED setting voltage (***V<(n) Voltage Set***)

The undervoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V< Measur't Mode*** cell.

There is no Timer Hold facility for Undervoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V<2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V< Operate Mode*** cell for each stage.

11.2.2 UNDERVOLTAGE PROTECTION LOGIC

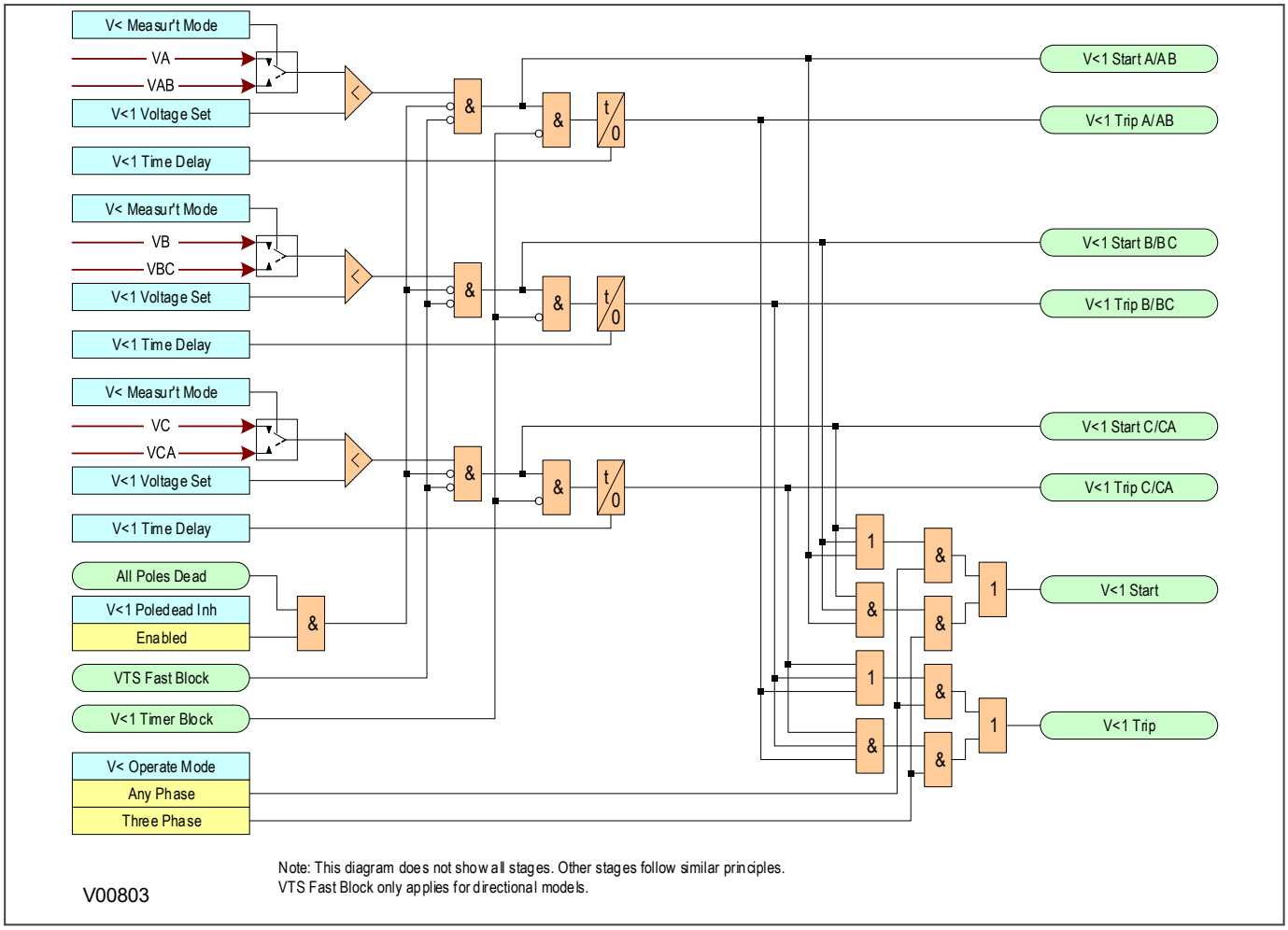


Figure 121: Undervoltage - single and three phase tripping mode (single stage)

The Undervoltage protection function detects when the voltage magnitude for a certain stage falls short of a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal and an ***All Poles Dead*** signal. This ***Start*** signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the undervoltage timer block signal (***V<(n) Timer Block***). For each stage, there are three Phase undervoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V<(n) Start***), which can be be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V< Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V< Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

In some cases, we do not want the undervoltage element to trip; for example, when the protected feeder is de-energised, or the circuit breaker is opened, an undervoltage condition would obviously be detected, but we would not want to start protection. To cater for this, an ***All Poles Dead*** signal blocks the ***Start*** signal for each phase. This is controlled by the ***V<Poledead Inh*** cell, which is included for each of the stages. If the cell is enabled, the relevant stage will be blocked by the integrated pole dead logic. This logic produces an output when it detects either an open

circuit breaker via auxiliary contacts feeding the opto-inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

11.2.3 APPLICATION NOTES

11.2.3.1 UNDERVOLTAGE SETTING GUIDELINES

In most applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case you should select phase-to-phase voltage measurement, as this quantity is less affected by single-phase voltage dips due to earth faults.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependant on the system in question but typical healthy system voltage excursions may be in the order of 10% of nominal value.

The same applies to the time setting. The required time delay is dependant on the time for which the system is able to withstand a reduced voltage.

If motor loads are connected, then a typical time setting may be in the order of 0.5 seconds.

Stage 1 is used for tripping and can be disabled, or selected as IDMT or DT. You can set stage 2 as an alarm stage to warn the user of unusual voltage conditions.

If only a single-phase VT signal is available and you require an undervoltage alarm, you must set the ***VTS status*** signal in the *SUPERVISION* column to `Indication` or `disabled`.

11.3 OVERVOLTAGE PROTECTION

Overvoltage conditions are generally related to loss of load conditions, whereby the supply voltage increases in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs (Auto Voltage Regulators) or On Load Tap Changers. However, failure of this equipment to bring the system voltage back within permitted limits leaves the system with an overvoltage condition which must be cleared.

Note:
During earth fault conditions on a power system there may be an increase in the healthy phase voltages. Ideally, the system should be designed to withstand such overvoltages for a defined period of time.

11.3.1 OVERVOLTAGE PROTECTION IMPLEMENTATION

Overvoltage Protection is implemented in the *VOLT PROTECTION* column of the relevant settings group. The Overvoltage parameters are contained within the sub-heading *OVERVOLTAGE*.

The product provides two stages of overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

You set this using the ***V>1 Function*** setting.

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K = Time multiplier setting
- t = Operating time in seconds
- M = Measured voltage setting voltage (***V>(n) Voltage Set***)

The overvoltage stages can be configured either as phase-to-neutral or phase-to-phase voltages in the ***V> Measur't Mode*** cell.

There is no Timer Hold facility for Overvoltage.

Stage 2 can have definite time characteristics only. This is set in the ***V>2 Status*** cell.

Outputs are available for single or three-phase conditions via the ***V> Operate Mode*** cell for each stage.

11.3.2 OVERVOLTAGE PROTECTION LOGIC

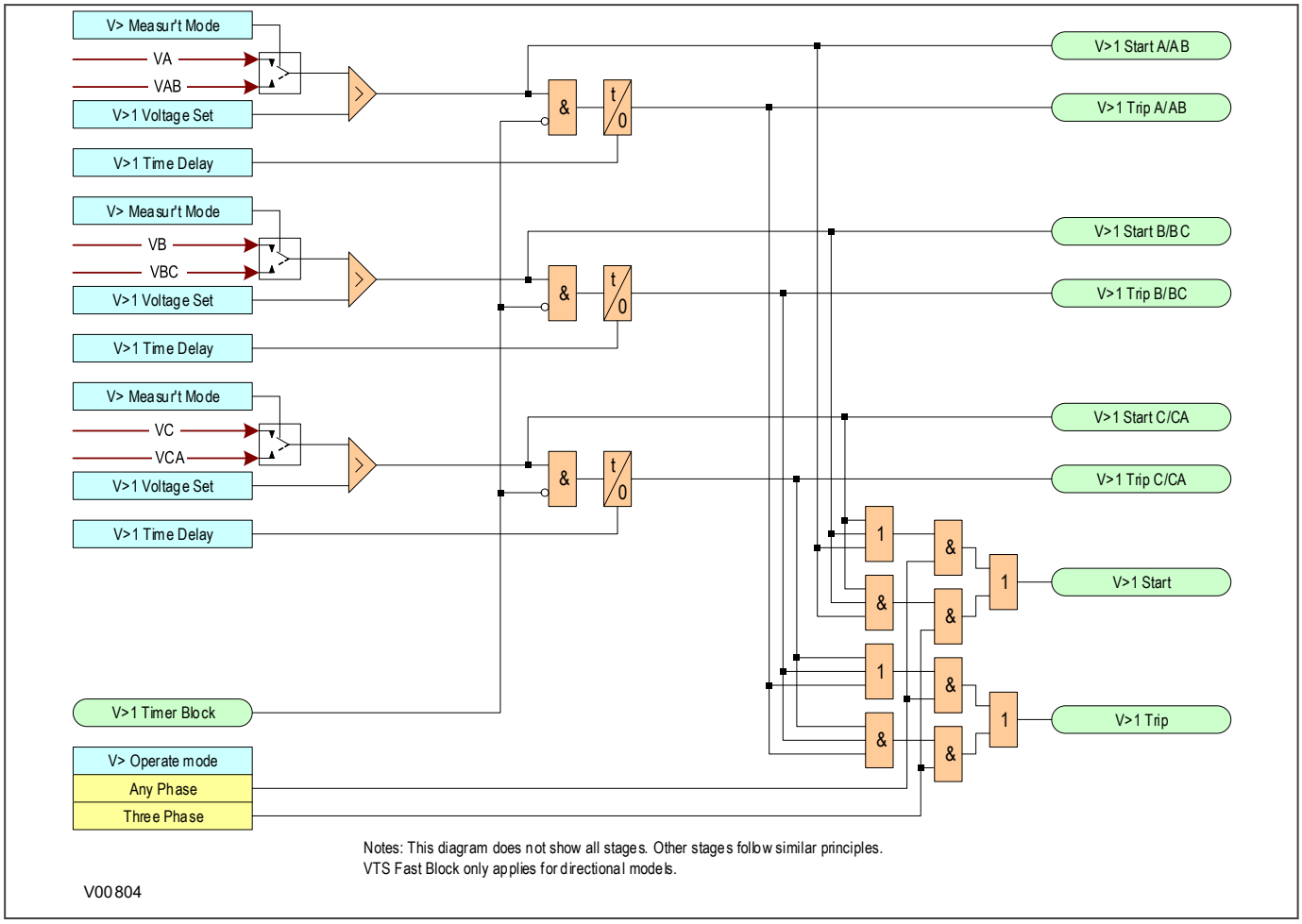


Figure 122: Overvoltage - single and three phase tripping mode (single stage)

The Overvoltage protection function detects when the voltage magnitude for a certain stage exceeds a set threshold. If this happens a ***Start*** signal, signifying the "Start of protection", is produced. This Start signal can be blocked by the ***VTS Fast Block*** signal. This start signal is applied to the timer module to produce the ***Trip*** signal, which can be blocked by the overvoltage timer block signal (***V>(n) Timer Block***). For each stage, there are three Phase overvoltage detection modules, one for each phase. The three ***Start*** signals from each of these phases are OR'd together to create a 3-phase Start signal (***V>(n) Start***), which can then be activated when any of the three phases start (Any Phase), or when all three phases start (Three Phase), depending on the chosen ***V> Operate Mode*** setting.

The outputs of the timer modules are the trip signals which are used to drive the tripping output relay. These tripping signals are also OR'd together to create a 3-phase Trip signal, which are also controlled by the ***V> Operate Mode*** setting.

If any one of the above signals is low, or goes low before the timer has counted out, the timer module is inhibited (effectively reset) until the blocking signal goes high.

11.3.3 APPLICATION NOTES

11.3.3.1 OVERVOLTAGE SETTING GUIDELINES

The provision of multiple stages and their respective operating characteristics allows for a number of possible applications:

- Definite Time can be used for both stages to provide the required alarm and trip stages.
- Use of the IDMT characteristic allows grading of the time delay according to the severity of the overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time-delayed alarm stage.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled.

This type of protection must be co-ordinated with any other overvoltage devices at other locations on the system.

Transformers can typically withstand a 110% overvoltage condition continuously. The withstand times for higher overvoltages should be declared by the transformer manufacturer.

To prevent operation during earth faults, the element should operate from the phase-phase voltages. To achieve this, you set ***V>1 Measur't Mode*** to *Phase-Phase* and ***V>1 Operating Mode*** set to *Three-phase*. You should typically set the overvoltage threshold ***V>1 Voltage Set*** to 100% - 120% of the nominal phase-phase voltage. You should also set the time delay to prevent unwanted tripping of the delayed overvoltage protection function due to transient over voltages, which do not pose a risk to the transformer. A typical delay setting would be 1 s - 3 s, with a longer delay being applied for lower voltage threshold settings.

The second stage can be used to provide instantaneous high-set over voltage protection. The typical threshold setting to be applied, ***V>2 Voltage Set***, would typically be 130 - 150% of the nominal phase-phase voltage. For instantaneous operation, you should set the time delay to 0 s.

If you select phase-to-neutral operation, take care to ensure that the element will grade with other protections during earth faults, where the phase-neutral voltage can rise significantly.

This type of protection must be coordinated with any other overvoltage devices at other locations on the system.

11.4 RESIDUAL OVERVOLTAGE PROTECTION

On a healthy three-phase power system, the sum of the three-phase to earth voltages is nominally zero, as it is the vector sum of three balanced vectors displaced from each other by 120°. However, when an earth fault occurs on the primary system, this balance is upset and a residual voltage is produced. This condition causes a rise in the neutral voltage with respect to earth. Consequently this type of protection is also commonly referred to as 'Neutral Voltage Displacement' or NVD for short.

This residual voltage is derived (from the phase voltages). Derived values are used where the model does not support measured functionality.

This offers an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balanced current transformers on each feeder may be either impractical, or uneconomic, or for providing earth fault protection for devices with no current transformers.

11.4.1 RESIDUAL OVERVOLTAGE PROTECTION IMPLEMENTATION

Residual Overvoltage Protection is implemented in the *RESIDUAL O/V NVD* column of the relevant settings group.

Some applications require more than one stage. For example an insulated system may require an alarm stage and a trip stage. It is common in such a case for the system to be designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The product provides two stages of Derived Residual Overvoltage protection with independent time delay characteristics.

Stage 1 provides a choice of operate characteristics, where you can select between:

- An IDMT characteristic
- DT (Definite Time)

The IDMT characteristic is defined by the following formula:

$$t = K/(M - 1)$$

where:

- K= Time multiplier setting
- t = Operating time in seconds
- M = Derived residual voltage setting voltage (***VN> Voltage Set***)

You set this using the ***VN>1 Function*** setting.

Stage 1 also provides a Timer Hold facility.

Stage 2 can have definite time characteristics only. This is set in the ***VN>2 status*** cell

The device derives the residual voltage internally from the three-phase voltage inputs supplied from either a 5-limb VT or three single-phase VTs. These types of VT design provide a path for the residual flux and consequently permit the device to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. Three-limb VTs have no path for residual flux and are therefore unsuitable for this type of protection.

11.4.2 RESIDUAL OVERVOLTAGE LOGIC

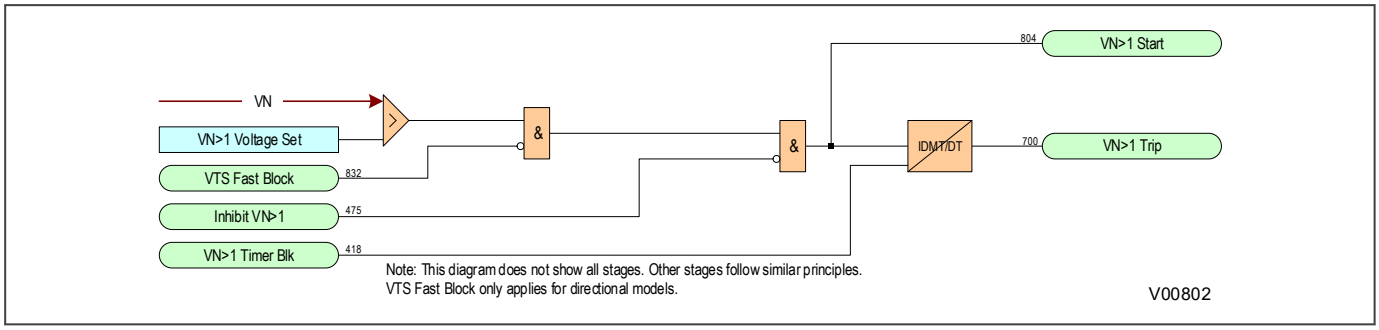


Figure 123: Residual Overvoltage logic

The Residual Overvoltage module (VN>) is a level detector that detects when the voltage magnitude exceeds a set threshold, for each stage. When this happens, the comparator output produces a ***Start*** signal (***VN>(n) Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the timer module. The output of the timer module is the ***VN> (n) Trip*** signal which is used to drive the tripping output relay.

11.4.3 APPLICATION NOTES

11.4.3.1 CALCULATION FOR SOLIDLY EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

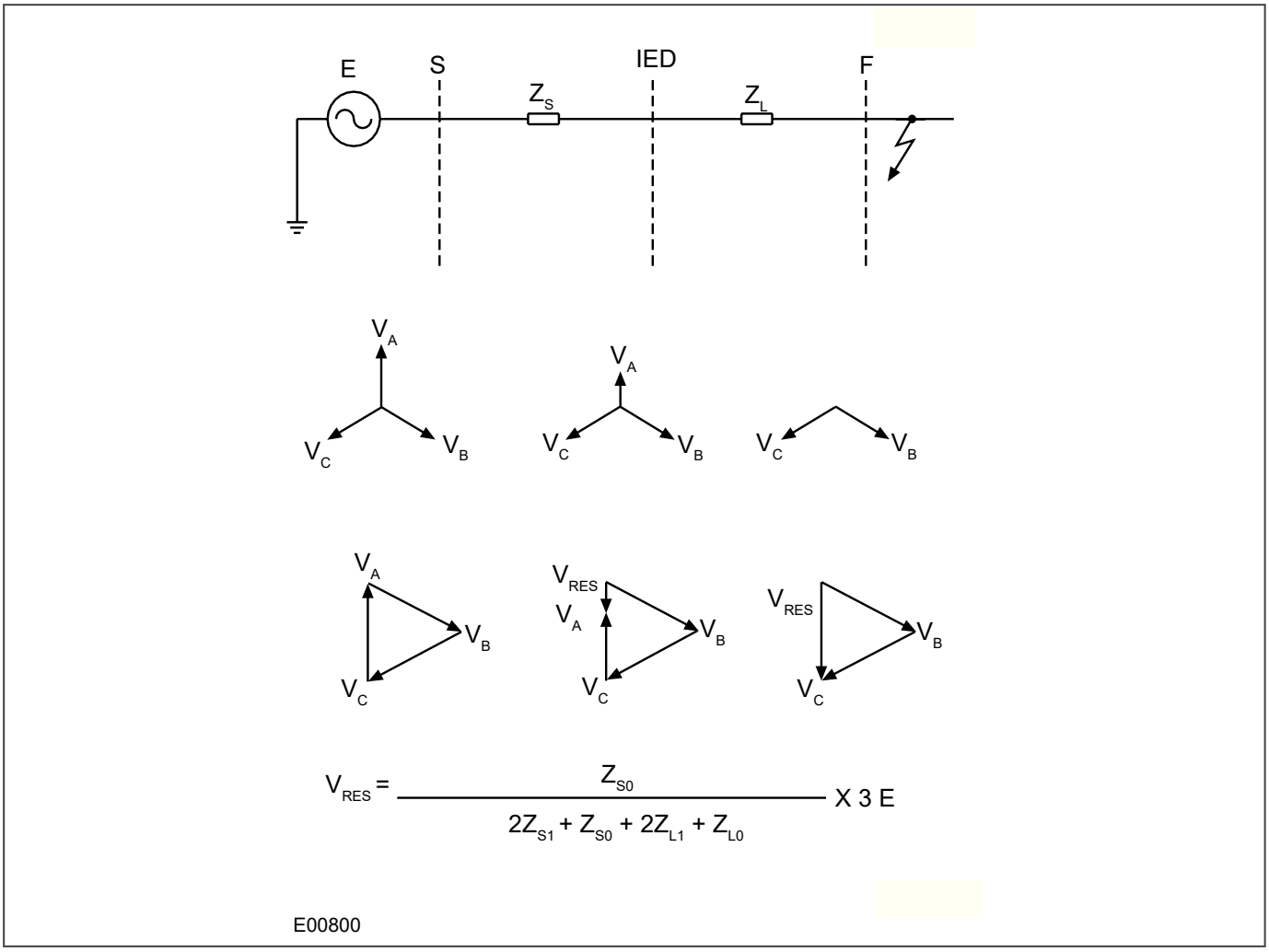


Figure 124: Residual voltage for a solidly earthed system

As can be seen from the above diagram, the residual voltage measured on a solidly earthed system is solely dependant on the ratio of source impedance behind the protection to the line impedance in front of the protection, up to the point of fault. For a remote fault far away, the Z_S/Z_L: ratio will be small, resulting in a correspondingly small residual voltage. Therefore, the protection only operates for faults up to a certain distance along the system. The maximum distance depends on the device setting.

11.4.3.2 CALCULATION FOR IMPEDANCE EARTHED SYSTEMS

Consider a Phase-A to Earth fault on a simple radial system.

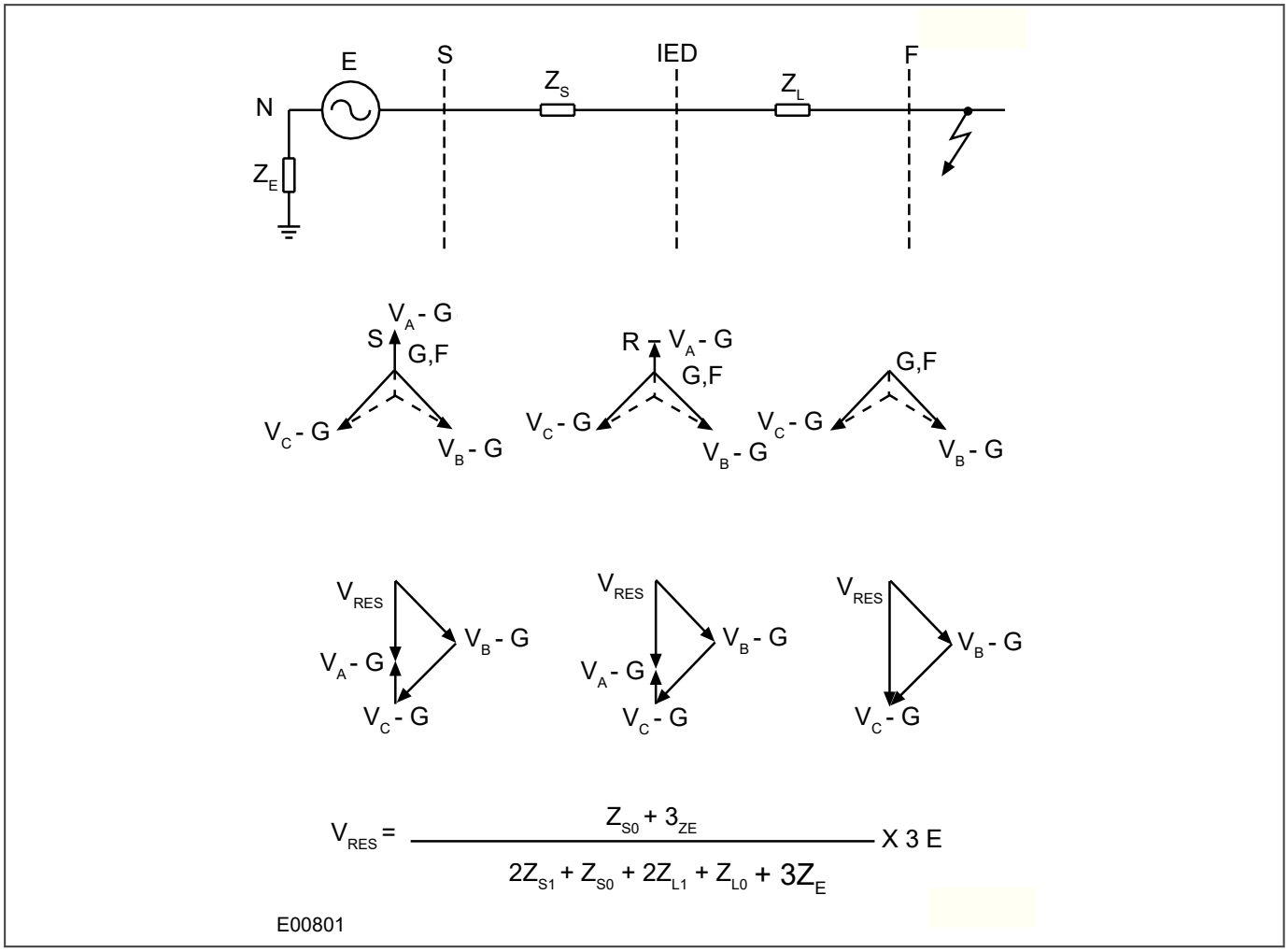


Figure 125: Residual voltage for an impedance earthed system

An impedance earthed system will always generate a relatively large degree of residual voltage, as the zero sequence source impedance now includes the earthing impedance. It follows then that the residual voltage generated by an earth fault on an insulated system will be the highest possible value (3 x phase-neutral voltage), as the zero sequence source impedance is infinite.

11.4.3.3 SETTING GUIDELINES

The voltage setting applied to the elements is dependant on the magnitude of residual voltage that is expected to occur during the earth fault condition. This in turn is dependant on the method of system earthing employed.

Also, you must ensure that the protection setting is set above any standing level of residual voltage that is present on the system.

11.5 NEGATIVE SEQUENCE OVERVOLTAGE PROTECTION

Where an incoming feeder is supplying rotating plant equipment such as an induction motor, correct phasing and balance of the supply is essential. Incorrect phase rotation will result in connected motors rotating in the wrong direction. For directionally sensitive applications, such as elevators and conveyor belts, it is unacceptable to allow this to happen.

Imbalances on the incoming supply cause negative phase sequence voltage components. In the event of incorrect phase rotation, the supply voltage would effectively consist of 100% negative phase sequence voltage only.

11.5.1 NEGATIVE SEQUENCE OVERVOLTAGE IMPLEMENTATION

Negative Sequence Overvoltage Protection is implemented in the *NEG SEQUENCE O/V* column of the relevant settings group.

The device includes one Negative Phase Sequence Overvoltage element with a single stage. Only Definite time is possible.

This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer) and may be interlocked with the motor contactor or circuit breaker to prevent the motor from being energised whilst incorrect phase rotation exists.

The element is enabled using the ***V2> status*** cell.

11.5.2 NEGATIVE SEQUENCE OVERVOLTAGE LOGIC

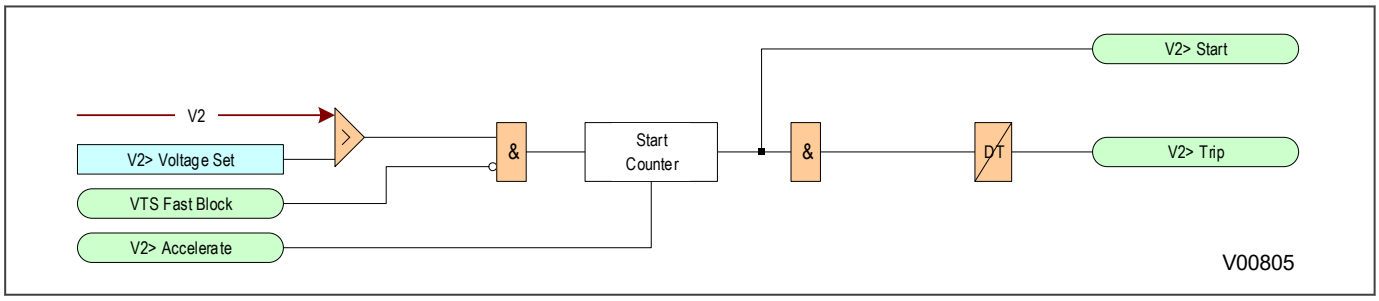


Figure 126: Negative Sequence Overvoltage logic

The Negative Voltage Sequence Overvoltage module (***V2>***) is a level detector that detects when the voltage magnitude exceeds a set threshold. When this happens, the comparator output Overvoltage Module produces a ***Start*** signal (***V2> Start***), which signifies the "Start of protection". This can be blocked by a ***VTS Fast block*** signal. This ***Start*** signal is applied to the DT timer module. The output of the DT timer module is the ***V2> Trip*** signal which is used to drive the tripping output relay.

The ***V2> Accelerate*** signal accelerates the operating time of the function, by reducing the number of confirmation cycles needed to start the function. At 50 Hz, this means the protection Start is reduced by 20 ms.

11.5.3 APPLICATION NOTES

11.5.3.1 SETTING GUIDELINES

The primary concern is usually the detection of incorrect phase rotation (rather than small imbalances), therefore a sensitive setting is not required. The setting must be higher than any standing NPS voltage, which may be present due to imbalances in the measuring VT, device tolerances etc.

A setting of approximately 15% of rated voltage may be typical.

Note:
*Standing levels of NPS voltage (V2) are displayed in the **V2 Magnitude** cell of the MEASUREMENTS 1 column.*

The operation time of the element depends on the application, but a typical setting would be in the region of 5 seconds.

CHAPTER 12

FREQUENCY PROTECTION FUNCTIONS

12.1 CHAPTER OVERVIEW

The device provides a range of frequency protection functions. This chapter describes the operation of these functions including the principles, logic diagrams and applications.

This chapter contains the following sections:

Chapter Overview 262

Overfluxing Protection 263

Frequency Protection 269

12.2 OVERFLUXING PROTECTION

If a power transformer is connected to an active load such as a generator, it is possible that the ratio of voltage to frequency exceeds certain limits. This will result in Overfluxing, sometimes known as overexcitation. An excessively high voltage or excessively low frequency causes the V/f ratio to rise, producing high flux densities in the magnetic core of the transformer. Overfluxing causes the transformer core to saturate resulting in stray flux in non-laminated components not designed to carry flux. This in turn causes eddy currents in solid components (e.g. core bolts and clamps) and end-of-core laminations causing rapid overheating and damage. Transformer manufacturers provide information about the V/f capability as a function of time. The limit is either in the form of a curve or a set-point with a time delay.

Transformer overfluxing might arise for the following reasons:

- High system voltage
- Generator full load rejection
- Increased voltage due to light loading of transmission lines (Ferranti effect)
- Low system frequency
- Generator excitation at low speed with Automatic Voltage Regulator (AVR) in service
- Geomagnetic disturbance (effects of solar radiation)
- Low frequency earth current circulation through a transmission system

The initial effect of overfluxing is to increase the magnetising current for a transformer. This current will be seen as a differential current, which could cause the device to maloperate, therefore some sort of restraint is needed. The fifth harmonic component of the current is used to block the differential element during mild or short term overfluxing conditions.

Persistent overfluxing however, may result in thermal damage or degradation of a transformer as a result of overheating.

The following protection strategy is therefore advisable to address potential overfluxing conditions:

- Maintain protection stability during transient overfluxing by blocking the differential protection
- Ensure tripping for persistent overfluxing by applying the overfluxing protection. It is common practice to use the overfluxing element to protect the transformer during system disturbance, especially on large network transformers.

12.2.1 OVERFLUXING PROTECTION IMPLEMENTATION

The Overfluxing settings are in the *OVERFLUXING* column of the relevant settings group. Depending on your device model, it provides one or two overfluxing elements with four stages of overfluxing protection plus an additional alarm stage). The P642 has a single-phase VT only, therefore only one overfluxing element is provided. The P643 and P645 can have a single-phase VT and a 3-phase VT, and therefore provides a single-phase overfluxing element and a three-phase overfluxing element. Both elements are similar in functionality and follow the same logical principles.

You enable or disable each stage of the overfluxing protection for each element by the relevant Status cells ***V/Hz>(n) Status*** and ***V/HZ Alm Status***.

The first stage can be set to operate with a definite time or inverse time delay (IDMT). This stage can be used to provide the protection trip output. The other three stages are all definite time stages. These can be combined with the first stage inverse time characteristic to create a combined multi-stage overfluxing trip operating characteristic using PSL.

An inhibit signal is provided for the first stage 1 only. This allows a definite time stage to override a section of the inverse time characteristic if required. The inhibit signal has the effect of resetting the timer, the start signal and the trip signal.

In addition to tripping stages 1 to 4, an Alarm stage is also provided (***V/Hz> Alm***) for each of the elements. This can be used to indicate an unhealthy condition.

12.2.1.1 TIME-DELAYED OVERFLUXING PROTECTION

Protection against damage due to prolonged overfluxing is achieved by using the first overfluxing protection stage with the IDMT characteristic. The setting flexibility of this element, by adjustment of the time delay at various V/Hz values, makes it suitable for various country-specific requirements. The manufacturer of the transformer should be able to supply information about the short-time over-excitation capabilities, which you can use to determine appropriate settings for the V/Hz tripping element. This variable time overfluxing protection should be used to trip the transformer directly.

The IDMT characteristic is $T = TMS/(M - 1)^2$

where:

M = (V/f p.u.) / (V/f trip setting)

V and F are measured entities

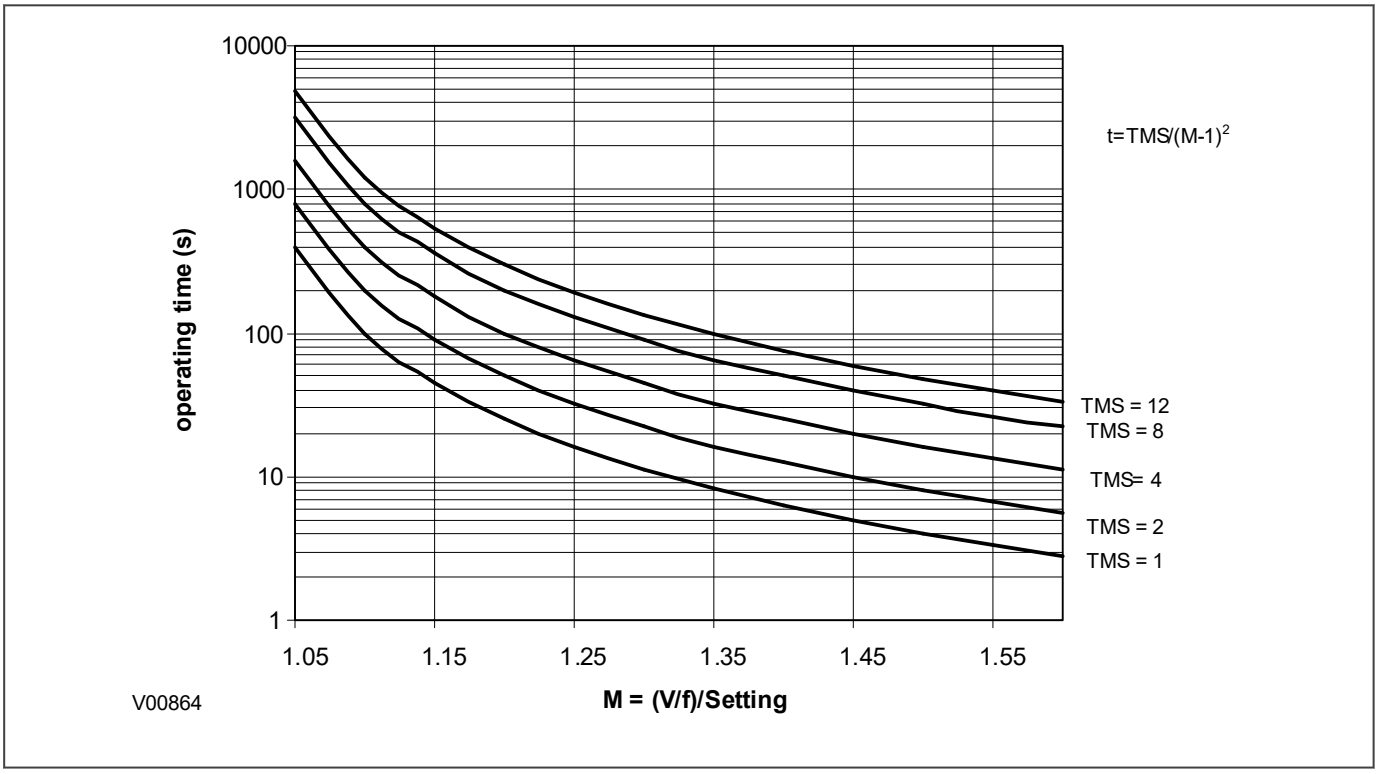


Figure 127: Variable time overfluxing protection characteristic

The IDMT characteristic is implemented as a thermal function. The internal IDMT timer is treated as a thermal replica with a cooling characteristic. After a V/Hz excursion, the timer should reset according to the reset cooling characteristic. Otherwise, if the unit is subjected to another V/Hz excursion before it has cooled to normal condition, damage could occur before the V/Hz trip point is reached.

A linear reset curve with a Reset Time (V/Hz>x tReset) setting is used for this purpose. The actual reset time left is:

Reset time = tReset * IDMTtimer/tTarget

Where $tTarget = TMS/(M-1)^2$.

The actual trip time delay is:

Trip delay = tTarget * (1-RESETtimer/tReset)

To make use of the time delayed overfluxing protection, the device must be supplied with a voltage signal which is representative of the primary system voltage on the source side of the transformer. This is defined by the ***Ref Voltage*** setting in the *OVERFLUXING* column.

The following diagram explains the reset characteristic. It will take tReset time for the thermal replica to reset completely to zero after it has reached 100% of ***V/f>1 trip*** at stage 1. If the thermal replica has not reached 100% of V/f>1 Trip, the reset time will be reduced proportionally. For example, if the reset time is set to 100 seconds, and the thermal replica has only reached 50% of V/f> Trip when V/Hz resets, the reset time will be 50 seconds as shown in stage 2. If another V/Hz excursion appears before the first reset reaches V/f Reset, the V/Hz time delay takes the reset time left into consideration, as shown in stage 3.

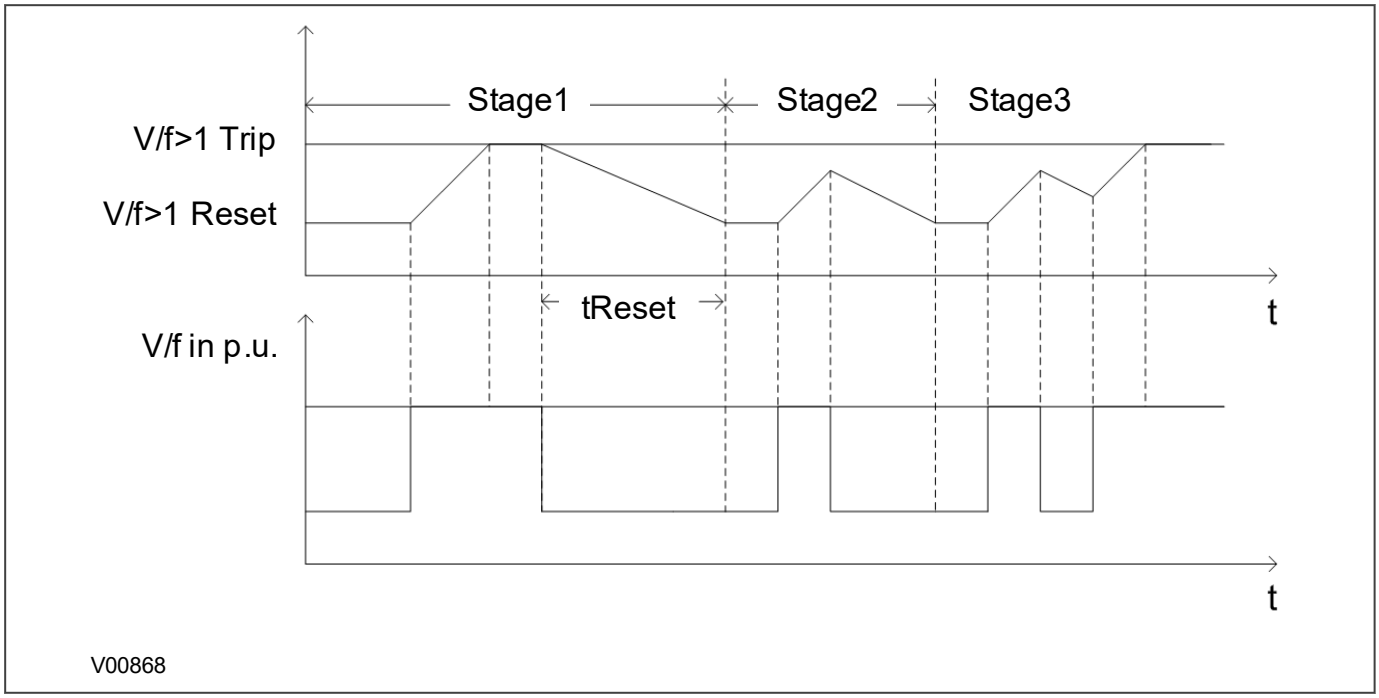


Figure 128: Overfluxing reset characteristic

12.2.1.2 5TH HARMONIC BLOCKING

A differential current 5th harmonic blocking feature can be used to prevent possible maloperation under transient overfluxing conditions. The 5th harmonic signal is derived from the differential current waveform on each phase. Blocking is on a per phase basis.

To ensure tripping for persistent overfluxing, caused by high system voltage or low system frequency, the device provides time delayed overfluxing protection. Where there is any risk of persistent geomagnetic overfluxing, with normal system voltage and frequency, the 5th harmonic differential current facility can be used to initiate tripping after a long time delay. This time delay would need to be programmed in the PSL as shown:

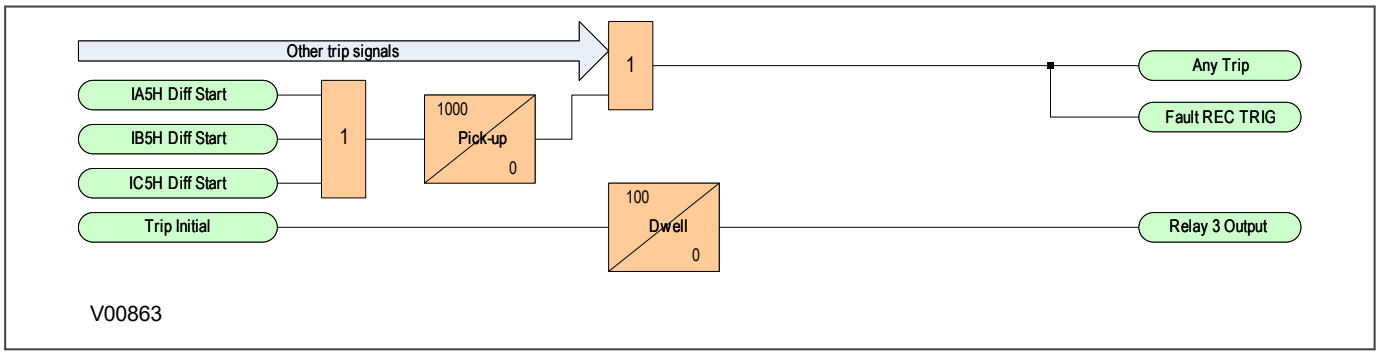


Figure 129: 5th harmonic blocking time delay in PSL

12.2.1.3 OVERFLUXING PROTECTION LOGIC

The overfluxing protection logic is shown below. This diagram shows the case where the first stage timer is set to IDMT. You can select a DT timer for the first stage if required with the setting ***V/Hz>1 Trip Func***. The diagram shown is for the 3-phase VT element. The single-phase element follows the same principles.

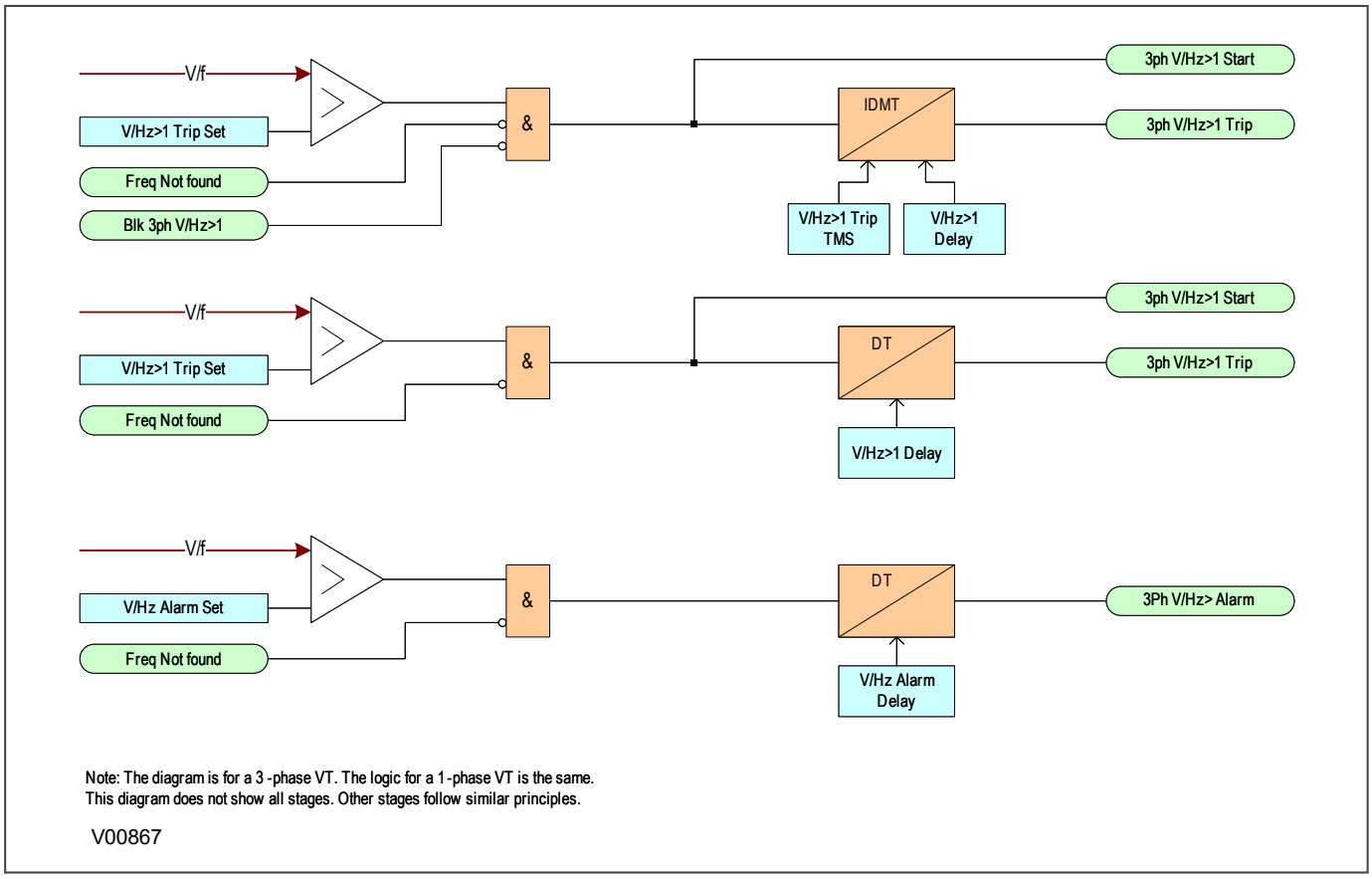


Figure 130: Overfluxing protection logic

12.2.2 APPLICATION NOTES

12.2.2.1 OVERFLUXING PROTECTION SETTING GUIDELINES

The pick up value for the overfluxing elements depends on the nominal core flux density levels. Unit transformers generally run at higher flux densities than transmission and distribution transformers, so they require a higher pick up setting and shorter tripping times which reflect this. Transmission transformers can also be at risk from overfluxing conditions, and you should take withstand levels into consideration when deciding on the required settings.

The IEEE C37.91-2000 standard states that overexcitation of a transformer can occur whenever the ratio of the per unit voltage to per unit frequency (V/Hz) at the secondary terminals of a transformer exceeds its rating of 1.05 per unit (PU) on transformer base at full load, 0.8 power factor, or 1.1 PU at no load.

Please refer to clause 4.1.6 in IEEE C57.12.00-2006 for further clarification on the capability of a transformer to operate above rated voltage and below rated frequency.

The element is set in terms of the actual ratio of voltage to frequency. You can therefore calculate the overfluxing threshold setting ***V/Hz>(n) Trip Set***, as follows:

A setting of 1.05 p.u. would equate to 110/50 x 1.05 = 2.31

where:

- The VT secondary voltage at rated primary volts is 110 V
- The rated frequency is 50 Hz

You should set the overfluxing alarm stage threshold ***V/Hz Alarm Set***, lower than the trip stage setting, to provide an indication that abnormal conditions are present and to alert an operator to adjust system parameters accordingly.

You should choose the time delay settings to match the withstand characteristics of the protected transformer. For an inverse time characteristic, set the time multiplier setting, ***V/Hz>1 Trip TMS*** such that the operating characteristic closely matches the withstand characteristic of transformer. For definite time trip stages, set the time delay ***V/Hz>(n) Trip Delay*** cells. The alarm stage time delay is set in the ***V/Hz Alarm Delay*** cell.

You can use PSL to combine the stages to create a multi-stage ***V/Hz*** trip operating characteristic, as shown below:

Note:
Consult the manufacturers' withstand characteristics before formulating these settings.

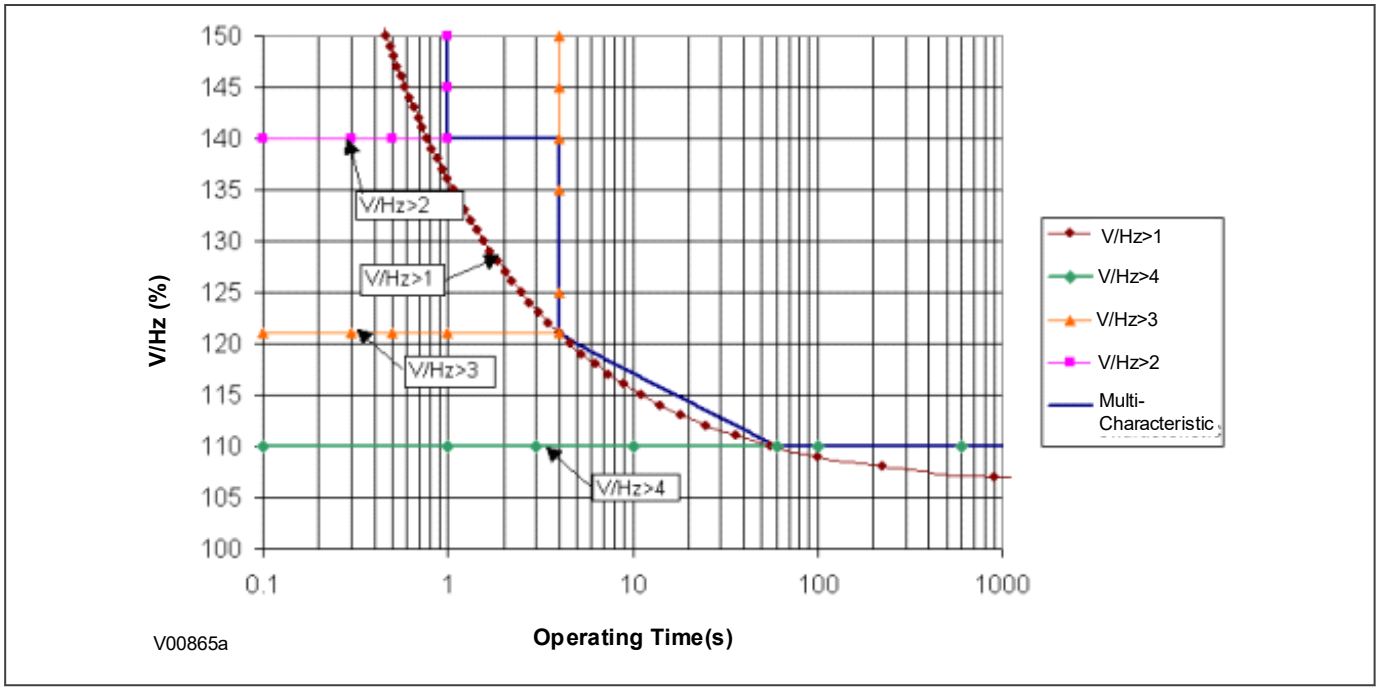


Figure 131: Multi-stage overfluxing characteristic

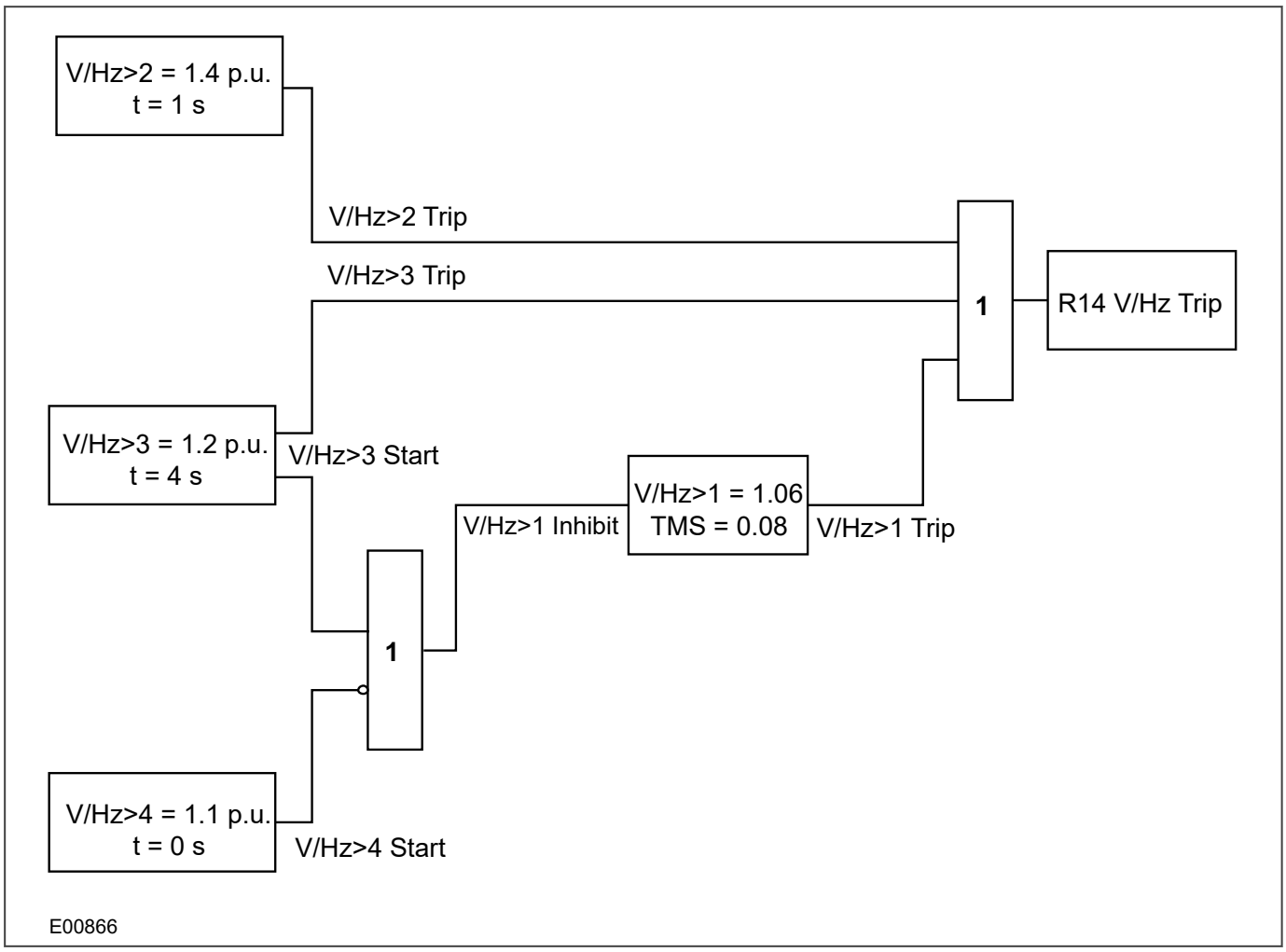


Figure 132: Scheme logic for multi-stage overfluxing characteristic

12.3 FREQUENCY PROTECTION

Power generation and utilisation needs to be well balanced in any industrial, distribution or transmission network. These electrical networks are dynamic entities, with continually varying loads and supplies, which are continually affecting the system frequency. Increased loading reduces the system frequency and generation needs to be increased to maintain the frequency of the supply. Conversely decreased loading increases the system frequency and generation needs to be reduced. Sudden fluctuations in load can cause rapid changes in frequency, which need to be dealt with quickly.

Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse, which has dire consequences.

Normally, generators are rated for a particular band of frequency. Operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken. This type of protection can be used for operator alarms or turbine trips in case of severe frequency decay.

Clearly a range of methods is required to ensure system frequency stability. The frequency protection in this device provides both underfrequency and overfrequency protection.

Frequency Protection is implemented in the *FREQ PROTECTION* column of the relevant settings group.

12.3.1 UNDERFREQUENCY PROTECTION

A reduced system frequency implies that the net load is in excess of the available generation. Such a condition can arise, when an interconnected system splits, and the load left connected to one of the subsystems is in excess of the capacity of the generators in that particular subsystem. Industrial plants that are dependant on utilities to supply part of their loads will experience underfrequency conditions when the incoming lines are lost.

Many types of industrial loads have limited tolerances on the operating frequency and running speeds (e.g. synchronous motors). Sustained underfrequency has implications on the stability of the system, whereby any subsequent disturbance may damage equipment and even lead to blackouts. It is therefore essential to provide protection for underfrequency conditions.

12.3.1.1 UNDERFREQUENCY PROTECTION IMPLEMENTATION

Simple underfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 4 stages of underfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F<1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F<1 Setting***: defines the frequency pickup setting
- ***F<1 Time Delay***: sets the time delay

12.3.1.2 UNDERFREQUENCY PROTECTION LOGIC

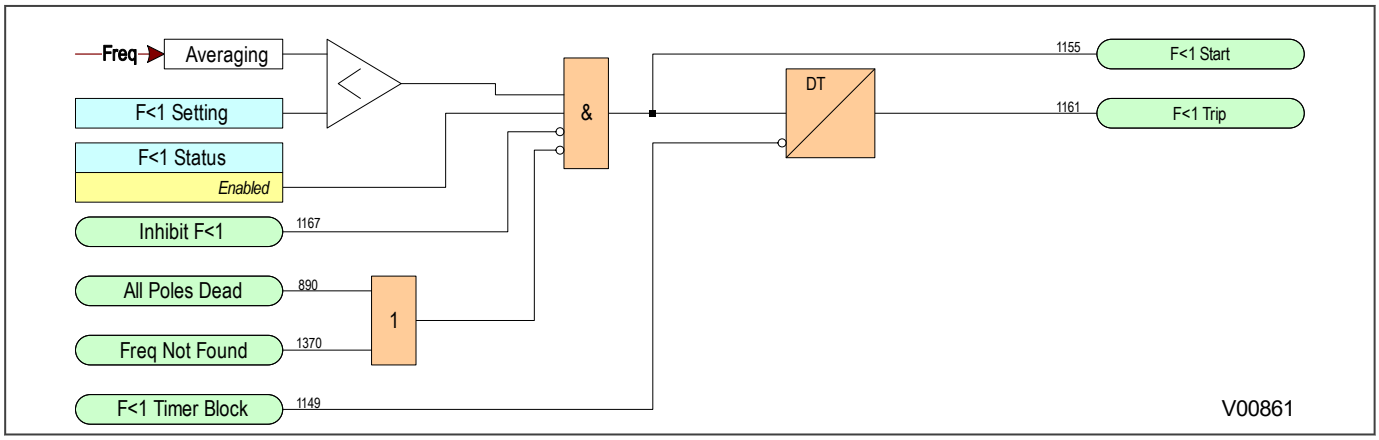


Figure 133: Underfrequency logic (single stage)

If the frequency is below the setting and not blocked the DT timer is started. If the frequency cannot be determined, the function is blocked.

12.3.1.3 APPLICATION NOTES

12.3.1.3.1 SETTING GUIDELINES

In order to minimise the effects of underfrequency, a multi-stage load shedding scheme may be used with the plant loads prioritised and grouped. During an underfrequency condition, the load groups are disconnected sequentially, with the highest priority group being the last one to be disconnected.

The effectiveness of each load shedding stage depends on the proportion of power deficiency it represents. If the load shedding stage is too small compared with the prevailing generation deficiency, then there may be no improvement in the frequency. This should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. These should not be excessive as this could jeopardize system stability. Time delay settings of 5 - 20 s are typical.

The protection function should be set so that declared frequency-time limits for the generating set are not infringed. Typically, a 10% underfrequency condition should be continuously sustainable.

12.3.2 OVERFREQUENCY PROTECTION

An increased system frequency arises when the mechanical power input to a generator exceeds the electrical power output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre. Under such conditions, the governor would normally respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Overfrequency protection is required as a backup to cater for cases where the reaction of the control equipment is too slow.

12.3.2.1 OVERFREQUENCY PROTECTION IMPLEMENTATION

Simple overfrequency Protection is configured in the FREQ PROTECTION column of the relevant settings group.

The device provides 2 stages of overfrequency protection. The function uses the following settings (shown for stage 1 only - other stages follow the same principles).

- ***F>1 Status:*** enables or disables underfrequency protection for the relevant stage
- ***F>1 Setting***: defines the frequency pickup setting
- ***F>1 Time Delay***: sets the time delay

12.3.2.2 OVERFREQUENCY PROTECTION LOGIC

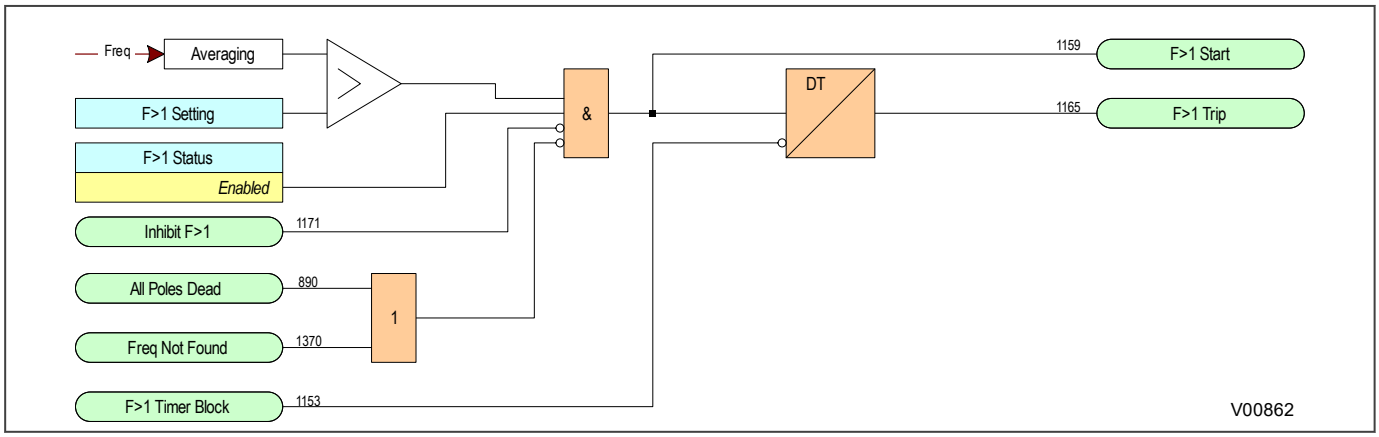


Figure 134: Overfrequency logic (single stage)

If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out, the trip is produced. If the frequency cannot be determined, the function is blocked.

12.3.2.3 APPLICATION NOTES

12.3.2.3.1 SETTING GUIDELINES

Following changes on the network caused by faults or other operational requirements, it is possible that various subsystems will be formed within the power network. It is likely that these subsystems will suffer from a generation/ load imbalance. The "islands" where generation exceeds the existing load will be subject to overfrequency conditions. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element can be suitably set to sense this contingency.

CHAPTER 13

MONITORING AND CONTROL

13.1 CHAPTER OVERVIEW

As well as providing a range of protection functions, the product includes comprehensive monitoring and control functionality.

This chapter contains the following sections:

Chapter Overview 274
Event Records 275
Disturbance Recorder 283
Measurements 284
Current Input Exclusion Function 286
Circuit Breaker Control 288
Pole Dead Function 292
Switch Status and Control 296
Test Mode 301
IEC 61850 Control Authority 302

13.2 EVENT RECORDS

GE Vernova devices record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyse how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged.

The event records can be displayed on an IED's front panel but it is easier to view them through the settings application software. This can extract the events log from the device and store it as a single .evt file for analysis on a PC.

The event records are detailed in the *VIEW RECORDS* column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

If viewing the event with the settings application software, simply open the extracted event file. All the events are displayed chronologically. Each event is summarised with a time stamp obtained from the ***Time & Date*** cell) and a short description relating to the event obtained from the ***Event Text*** cell). You can expand the details of the event by clicking on the **+** icon to the left of the time stamp.

The following table shows the correlation between the fields in the setting application software's event viewer and the cells in the menu database.

Field in Event Viewer	Equivalent cell in menu DB	Cell reference	User settable?
Left hand column header	VIEW RECORDS → Time & Date	01 03	No
Right hand column header	VIEW RECORDS → Event Text	01 04	No
Description	SYSTEM DATA → Description	00 04	Yes
Plant reference	SYSTEM DATA → Plant Reference	00 05	Yes
Model number	SYSTEM DATA → Model Number	00 06	No
Address	Displays the Courier address relating to the event	N/A	No
Event type	VIEW RECORDS → Menu Cell Ref	01 02	No
Event Value	VIEW RECORDS → Event Value	01 05	No
Evt Unique Id	VIEW RECORDS → Evt Unique ID	01 FE	No

The ***Select Event*** setting allows access to individual event records, with the latest event stored at position 0. This setting also defines the maximum number of records available.

In addition to the event log, there are two logs which contain duplicates of the last 5 maintenance records and the last 5 fault records. The purpose of this is to provide convenient access to the most recent fault and maintenance events.

13.2.1 EVENT TYPES

There are several different types of event:

- Opto-input events (Change of state of opto-input)
- Contact events (Change of state of output relay contact)
- Alarm events
- Fault record events
- Standard events
- Security events

Standard events are further sub-categorised internally to include different pieces of information. These are:

- Protection events (starts and trips)
- Maintenance record events
- Platform events

Note:
The first event in the list (event 0) is the most recent event to have occurred.

13.2.1.1 OPTO-INPUT EVENTS

If one or more of the opto-inputs has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all opto-inputs. You can tell which opto-input has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Logic Inputs #` where # is the batch number of the opto-inputs. This is '1', for the first batch of opto-inputs and '2' for the second batch of opto-inputs (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the opto-inputs, where the Least Significant Bit (LSB), on the right corresponds to the first opto-input `Input L1`.

The same information is also shown in the ***Opto I/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

13.2.1.2 CONTACT EVENTS

If one or more of the output relays (also known as output contacts) has changed state since the last time the protection algorithm ran (which runs at several times per cycle), a new event is created, which logs the logic states of all output relays. You can tell which output relay has changed state by comparing the new event with the previous one.

The description of this event type, as shown in the ***Event Text*** cell is always `Output Contacts #` where # is the batch number of the output relay contacts. This is '1', for the first batch of output contacts and '2' for the second batch of output contacts (if applicable).

The event value shown in the ***Event Value*** cell for this type of event is a binary string. This shows the logical states of the output relays, where the LSB (on the right) corresponds to the first output contact `Output R1`.

The same information is also shown in the ***Relay O/P Status*** cell in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

13.2.1.3 ALARM EVENTS

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event.

The description of this event type, as shown in the ***Event Text*** cell is cell dependent on the type of alarm and will be one of those shown in the following tables, followed by `OFF` or `ON`.

The event value shown in the ***Event Value*** cell for this type of event is a 32 bit binary string. There are one or more banks 32 bit registers, depending on the device model. These contain all the alarm types and their logic states (`ON` or `OFF`).

The same information is also shown in the ***Alarm Status (n)*** cells in the *SYSTEM DATA* column. This information is updated continuously, whereas the information in the event log is a snapshot at the time when the event was created.

Alarm Status 1

Bit no.	Bit Mask (hex)	Alarm Description
0	0x00000001	Not Used
1	0x00000002	Not Used
2	0x00000004	Setting Group selection by DDB inputs invalid
3	0x00000008	CB Status Alarm
4	0x00000010	RTD Thermal Alarm
5	0x00000020	RTD Open Circuit Failure
6	0x00000040	RTD Short Circuit Failure
7	0x00000080	RTD Data Inconsistency Error
8	0x00000100	RTD Board Failure
9	0x00000200	Current Loop Input 1 Alarm
10	0x00000400	Current Loop Input 2 Alarm
11	0x00000800	Current Loop Input 3 Alarm
12	0x00001000	Current Loop Input 4 Alarm
13	0x00002000	Current Loop Input 1 Undercurrent Fail Alarm
14	0x00004000	Current Loop Input 2 Undercurrent Fail Alarm
15	0x00008000	Current Loop Input 3 Undercurrent Fail Alarm
16	0x00010000	Current Loop Input 4 Undercurrent Fail Alarm
17	0x00020000	Out of Service Alarm
18	0x00040000	Frequency Out of Range Alarm
19	0x00080000	UNUSED
20	0x00100000	UNUSED
21	0x00200000	UNUSED
22	0x00400000	Current Loop Input Failure
23	0x00800000	Current Loop Input Output Failure
24	0x01000000	VCO1 Configuration Alarm
25	0x02000000	VCO2 Configuration Alarm
26	0x04000000	UNUSED
27	0x08000000	CTS Fail Alarm
28	0x10000000	Circuitry FLT Alm
29	0x20000000	VTS VT Fail Alarm
30	0x40000000	Thermal Pre-trip Alarm
31	0x80000000	Aging Acceleration Factor (FAA) alarm

Alarm Status 2

Bit no.	Bit Mask (hex)	Alarm Description
0	0x00000001	LOL alarm

Bit no.	Bit Mask (hex)	Alarm Description
1	0x00000002	Breaker Fail Any Trip
2	0x00000004	CB Fail Alarm T1
3	0x00000008	CB Fail Alarm T2
4	0x00000010	CB Fail Alarm T3
5	0x00000020	CB Fail Alarm T4
6	0x00000040	CB Fail Alarm T5
7	0x00000080	CB Fail Alarm T6
8	0x00000100	CB Fail Alarm T7
9	0x00000200	CB Fail Alarm T8
10	0x00000400	CB Fail Alarm T9
11	0x00000800	CB Fail Alarm T10
12	0x00001000	CB Fail Alarm T11
13	0x00002000	CB Fail Alarm T12
14	0x00004000	CB Fail Alarm T13
15	0x00008000	CB Fail Alarm T14
16	0x00010000	CB Fail Alarm T15
17	0x00020000	CB Fail Alarm T16
18	0x00040000	CB Fail Alarm T17
19	0x00080000	CB Fail Alarm T18
20	0x00100000	UNUSED
21	0x00200000	HV V/Hz>1 Alarm
22	0x00400000	HV V/Hz>2 PrTrp
23	0x00800000	LV V/Hz>1 Alarm
24	0x01000000	LV V/Hz>2 PrTrp
25	0x02000000	UNUSED
26	0x04000000	UNUSED
27	0x08000000	Frequency Protection Alarm
28	0x10000000	Through fault Alarm
29	0x20000000	Z1 Test Mode
30	0x40000000	Z2 Test Mode
31	0x80000000	UNUSED

Alarm Status 3

Bit no.	Bit Mask (hex)	Alarm Description
0	0x00000001	Battery Fail alarm indication
1	0x00000002	Failure
2	0x00000004	unused

Bit no.	Bit Mask (hex)	Alarm Description
3	0x00000008	Enrolled GOOSE IED absent alarm indication
4	0x00000010	Network Interface Card not fitted/failed alarm
5	0x00000020	Network Interface Card not responding alarm
6	0x00000040	Network Interface Card fatal error alarm indication
7	0x00000080	Network Interface Card software reload alarm
8	0x00000100	Bad TCP/IP Configuration Alarm
9	0x00000200	Bad OSI Configuration Alarm
10	0x00000400	Network Interface Card link fail alarm indication
11	0x00000800	Main card/NIC software mismatch alarm indication
12	0x00001000	IP address conflict alarm indication
13	0x00002000	unused
14	0x00004000	unused
15	0x00008000	unused
16	0x00010000	unused
17	0x00020000	unused
18	0x00040000	unused
19	0x00080000	unused
20	0x00100000	SNTP Failure Alarm
21	0x00200000	MMS libraries memory allocation fails.
22	0x00400000	unused
23	0x00800000	unused
24	0x01000000	unused
25	0x02000000	unused
26	0x04000000	unused
27	0x08000000	unused
28	0x10000000	unused
29	0x20000000	unused
30	0x40000000	unused
31	0x80000000	unused

Alarm Status 4

Bit no.	Bit Mask (hex)	Alarm Description
0	0x00000001	User Alarm 1 (0=Self-reset, 1=Manual reset)
1	0x00000002	User Alarm 2 (0=Self-reset, 1=Manual reset)
2	0x00000004	User Alarm 3 (0=Self-reset, 1=Manual reset)
3	0x00000008	User Alarm 4 (0=Self-reset, 1=Manual reset)
4	0x00000010	User Alarm 5 (0=Self-reset, 1=Manual reset)

Bit no.	Bit Mask (hex)	Alarm Description
5	0x00000020	User Alarm 6 (0=Self-reset, 1=Manual reset)
6	0x00000040	User Alarm 7 (0=Self-reset, 1=Manual reset)
7	0x00000080	User Alarm 8 (0=Self-reset, 1=Manual reset)
8	0x00000100	User Alarm 9 (0=Self-reset, 1=Manual reset)
9	0x00000200	User Alarm 10 (0=Self-reset, 1=Manual reset)
10	0x00000400	User Alarm 11 (0=Self-reset, 1=Manual reset)
11	0x00000800	User Alarm 12 (0=Self-reset, 1=Manual reset)
12	0x00001000	User Alarm 13 (0=Self-reset, 1=Manual reset)
13	0x00002000	User Alarm 14 (0=Self-reset, 1=Manual reset)
14	0x00004000	User Alarm 15 (0=Self-reset, 1=Manual reset)
15	0x00008000	User Alarm 16 (0=Self-reset, 1=Manual reset)
16	0x00010000	User Alarm 17 (0=Self-reset, 1=Manual reset)
17	0x00020000	User Alarm 18 (0=Self-reset, 1=Manual reset)
18	0x00040000	User Alarm 19 (0=Self-reset, 1=Manual reset)
19	0x00080000	User Alarm 20 (0=Self-reset, 1=Manual reset)
20	0x00100000	User Alarm 21 (0=Self-reset, 1=Manual reset)
21	0x00200000	User Alarm 22 (0=Self-reset, 1=Manual reset)
22	0x00400000	User Alarm 23 (0=Self-reset, 1=Manual reset)
23	0x00800000	User Alarm 24 (0=Self-reset, 1=Manual reset)
24	0x01000000	User Alarm 25 (0=Self-reset, 1=Manual reset)
25	0x02000000	User Alarm 26 (0=Self-reset, 1=Manual reset)
26	0x04000000	User Alarm 27 (0=Self-reset, 1=Manual reset)
27	0x08000000	User Alarm 28 (0=Self-reset, 1=Manual reset)
28	0x10000000	User Alarm 29 (0=Self-reset, 1=Manual reset)
29	0x20000000	User Alarm 30 (0=Self-reset, 1=Manual reset)
30	0x40000000	User Alarm 31 (0=Self-reset, 1=Manual reset)
31	0x80000000	User Alarm 32 (0=Self-reset, 1=Manual reset)

13.2.1.4 FAULT RECORD EVENTS

An event record is created for every fault the IED detects. This is also known as a fault record.

The event type description shown in the ***Event Text*** cell for this type of event is always `Fault Recorded`.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the ***Select Fault*** setting, where fault number 0 is the latest fault.

A fault record is triggered by the ***Fault REC TRIG*** signal DDB, which is assigned in the PSL. The fault recorder records the values of all parameters associated with the fault for the duration of the fault. These parameters are stored in separate Courier cells, which become visible depending on the type of fault.

The fault recorder stops recording only when:

The Start signal is reset AND the undercurrent is ON OR the Trip signal is reset, as shown below:

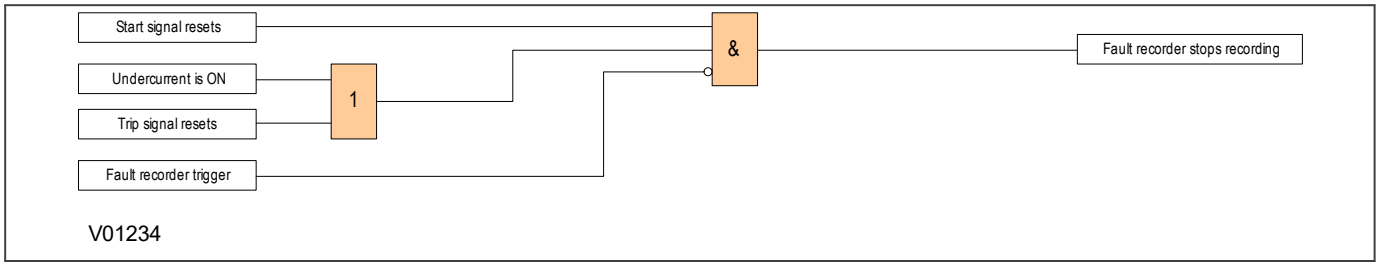


Figure 135: Fault recorder stop conditions

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The timestamp assigned to the fault record event corresponds to the time when the fault recorder stops.

Note:
We recommend that you do not set the triggering contact to latching. This is because if you use a latching contact, the fault record would not be generated until the contact has been fully reset.

13.2.1.5 MAINTENANCE EVENTS

Internal failures detected by the self-test procedures are logged as maintenance records. Maintenance records are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is always `Maint Recorded`.

The ***Event Value*** cell also provides a unique binary code.

The IED contains a separate register containing the latest maintenance records. This provides a convenient way of viewing the latest maintenance records and saves searching through the event log. You access these fault records using the ***Select Maint*** setting.

The maintenance record has a number of extra menu cells relating to the maintenance event. These parameters are ***Maint Text***, ***Maint Type*** and ***Maint Data***. They contain details about the maintenance event selected with the ***Select Maint*** cell.

13.2.1.6 PROTECTION EVENTS

The IED logs protection starts and trips as individual events. Protection events are special types of standard events.

The event type description shown in the ***Event Text*** cell for this type of event is dependent on the protection event that occurred. Each time a protection event occurs, a DDB signal changes state. It is the name of this DDB signal followed by 'ON' or 'OFF' that appears in the ***Event Text*** cell.

The ***Event Value*** cell for this type of event is a 32 bit binary string representing the state of the relevant DDB signals. These binary strings can also be viewed in the *COMMISSION TESTS* column in the relevant DDB batch cells.

Not all DDB signals can generate an event. Those that can are listed in the *RECORD CONTROL* column. In this column, you can set which DDBs generate events.

13.2.1.7 SECURITY EVENTS

An event record is generated each time a setting that requires an access level is executed.

The event type description shown in the ***Event Text*** cell displays the type of change.

13.2.1.8 PLATFORM EVENTS

Platform events are special types of standard events.

The event type description shown in the ***Event Text*** cell displays the type of change.

13.3 DISTURBANCE RECORDER

The disturbance recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals. The digital signals may be inputs, outputs, or internal DDB signals. The disturbance records can be extracted using the disturbance record viewer in the settings application software. The disturbance record file can also be stored in the COMTRADE format. This allows the use of other packages to view the recorded data.

The integral disturbance recorder has an area of memory specifically set aside for storing disturbance records. The number of records that can be stored is dependent on the recording duration. The minimum duration is 0.1 s and the maximum duration is 10.5 s.

When the available memory is exhausted, the oldest records are overwritten by the newest ones.

Each disturbance record consists of a number of analogue data channels and digital data channels. The relevant CT and VT ratios for the analogue channels are also extracted to enable scaling to primary quantities.

The fault recording times are set by a combination of the ***Duration*** and ***Trigger Position*** cells. The ***Duration*** cell sets the overall recording time and the ***Trigger Position*** cell sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.

With the ***Trigger Mode*** set to *Single*, if further triggers occurs whilst a recording is taking place, the recorder will ignore the trigger. However, with the ***Trigger Mode*** set to *Extended*, the post trigger timer will be reset to zero, extending the recording time.

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

You may choose any of the digital channels to trigger the disturbance recorder on either a low to high or a high to low transition, via the ***Input Trigger*** cell. The default settings are such that any dedicated trip output contacts will trigger the recorder.

It is not possible to view the disturbance records locally via the front panel LCD. You must extract these using suitable setting application software such as MiCOM S1 Agile.

13.4 MEASUREMENTS

13.4.1 MEASURED QUANTITIES

The device measures directly and calculates a number of system quantities, which are updated every second. You can view these values in the relevant MEASUREMENT columns or with the Measurement Viewer in the settings application software. Depending on the model, the device may measure and display some or more of the following quantities:

- Measured and calculated analogue current and voltage values
- Power and energy quantities
- Peak, fixed and rolling demand values
- Frequency measurements
- Thermal measurements

13.4.1.1 MEASURED AND CALCULATED CURRENTS

The device measures phase-to-phase and phase-to-neutral current values. The values are produced by sampling the analogue input quantities, converting them to digital quantities to present the magnitude and phase values. Sequence quantities are produced by processing the measured values. These are also displayed as magnitude and phase angle values.

These measurements are contained in the *MEASUREMENTS 1* column.

13.4.1.2 MEASURED AND CALCULATED VOLTAGES

The device measures phase-to-phase and phase-to-neutral voltage values. The values are produced by sampling the analogue input quantities, converting them to digital quantities to present the magnitude and phase values. Sequence quantities are produced by processing the measured values. These are also displayed as magnitude and phase angle values.

These measurements are contained in the *MEASUREMENTS 1* column.

13.4.1.3 POWER AND ENERGY QUANTITIES

Using the measured voltages and currents the device calculates the apparent, real and reactive power quantities. These are produced on a phase by phase basis together with three-phase values based on the sum of the three individual phase values. The signing of the real and reactive power measurements can be controlled using the measurement mode setting. The four options are defined in the following table:

Measurement Mode	Parameter	Signing
0 (Default)	Export Power Import Power Lagging Vars Leading VArs	+ – + –
1	Export Power Import Power Lagging Vars Leading VArs	– + + –
2	Export Power Import Power Lagging Vars Leading VArs	+ – – +

Measurement Mode	Parameter	Signing
3	Export Power Import Power Lagging Vars Leading VArs	– + – +

The device also calculates the per-phase and three-phase power factors.

These power values increment the total real and total reactive energy measurements. Separate energy measurements are maintained for the total exported and imported energy. The energy measurements are incremented up to maximum values of 1000 GWhr or 1000 GVARhr at which point they reset to zero. It is possible to reset these values using the menu or remote interfaces using the Reset demand cell.

These measurements are contained in the *MEASUREMENTS 2* column.

13.4.1.4 DEMAND VALUES

The device produces fixed, rolling, and peak demand values. You reset these quantities using the ***Reset demand*** cell.

The fixed demand value is the average value of a quantity over the specified interval. Values are produced for three phase real and reactive power. The fixed demand values displayed are those for the previous interval. The values are updated at the end of the fixed demand period according to the ***Fix Dem Period*** setting in the *MEASURE'T SETUP* column.

The rolling demand values are similar to the fixed demand values, but a sliding window is used. The rolling demand window consists of a number of smaller sub-periods. The resolution of the sliding window is the sub-period length, with the displayed values being updated at the end of each of the sub-periods according to the ***Roll Sub Period*** setting in the *MEASURE'T SETUP* column.

Peak demand values are produced for each phase current and the real and reactive power quantities. These display the maximum value of the measured quantity since the last reset of the demand values.

These measurements are contained in the *MEASUREMENTS 2* column.

13.4.1.5 OTHER MEASUREMENTS

Depending on the model, the device produces a range of other measurements such as thermal measurements.

These measurements are contained in the *MEASUREMENTS 3* column.

13.4.2 MEASUREMENT SETUP

You can define the way measurements are set up and displayed using the *MEASURE'T SETUP* column and the measurements are shown in the relevant MEASUREMENTS tables.

13.4.3 OPTO-INPUT TIME STAMPING

Each opto-input sample is time stamped within a tolerance of +/- 1 ms with respect to the Real Time Clock. These time stamps are used for the opto event logs and for the disturbance recording. The device needs to be synchronised accurately to an external clock source such as an IRIG-B signal or a master clock signal provided in the relevant data protocol.

For both the filtered and unfiltered opto-inputs, the time stamp of an opto-input change event is the sampling time at which the change of state occurred. If multiple opto-inputs change state at the same sampling interval, these state changes are reported as a single event.

13.5 CURRENT INPUT EXCLUSION FUNCTION

In the P643 and P645, it is possible to exclude current inputs from the protection functions. This may be useful for example in a phase shifting transformer, or during the commissioning or maintenance process.

When a current input is excluded, the device sets the current from that input to zero for calculation purposes, even if the current measured is not zero. The device compares the actual current flowing with the under current element threshold to ensure that the CT input is excluded if the current is below the undercurrent threshold when the master CT exclusion DDB signal is not asserted. The under current threshold is fixed to 0.05 In.

13.5.1 CURRENT INPUT EXCLUSION LOGIC

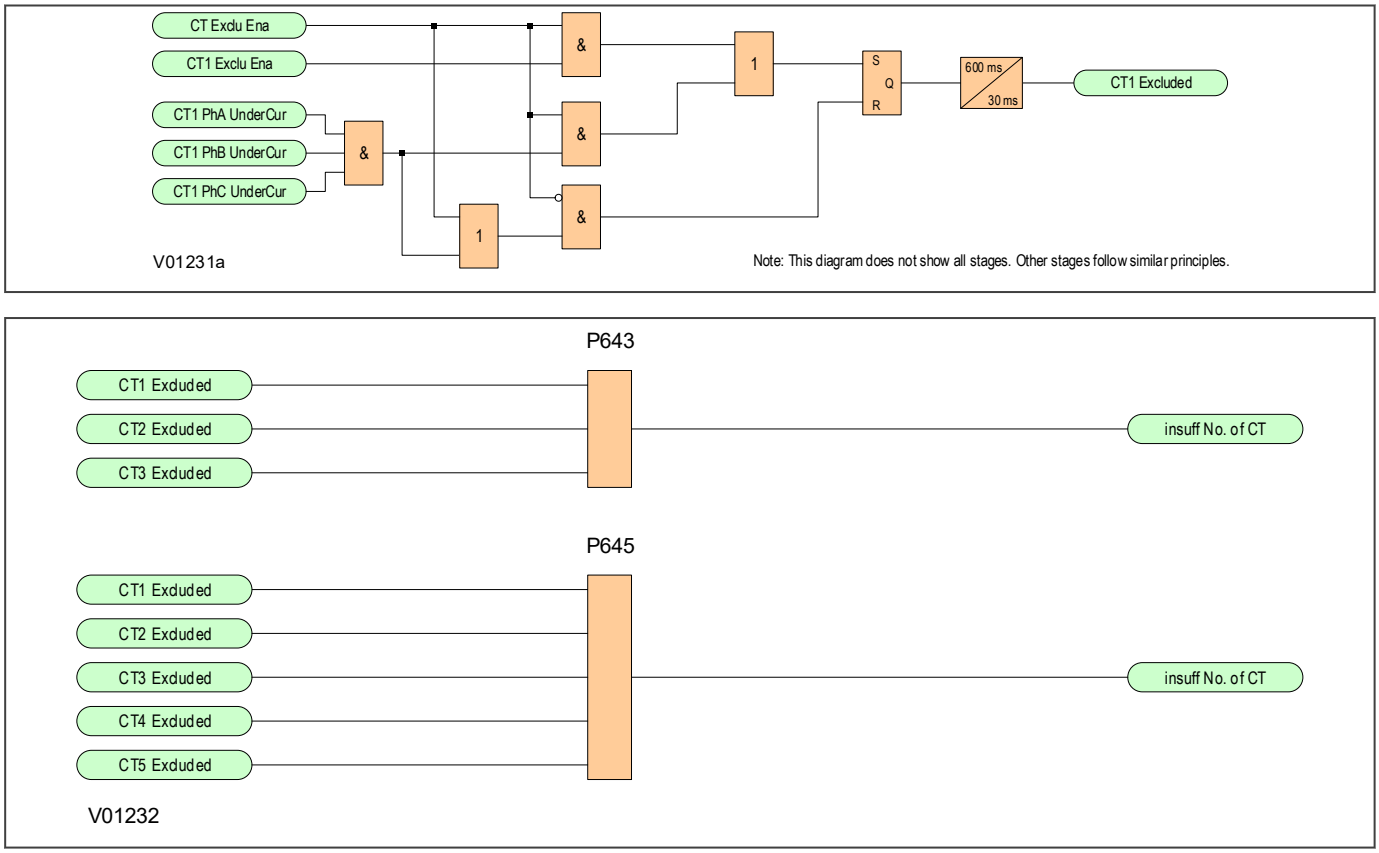


Figure 136: CT Exclusion logic

Only one current input can be excluded from the P643 and a maximum of three current inputs can be excluded from the P645. An alarm DDB (***Insuff No. of CT***) is issued when more than the maximum number of current inputs are excluded. The status of the exclusion DDB signals (***CTx Excluded***) is stored in the device's internal non-volatile memory. An alarm (***Disc CT Invalid***) is raised if the stored statuses do not match the statuses after the power supply is re-established. When the ***Disc CT Invalid*** DDB signal is asserted, all protection functions using the relevant CT inputs are blocked.

Note:
For the differential element to operate correctly, the number of CTs used cannot be less than 2. Also CTs should be excluded one at a time.

13.5.2 APPLICATION NOTES

13.5.2.1 CURRENT INPUT EXCLUSION EXAMPLE

In the following figure, the adjacent isolators to CB1 are open and locked because of maintenance work on CB1.

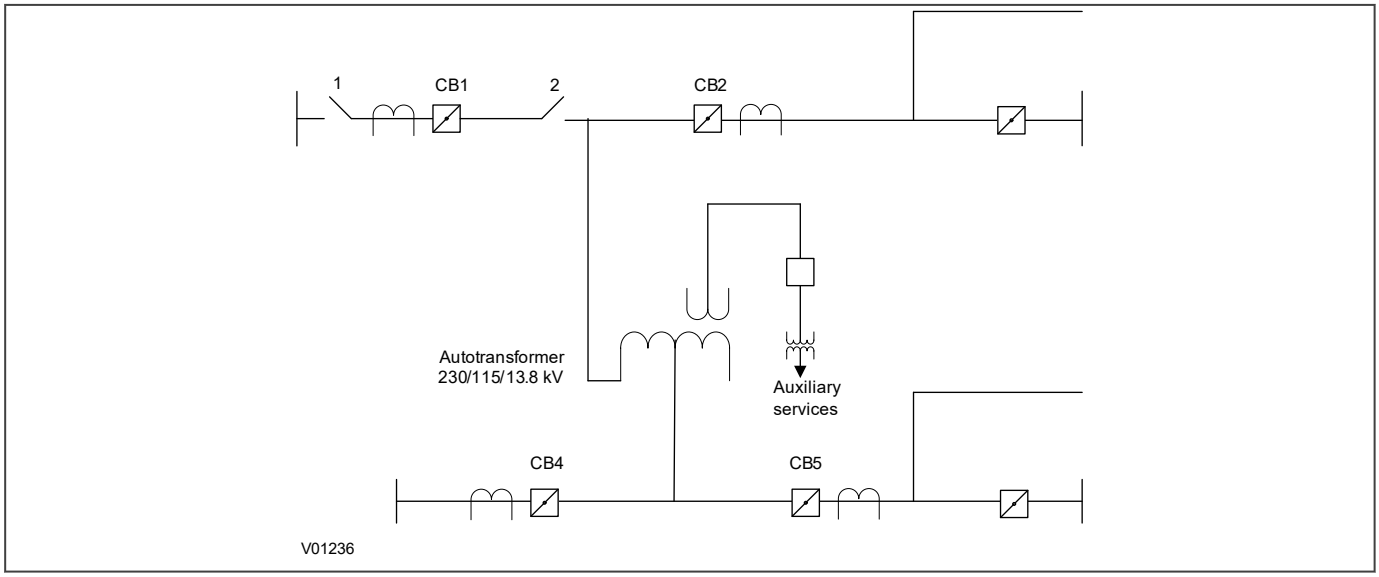


Figure 137: CT input exclusion - 1.5 CB application

The current transformer associated with CB1 is connected to the T1 CT input. Auxiliary contacts from CB1 isolators 1 and 2 must be connected to an opto-input as follows.

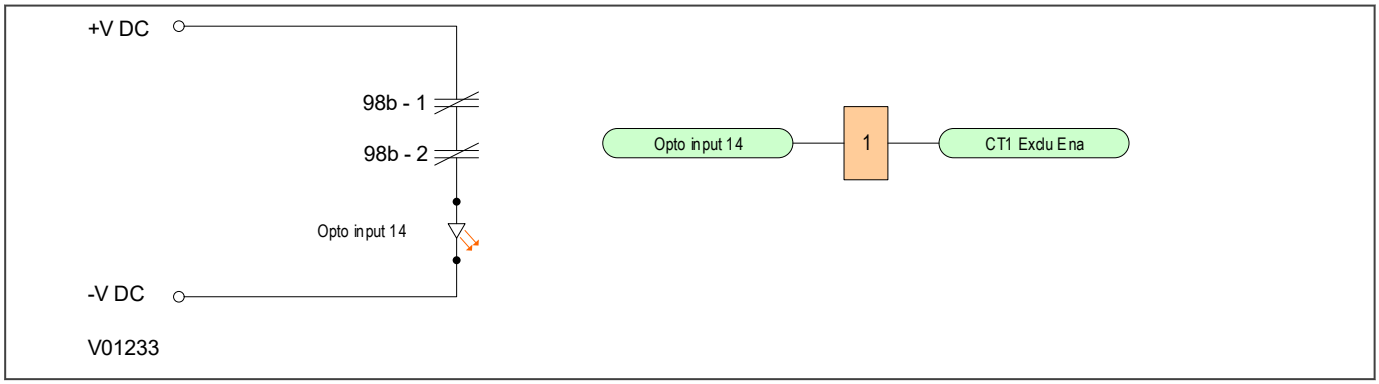


Figure 138: CT input exclusion - auxiliary contact connection

When isolators 1 and 2 are open, the opto-input L14 is energized and ***CT1 Exclu Ena*** is asserted. To set ***CT1 Excluded***, T1 CT Phase A, B and C undercurrent elements must also be asserted.

13.6 CIRCUIT BREAKER CONTROL

Although some circuit breakers do not provide auxiliary contacts, most provide auxiliary contacts to reflect the state of the circuit breaker. For P64 IEDs the status information needs to be wired in the PSL using the DDBs CBx Closed, where x is the number of CB.

If no CB auxiliary contacts are available then no CB control will be possible.

For controls, the ***CB control by*** cell should be set accordingly.

The output contact can be set to operate following a time delay defined by the setting ***Man Close Delay***. One reason for this delay is to give personnel time to safely move away from the circuit breaker following a CB close command.

The length of the trip and close control pulses can be set via the ***Trip Pulse Time*** and **Close Pulse Time** settings respectively. These should be set long enough to ensure the breaker has completed its open or close cycle before the pulse has elapsed.

If an attempt to close the breaker is being made, and a protection trip signal is generated, the protection trip command overrides the close command.

If the CB fails to respond to the control command (indicated by no change in the state of CB Status inputs) an alarm is generated after the relevant trip or close pulses have expired. This alarm can be viewed on the LCD display, remotely, or can be assigned to an output contact using the programmable scheme logic (PSL).

Note:
*The **CB Healthy Time** set under this menu section is applicable to manual circuit breaker operations only.*

The device includes the following options for control of a single circuit breaker:

- The IED menu (local control)
- The CB Open/Close keys and the SLD on the graphical HMI
- The opto-inputs (local control)
- SCADA communication (remote control)

13.6.1 CB CONTROL USING THE IED MENU

You can control manual trips and closes with the ***CB Trip/Close*** command in the *SYSTEM DATA* column. This can be set to `No Operation`, `Trip`, or `Close` accordingly.

For this to work you have to set the ***CB control by*** cell to option 1 `Local`, option 3 `Local + Remote`, option 5 `Opto+Local`, option 7 `Opto+Local+Remote` or option 8 `L/R Key` in the *CB CONTROL* column.

13.6.2 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

13.6.2.1 CIRCUIT BREAKER CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the circuit breaker selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the ***CB Control by*** setting is selected, to option 1 `Local`, option 3 `Local+Remote`, option 5 `Opto+local`, option 7 `Opto+Rem+local` or option 8 `L/R Key` in the *CB CONTROL* column users are allowed to use the Trip and Close Key on the front panel to operate the CB.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***CB control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is green and the REMOTE mode is selected. ***The L/R Key Status*** DDB status is stored in non-volatile memory, so that it's status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant which you require to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the Open or Close key to operate

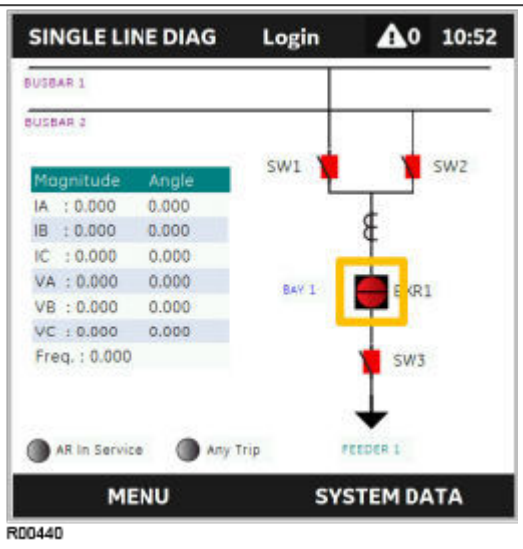


Figure 139: HMI SLD Display

For the Circuit Breaker Commands from HMI, additional checks are done:

If the CB is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "Control by" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "Control by" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "Control by" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - In Remote Control".

If the associated local DDB is set to local, the switchgear command will not be available, and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

13.6.3 CB CONTROL USING THE OPTO-INPUTS

Certain applications may require the use of push buttons or other external signals to control the various CB control operations. It is possible to connect such push buttons and signals to opto-inputs and map these to the relevant DDB signals.

For this to work, you have to set the ***CB control by*** cell to option 4 `opto`, option 5 `Opto+Local`, option 6 `Opto +Remote`, or option 7 `Opto+Local+Remote` in the *CB CONTROL* column.

13.6.4 REMOTE CB CONTROL

Remote CB control can be achieved by setting the ***CB Trip/Close*** cell in the *SYSTEM DATA* column to trip or close by using a command over a communication link.

For this to work, you have to set the ***CB control by*** cell to option 2 `Remote`, option 3 `Local+Remote`, option 6 `Opto+remote`, option 7 `Opto+Local+Remote` or option 8 `L/R Key` in the *CB CONTROL* column.

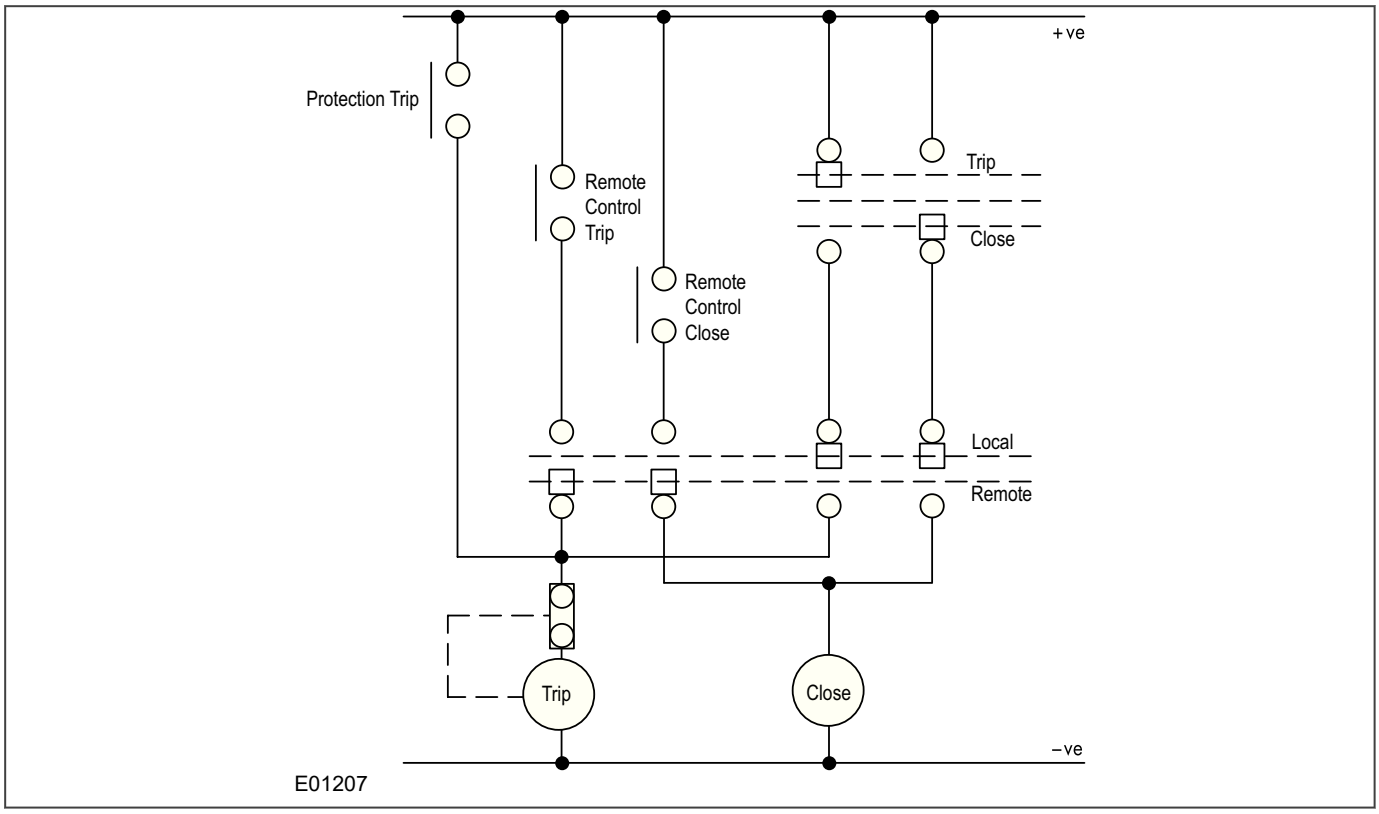


Figure 140: Remote Control of Circuit Breaker

DNP 3.0 protocol: The switch positions can be controlled from Binary Outputs/Control Relay Output Blocks.

IEC 61850 protocol: The CB and switch positions can be controlled in the ‘CSWI’ Logical Node that is linked to the ‘XCBR’ Circuit Breaker Logical Node and 'XSWI' switch Logical Nodes. For Control Authority as per IEC 61850, it is necessary to select ***CB Control by*** cell as option 8 `L/R Key`.

13.6.5 CB HEALTHY CHECK

A CB Healthy check is available if required. This facility accepts an input to one of the opto-inputs to indicate that the breaker is capable of closing (e.g. that it is fully charged). A time delay can be set with the setting ***CB Healthy Time***. If the CB does not indicate a healthy condition within the time period following a Close command, the device will lockout and alarm.

13.6.6 CB CONTROL LOGIC

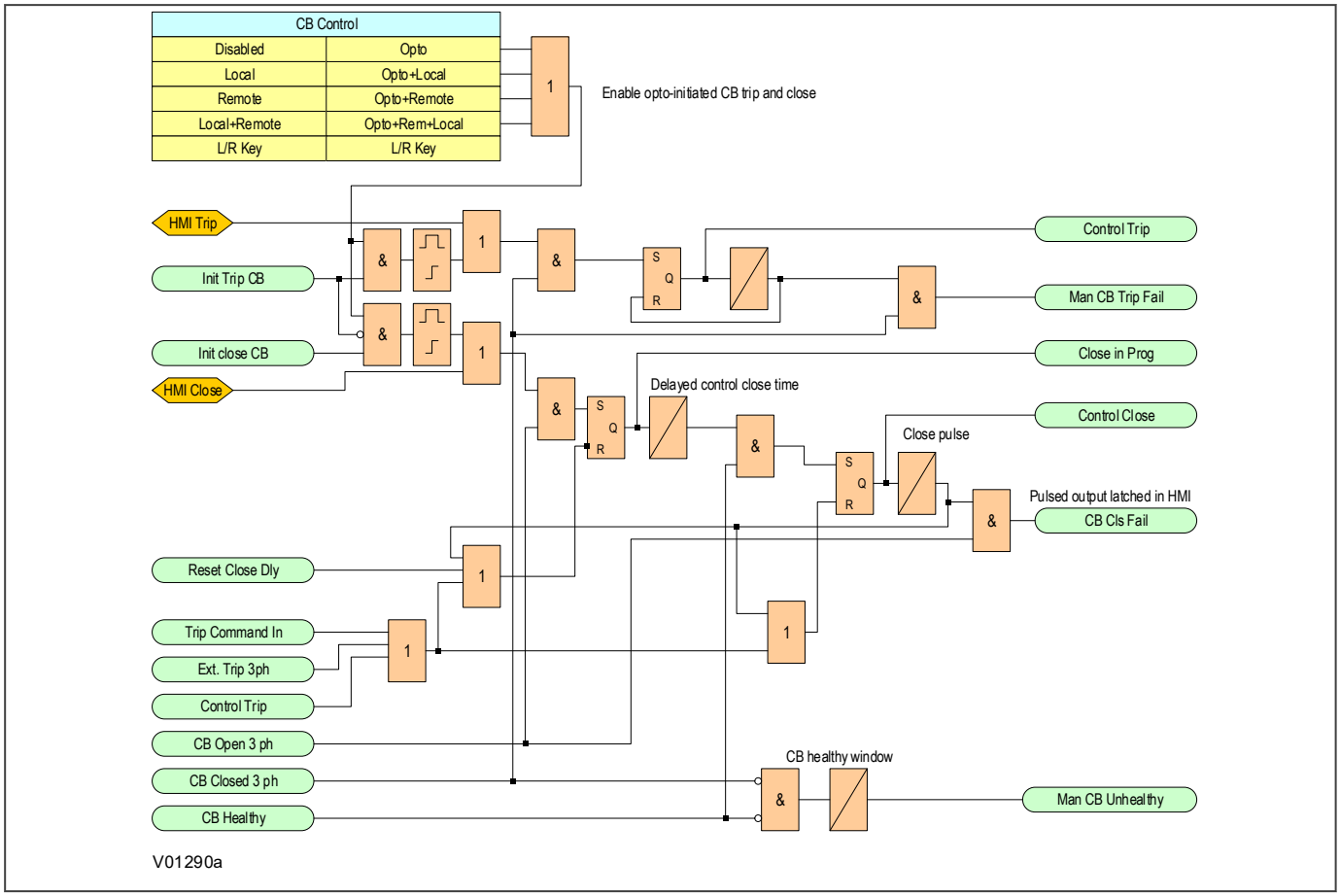


Figure 141: CB control logic

13.7 POLE DEAD FUNCTION

The Pole Dead Logic is used to determine and indicate that one or more phases of the line are not energised. A Pole Dead condition is determined either by measuring:

- the line currents and/or voltages, or
- by monitoring the status of the circuit breaker auxiliary contacts, as shown by dedicated DDB signals.

It can also be used to block operation of underfrequency and undervoltage elements where applicable.

13.7.1 POLE DEAD FUNCTION IMPLEMENTATION

Pole Dead logic can be implemented in all of the P64 models. If implemented in the P642, it requires a model with two single phase VT inputs. If implemented in the P643 or P645, it requires a three phase VT input.

In the P642, the phase -to-phase voltages VAB and VBC are considered, whilst in the P643 and P645, the phase -to-neutral votlages VAN, VBN and VCN are considered.

The pole dead function is used to determine when the circuit breaker poles are open. This indication may be forced, using status indication from CB auxiliary contacts (52a or 52b) mapped to opto-inputs, or internally determined by the device. If internally determined, the 52b contacts are used and inverted in the PSL because only the ***CBx closed*** DDB signal is available for each breaker. The device will also initiate a pole dead condition for the following conditions:

- ***VTS Slow Block*** DDB signal is low,
- The line current and voltage fall below a preset threshold.

This is necessary so that a pole dead indication is still given even when an upstream breaker is opened. The undervoltage and undercurrent thresholds have the following, fixed, pick-up and drop-off levels:

- VA<, VB<, VC<, these level detectors operate on phase voltages and have a fixed setting, Pick-up level = 10 V (Vn = 100/120 V), 40 V (Vn = 380/480 V), Drop Off level = 30 V (Vn = 100/120 V), 120V (Vn = 380/480 V).
- VAB<, VBC<, these level detectors operate on phase-phase voltages and have a fixed setting, Pick-up level = 70 V (Vn = 100/120 V), Drop Off level = 95 V (Vn = 100/120 V).
- IA<, IB<, IC<, these level operate on phase currents and have a fixed setting, Pick-up level = 0.05 In, Drop Off level = 0.055 In.

Note:
If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the device for a correct pole dead indication.

13.7.2 POLE DEAD LOGIC

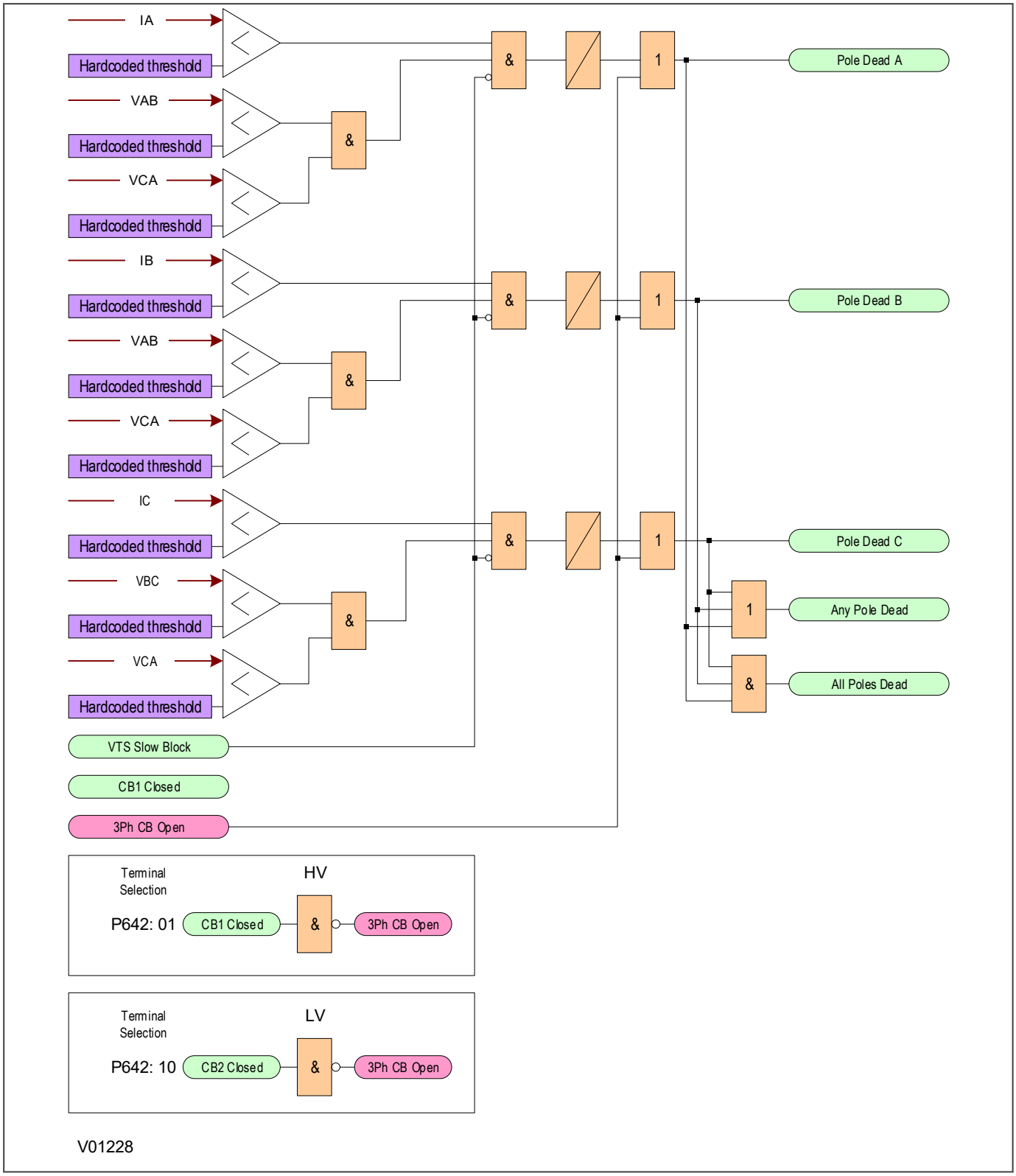


Figure 142: Pole Dead logic - P642

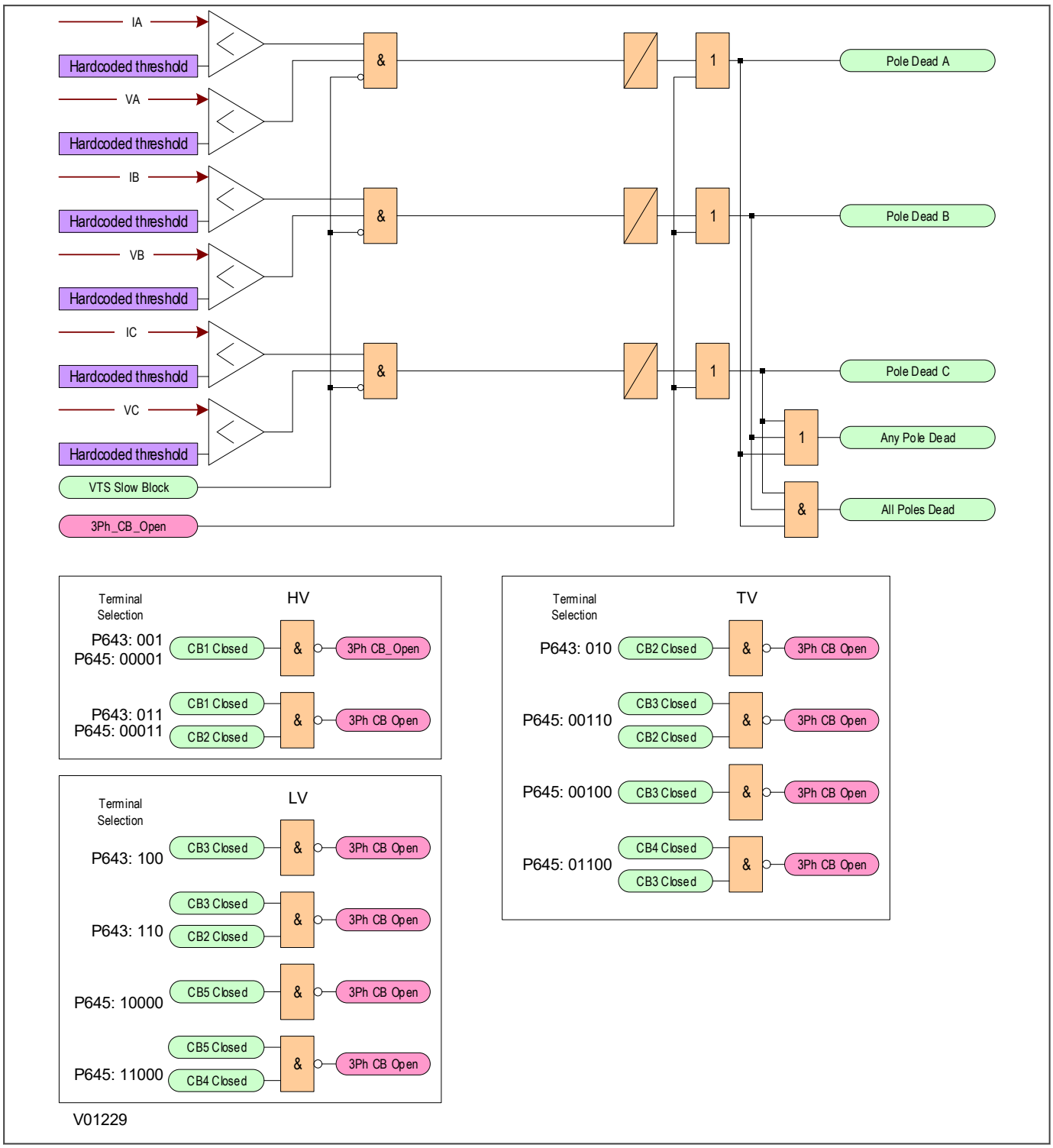


Figure 143: Pole Dead logic - P643 and P645

If both the line current and voltage fall below a certain threshold the device will initiate a Pole Dead condition. The undervoltage (V<) and undercurrent (I<) thresholds are hardcoded internally.

If one or more poles are dead, the device will indicate which phase is dead and will also assert the ***Any Pole Dead*** DDB signal. If all phases are dead the ***Any Pole Dead*** signal would be accompanied by the ***All Poles Dead*** signal.

If the VT fails, a ***VTS Slow Block*** signal is taken from the VTS logic to block the Pole Dead indications that would be generated by the undervoltage and undercurrent thresholds. However, the VTS logic will not block the Pole Dead

indications if they are initiated by a ***CBx Closed*** signal. A ***CBx closed*** signal is inverted and automatically initiates a Pole Dead condition regardless of the current and voltage measurement.

13.7.3 CB STATUS INDICATION

The Pole Dead logic needs a way of initiating the Pole Dead indications for a 3-phase CB Open condition, which bypasses the VTS blocking. This is normally achieved with a CB State Monitoring function. However, the P64 does not contain a dedicated CB state monitoring function, so it needs a mechanism by which to achieve this. To do this, we produce an internal DDB signal (3 ph CB Open), by looking at the status of the CB auxiliary contacts of the windings to which the voltage transformers are connected. Each terminal (T1 to T5) has an external ***CBx Closed*** DDB signal associated with it, which are connected to the CB auxiliary contacts if available. The internal ***3ph CB Open*** indication is produced by ANDing together the statuses of the relevant CBs. This is dependent on the model and the terminal status configuration, and is shown in the logic diagram.

For cases where there are no auxiliary contacts available, the ***CB Open 3 ph*** signal must be forced low to avoid a false Pole Dead indication. You can do this by forcing all five ***CBx Closed*** DDB signals high using opto-inputs as shown below.

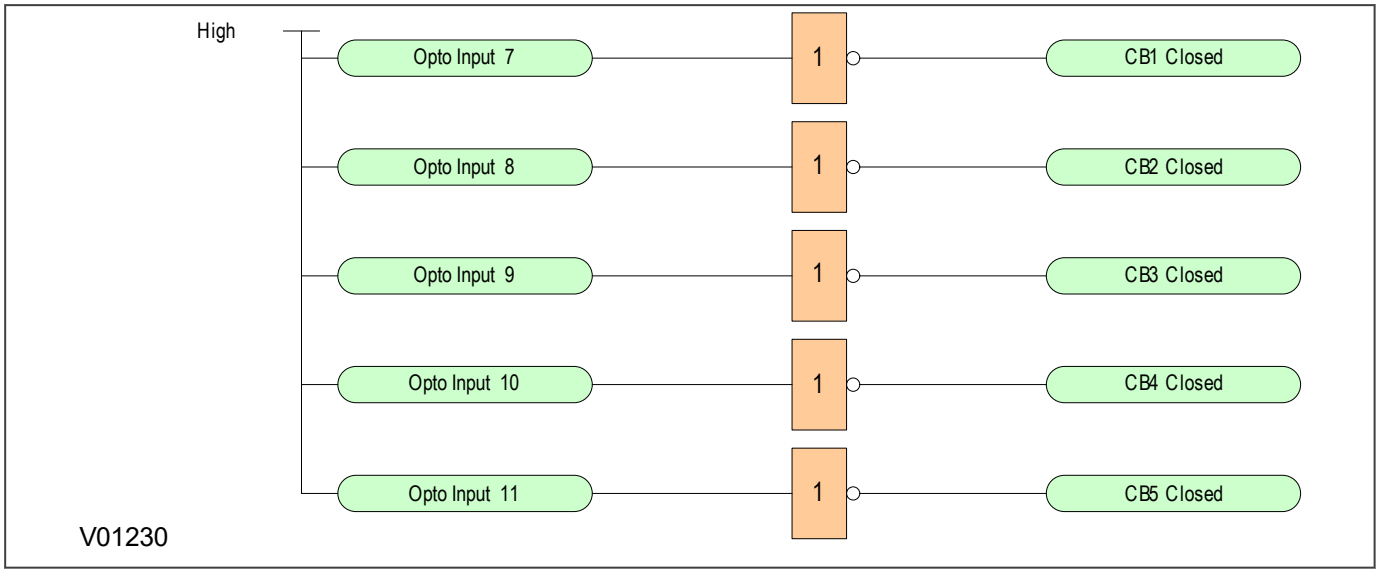


Figure 144: Forcing CB Closed signals

13.8 SWITCH STATUS AND CONTROL

All P64 products support Switch Status and Control for up to 8 switchgear elements. This is available for IEC60870-5-103 and IEC61850 protocols. The device is able to monitor the status of and control up to eight switches. The types of switch that can be controlled are:

- Load Break switch
- Disconnector
- Earthing SwitchP64
- High Speed Earthing Switch

Consider the following feeder bay:

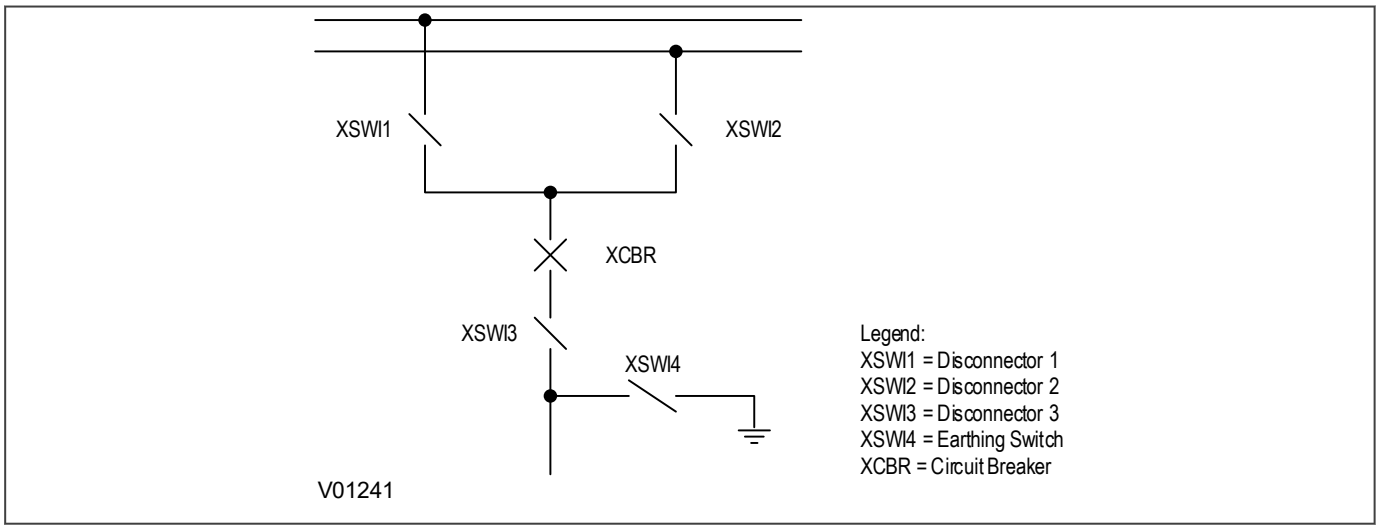


Figure 145: Representation of typical feeder bay

This bay shows four switches of the type LN XSWI and one circuit breaker of type LN XCBR. In this example, the switches XSWI1 – XSWI3 are disconnectors and XCSWI4 is an earthing switch.

For the device to be able to control the switches, the switches must provide auxiliary contacts to indicate the switch status. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers.

There are eight sets of settings in the *SWITCH CONTROL* column, which allow you to set up the Switch control, one set for each switch. These settings are as follows:

SWITCH1 Type

This setting defines the type of switch. It can be a load breaking switch, a disconnector, an earthing switch or a high speed earthing switch.

SWI1 Status Inpt

This setting defines the type of auxiliary contacts that will be used for the control logic. For convenience, the device settings refer to the auxiliary contacts as 52A and 52B, even though they are not circuit breakers. "A" contacts match the status of the primary contacts, whilst "B" contacts are of the opposite polarity.

SWI1 Control by

This setting determines how the switch is to be controlled. This can be Local (using the device directly) remote (using a communications link), or both.

SWI1Trip/Close

This is a command t o directly trip or close the switch.

SWI1 Trp Puls T and ***SWI1 Cls Puls T***

These settings allow you to control the width of the open and close pulses.

SWI1 Sta Alrm T

This setting allows you to define the duration of wait timer before the relay raises a status alarm.

SWI1 Trp Fail T and ***SWI1 Cls Fail T***

These settings allow you to control the delay of the open and close alarms when the final switch status is not in line with expected status.

SWI1 Operations

This is a data cell, which displays the number of switch operations that have taken place. It is an accumulator, which you can reset using the ***Reset SWI1 Data*** setting

Reset SWI1 Data

This setting resets the switch monitoring data.

Note:
Settings for switch 1 are shown, but settings for all other switch elements are the same.

IEC 61850 protocol: The Switch position can be controlled in the 'CSWI' Logical Node that is linked to the 'XSWI' Switch Logical Node. For Control Authority as per IEC 61850, it is necessary to select ***SWx Control by*** cell as option 4 L/R Key.

13.8.1 SINGLE LINE DIAGRAM (SLD) VIEWER

The SLD menu displays the saved SLD on the graphical HMI screen. You can navigate to the SLD menu using the bottom Menu context keys or by using the quick launch menu on the Home page. The SLD is configured and uploaded into the IED using the S1 Agile configuration tool. Items of plant can be selected on the SLD screen using the navigation keypad.

13.8.2 SWITCH CONTROL (SLD VIEW ONLY)

You can OPEN and CLOSE the switches selected on the SLD using the dedicated OPEN, CLOSE and L/R buttons on the front HMI Panel.

When the Switch Control by setting is selected to option 1 *LOCAL*, option 3 `Local+Remote` or option 4 `L/R Key` in the SWITCH CONTROL column, users are allowed to use the Open and Close Key on the front panel to operate the SWITCH.

To control an item of plant using the Open and Close and L/R buttons:

- Set ***Switch Control by*** setting to `L/R Key`
- Select the Local operating mode by pressing the L/R button

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is green and the REMOTE mode is selected. The **L/R Key Status** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

- In the SLD menu, navigate to the item of plant you want to control using the navigation keypad
- The selected plant is highlighted with an orange border
- Use the Enter key to select the item
- Press the OPEN or CLOSE key to operate

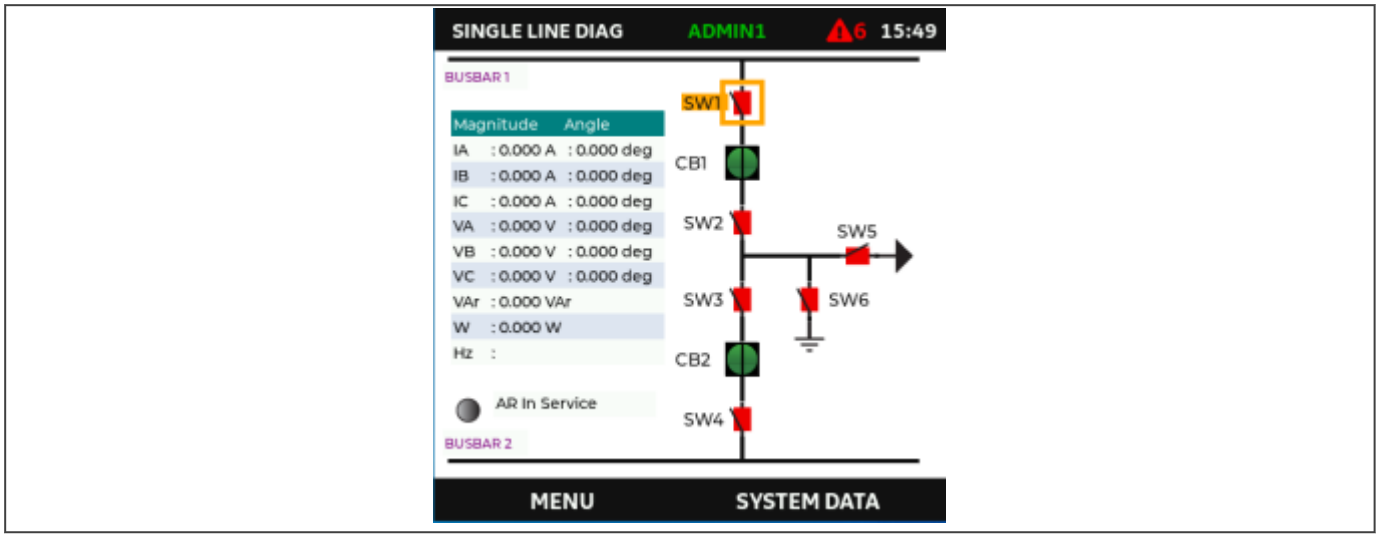


Figure 146: HMI SLD display

Figure 147: For the Switch Commands from HMI, these additional checks are done:

If the Switch is in indeterminant state, the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked - Intermediate State".

If the associated "***Control by***" setting is set to "disabled" the switchgear command will not be available and HMI will raise a warning dialogue with the message - "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "remote" the switchgear command will not be available and HMI will raise a warning dialogue with the message "Commands blocked due to Settings".

If the associated "***Control by***" setting is set to "L/R key" and soft key status is set to remote, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - In Remote Control."

If the associated local DDB is set to local, the switchgear command will not be available and HMI will pop-up the message - "Commands blocked - Switchgear in Local".

13.8.3 SWITCH CONTROL LOGIC

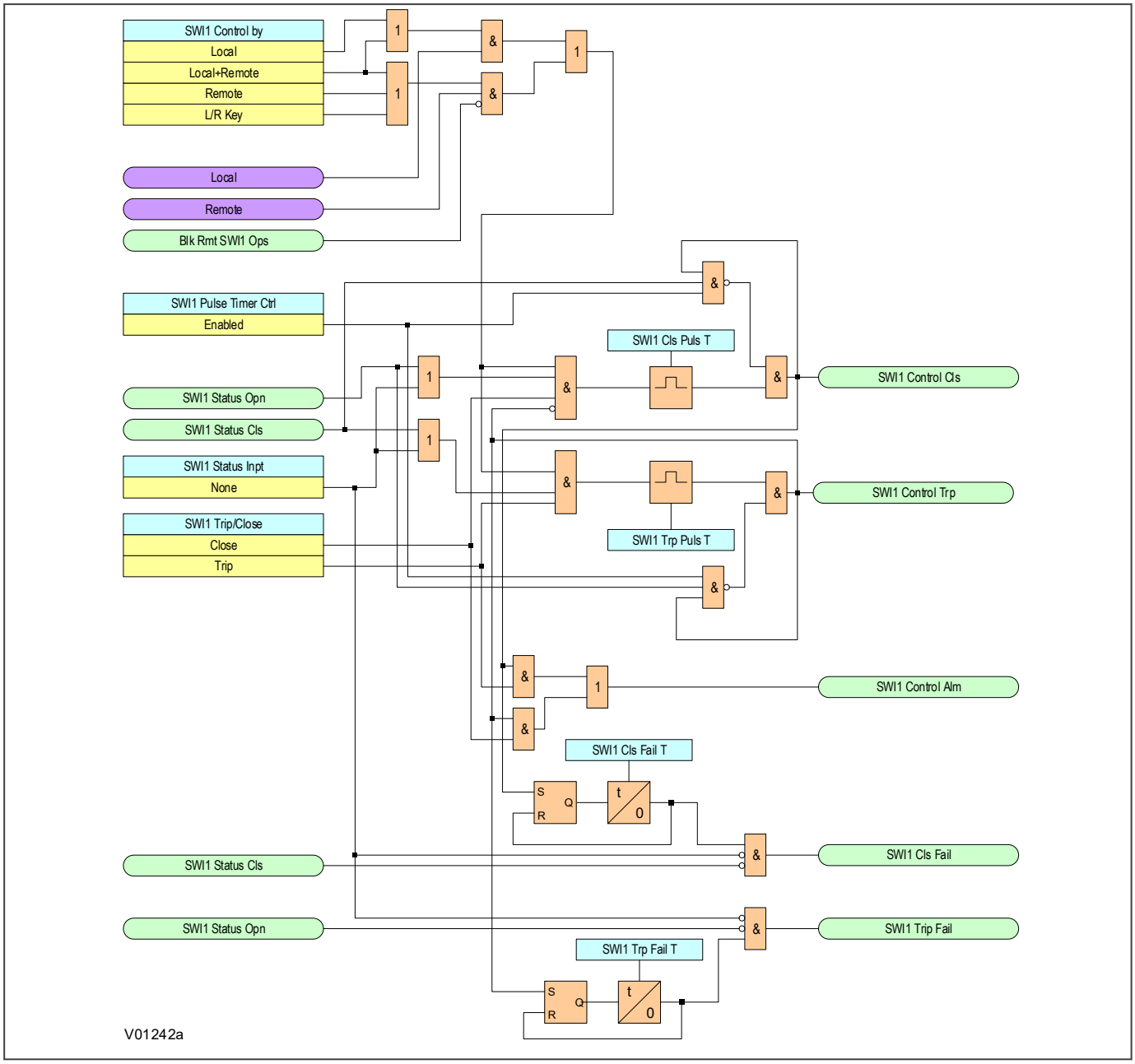


Figure 148: Switch control logic

13.8.4 SWITCH STATUS LOGIC

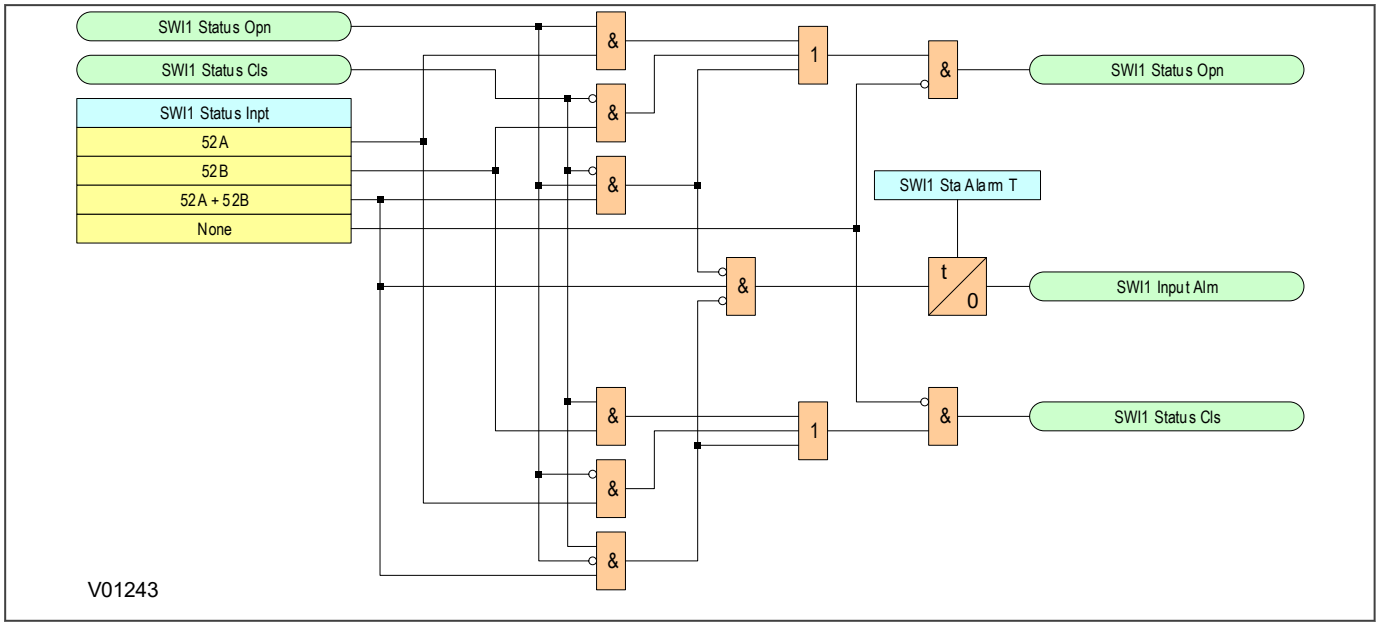


Figure 149: Switch status logic

13.9 TEST MODE

The behaviour of the IED is dependant on if it is in normal operation or in one of the Test Modes. This is reflected in some of the data that can be monitored and affects the allowed control operations, particularly using the IEC 61850 protocol.

The mode of operation is set using the ***IED Test Mode*** cell under the *COMMISSION TESTS* column. See the Commissioning Instructions chapter for more information.

When the IED is in either ***Test*** or ***Contacts Blocked*** mode, IEC 61850 status and measurement data will be transmitted with its quality parameter set to ***test***, so that the receiver understands that they have been issued by a device under test and can respond accordingly.

When the IED is in either ***Test*** or ***Contacts Blocked*** mode, the IED only responds to IEC 61850 MMS controls from the client with the 'test' flag set (with the exception of controls on System/LLN0.Mod).

You can select the mode of operation of the P40 IED by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column
- Using an IEC 61850 MMS control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the P40 IED behaviour under the different modes:

IED Test Mode Setting	IEC 61850 Mod	Result
Disabled	on	• Normal IED behaviour • IED only responds to incoming GOOSE and SV messages with quality q.test = false
Test	test	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are still active • IEC 61850 message outputs have 'quality' q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true
Contacts Blocked	test/blocked	• Protection remains enabled • IED responds to incoming GOOSE and SV messages with both quality q.test = true and q.test = false • Relay output contacts are disabled • IEC 61850 message outputs have quality q.test = true • IED responds to incoming IEC 61850 MMS messages with only quality q.test = true

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

13.10 IEC 61850 CONTROL AUTHORITY

Within the substation, control commands to the primary equipment, such as the breaker or disconnect/earth switches can be originated from one of four levels: Device, Bay, Station or Remote.

Device: Controls are issued manually at the device in the yard/GIS. Any commands from remote locations are not accepted. For this to happen the XCBR/XSWI.Loc object should be True. For P40 devices, the XCBR/XSWI.Loc is mapped to these DDBs:

DDB No.	DDB Name	Description
2186	LocKey Local	This DDB signal indicates that the IED is in local status
2187	SW1 Local	This DDB signal indicates that the switch 1 is in local status
2188	SW2 Local	This DDB signal indicates that the switch 2 is in local status
2189	SW3 Local	This DDB signal indicates that the switch 3 is in local status
2190	SW4 Local	This DDB signal indicates that the switch 4 is in local status
2191	SW5 Local	This DDB signal indicates that the switch 5 is in local status
2192	SW6 Local	This DDB signal indicates that the switch 6 is in local status
2193	SW7 Local	This DDB signal indicates that the switch 7 is in local status
2194	SW8 Local	This DDB signal indicates that the switch 8 is in local status
2195	CB1 Local	This DDB signal indicates that the CB1 is in local status
2196	CB2 Local	This DDB signal indicates that the CB2 is in local status
2197	CB3 Local	This DDB signal indicates that the CB3 is in local status
2198	CB4 Local	This DDB signal indicates that the CB4 is in local status
2199	CB5 Local	This DDB signal indicates that the CB4 is in local status

If the DDBs associated are not connected, the default is False which facilitates remote operations.

Bay: The commands are issued from the HMI of the P40. The P40 has a dedicated L/R Button for selection in the front face.

Key	Description	Function
	Local/Remote key	To select between local and remote operating modes.

When the L/R button on the front panel is pressed, it will toggle the status of DDB ***L/R Key Status***. When the DDB status is TRUE, the L/R Key LED is Red and the Local mode is selected. When the DDB status is FALSE, the L/R Key LED is Green and the REMOTE mode is selected. The ***L/R Key Status*** DDB status is stored in non-volatile memory, so that its status is recovered after an IED power cycle.

Bay Level controls are possible from the HMI if the ***L/R Key Status*** is in Local. When L/R Key is in Local the IEC 61850 Signal, System\LLN0.Loc is set as True. When L/R Key is in Remote, and a control action is attempted, the User will be advised with a pop-up message of "Command Unavailable - in remote".

To facilitate integration of the IED into a wired Local/Remote control switch in a panel, an additional DDB L/R Key has been provided.

This is modelled into IEC 61850 System\LLN0.LocKey. The data object LocKey represents the status of a physical key switch and allows taking over the control authority, if the DDB is wired. If the DDB is used, and is set to 1, the IED Local/Remote (System\LLN0.Loc) automatically changes to Local. At this stage, it is not possible to change the

IED L/R Key to remote. If the DDB is set to 0, the IED L/R does not automatically change to Remote. If necessary, a user action is required to change the control authority to Remote.

Station/Remote: Station level commands are those originating from either the substation gateway or from the station HMI. Remote commands are from the remote Network Control Center (NCC).

The data object LocSta modelled in System\LLN0 shows the control authority at station level. If LocSta=True, control authority is at station level and control from remote is disabled. If LocSta=False, control commands are allowed from remote, e.g. network control center (NCC).

P40 devices also support the concept of Multiple Level Control authority. This is done via a dedicated datapoint in System\LLN0 known as MltLev. If true, authority control from multiple levels is allowed, otherwise no other control level is allowed.

Under certain operational conditions, such as during maintenance, it is necessary to block commands from one or more of these levels. The local/remote control feature (described in IEC 61850 7-4: Annex B) allows users to enable or disable control authority from one or more of the three levels, as illustrated in the tables below:

IEC 61850 commands originating from the various levels are differentiated using the Origin.OrCat attribute value in the IEC 61850 command.

If the control command is rejected by the P40 IED due to control authority check, the AddCause - Blocked-by-switching-hierarchy will be shown in the IEC 61850 Client.

Control Authority for Other Controllable Objects								
Device	**Switch**	**Bay Control**			**Manual Control at Front Panel**	**Command From**		
		Mode of Switching Authority for Local Control	**Local Control Behaviour**	**Control Authority at Station Level**		**OrCat**		
LLN0.Loc Key	**XCBR.Loc XWI.Loc**	**LLN0.Mlt Lev**	**CSWI.Loc**	**CSWI.Loc Sta**		**Bay**	**Station**	**Remote**
T	n.a.	F	n.a.	n.a.	AA	NA	NA	NA
F	T	F	T	n.a.	AA	NA	NA	NA
F	T	F	F	n.a.	NA	NA	NA	NA
F	F	F	T	n.a.	AA	NA	NA	NA
F	F	F	F	T	NA	NA	AA	NA
F	F	F	F	F	NA	NA	NA	AA
T	n.a.	T	n.a.	n.a.	AA	NA	NA	NA
F	T	T	T	n.a.	AA	NA	NA	NA
F	T	T	F	n.a.	NA	NA	NA	NA
F	F	T	T	n.a.	AA	NA	NA	NA
F	F	T	F	T	NA	AA	AA	NA
F	F	T	F	F	NA	AA	AA	AA

n.a. - Not Applicable
AA - Always Allowed
NA - Not Allowed

In addition to the CB/Switches, P40 devices follow the concept of Control Authority for other commands executed via IEC 61850. These include:

- Control Inputs
- Reset of Trip LED
- Enable/Disable of Protection, Check Sync and Auto Recloser
- Reset of demands and thermal measurements

Control Authority for Other Controllable Objects							
Device	Bay Control			Manual Control at Front Panel	Command From		
	Mode of Switching Authority for Local Control	Local Control Behaviour	Control Authority at Station Level		OrCat		
LLN0.Loc Key	LLN0.Mlt Lev	LLN0.Loc	LLN0.Loc Sta		Bay	Station	Remote
T	F	n.a.	n.a.	AA	NA	NA	NA
F	F	T	n.a.	AA	NA	NA	NA
F	F	F	T	AA	NA	AA	NA
F	F	F	F	AA	NA	NA	AA
T	T	n.a.	n.a.	AA	NA	NA	NA
F	T	T	n.a.	AA	NA	NA	NA
F	T	F	T	AA	AA	AA	NA
F	T	F	F	AA	AA	AA	AA
n.a. - Not Applicable AA - Always Allowed NA - Not Allowed							

IEC 61850 based control authority can be visualized from the P40 HMI.

This is under the COMMISSION TESTS Menu, under IEC 61850 Control Sub Menu:

Menu Text	Description	Min	Max	Default	Controllable
Multiple Level	Used to enable/disable the 'multi level control authority' feature for breaker/switch and other controls	Disabled	Enabled	Disabled	Yes
Station Level	Used to get control command of station authority from IEC 61850 Client	Disabled	Enabled	Disabled	No
Device Level	Used to show the IED local/remote status	Local	Remote	Local	No

Multiple Level Control Authority can be selected either via an IEC 61850 MMS Command or via selection from the menu item shown above.

Note:
The Control Authority only works if the Protocol is IEC 61850. For Legacy Protocols, the existing control mechanism remains.

Note:
For Control Authority for CB/Switches, it is mandatory to select the option of L/R for CB/Switches if IEC 61850 is used.

CHAPTER 14

SUPERVISION

14.1 CHAPTER OVERVIEW

This chapter describes the supervison functions.

This chapter contains the following sections:

Chapter Overview 308
Voltage Transformer Supervision 309
Current Transformer Supervision 314
Trip Circuit Supervision 318

14.2 VOLTAGE TRANSFORMER SUPERVISION

The Voltage Transformer Supervision (VTS) function is used to detect failure of the AC voltage inputs to the protection. This may be caused by voltage transformer faults, overloading, or faults on the wiring, which usually results in one or more of the voltage transformer fuses blowing.

If there is a failure of the AC voltage input, the IED could misinterpret this as a failure of the actual phase voltages on the power system, which could result in unnecessary tripping of a circuit breaker.

The VTS logic is designed to prevent such a situation by detecting voltage input failures, which are NOT caused by power system phase voltage failure, and automatically blocking associated voltage dependent protection elements. A time-delayed alarm output is available to warn of a VTS condition.

The following scenarios are possible with respect to the failure of the VT inputs.

- Loss of one or two-phase voltages
- Loss of all three-phase voltages under load conditions
- Absence of three-phase voltages upon line energisation

14.2.1 LOSS OF ONE OR TWO PHASE VOLTAGES

If the power system voltages are healthy, no Negative Phase Sequence (NPS) current will be present. If however, one or two of the AC voltage inputs are missing, there will be Negative Phase Sequence voltage present, even if the actual power system phase voltages are healthy. VTS works by detecting Negative Phase Sequence (NPS) voltage without the presence of Negative Phase Sequence current. So if there is NPS voltage present, but no NPS current, it is certain that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

14.2.2 LOSS OF ALL THREE PHASE VOLTAGES

If all three voltage inputs are lost, there will be no Negative Phase Sequence quantities present, but the device will see that there is no voltage input. If this is caused by a power system failure, there will be a step change in the phase currents. However, if this is not caused by a power system failure, there will be no change in any of the phase currents. So if there is no measured voltage on any of the three phases and there is no change in any of the phase currents, this indicates that there is a problem with the voltage transformers and a VTS block should be applied to voltage dependent protection functions to prevent maloperation.

14.2.3 ABSENCE OF ALL THREE PHASE VOLTAGES ON LINE ENERGISATION

On line energization there should be a change in the phase currents as a result of loading or line charging current. Under this condition we need an alternative method of detecting three-phase VT failure.

If there is no measured voltage on all three phases during line energization, two conditions might apply:

- A three-phase VT failure
- A close-up three-phase fault.

The first condition would require VTS to block the voltage-dependent functions.

In the second condition, voltage dependent functions should not be blocked, as tripping is required.

To differentiate between these two conditions overcurrent level detectors are used (***VTS I> Inhibit*** and ***VTS I2> Inhibit***). These prevent a VTS block from being issued in case of a genuine fault. These elements should be set in excess of any non-fault based currents on line energisation (load, line charging current, transformer inrush current if applicable), but below the level of current produced by a close-up three-phase fault.

If the line is closed where a three-phase VT failure is present, the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three-phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

14.2.4 VTS IMPLEMENTATION

Voltage Transformer Supervision is usually used with devices with a 3-phase voltage input, such as the P643 and P645 with the optional 3phase VT input. it can however be implemented in a P642, but only if you have ordered a model with 2-VT inputs, and if the VTs are configured as shown in the wiring diagrams.

VTS is implemented in the *SUPERVISION* column of the relevant settings group, under the sub-heading *VT SUPERVISION*.

The following settings are relevant for VT Supervision:

- ***VTS Status***: determines whether the VTS Operate output will be a blocking output or an alarm indication only
- ***VTS Reset Mode***: determines whether the Reset is to be manual or automatic
- ***VTS Time delay***: determines the operating time delay
- ***VTS I> Inhibit***: inhibits VTS operation in the case of a phase overcurrent fault
- ***VTS I2> Inhibit***: inhibits VTS operation in the case of a negative sequence overcurrent fault

VTS is only enabled during a live line condition (as indicated by the pole dead logic) to prevent operation under dead system conditions.

14.2.5 VTS LOGIC

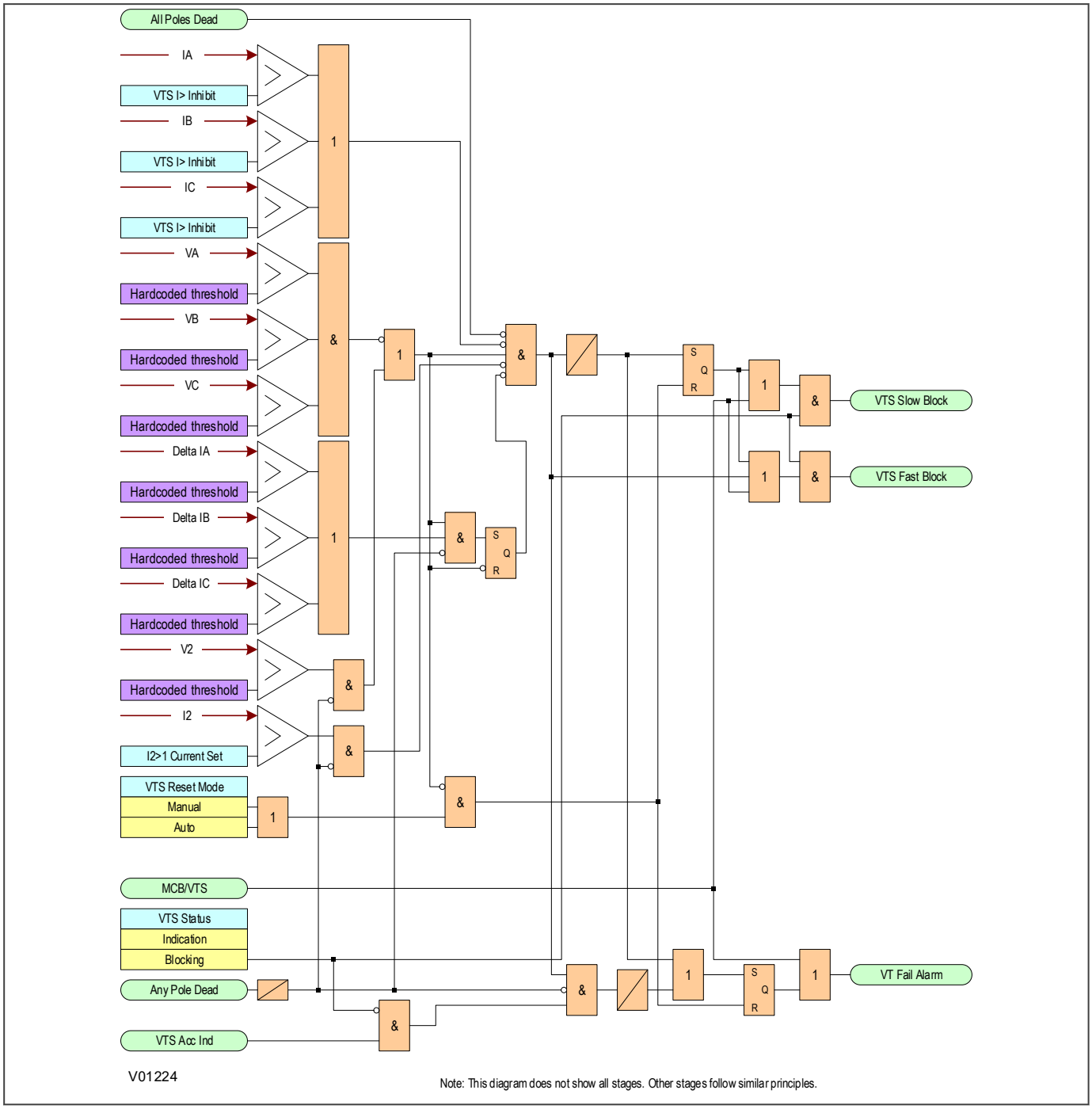


Figure 150: VTS logic (P642 with 2 single-phase VTs)

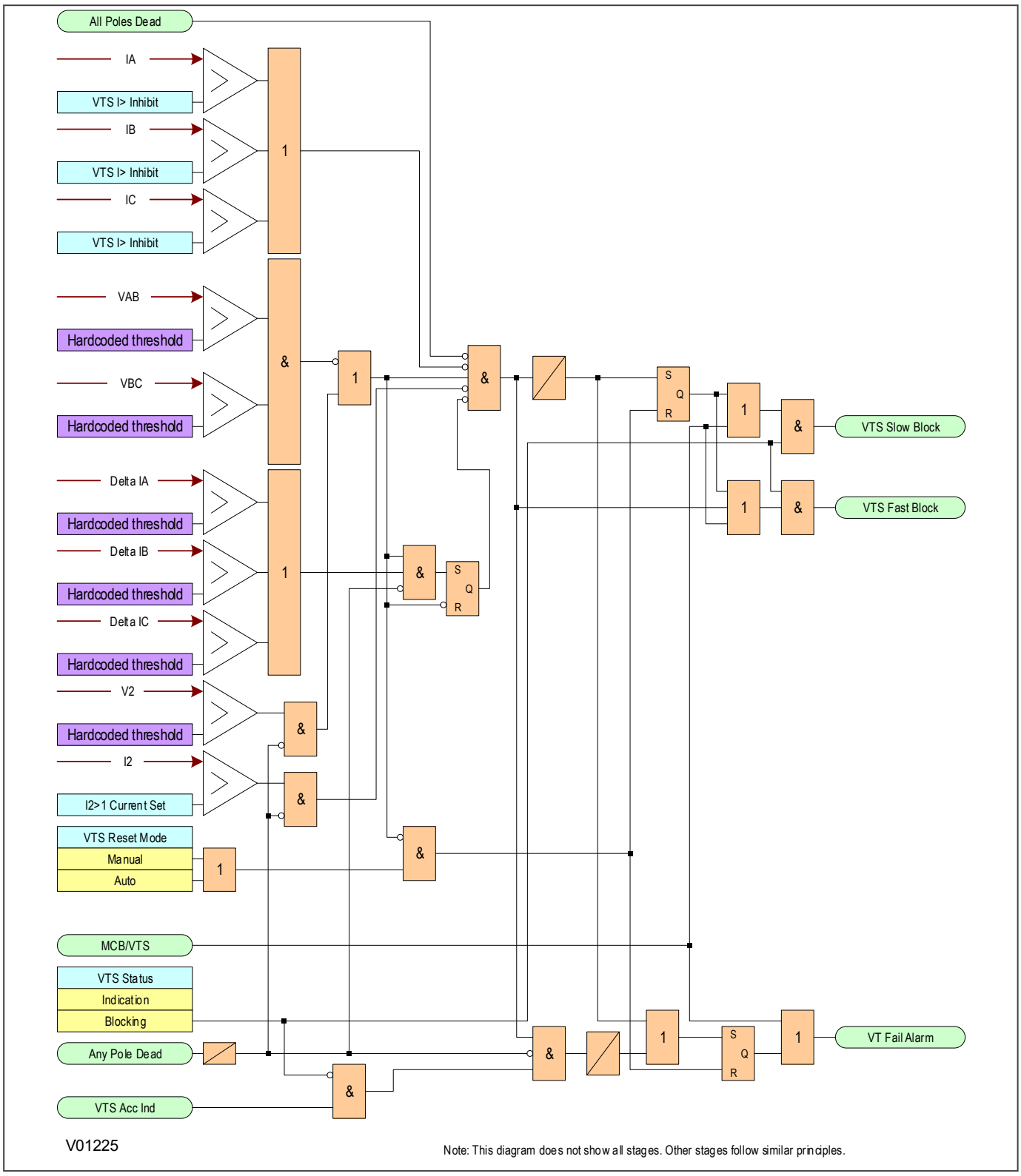


Figure 151: VTS logic (P643 and P645 with 3-phase VTs)

For the P643 and P645, a 3-phase VT is used and each of the input voltages VA, VB and VC are with respect to earth. For the P642, two single-phase VTs are used and the two input voltages VA and VB are phase-to-phase voltages

As can be seen from the diagram, the VTS function is inhibited if:

- An ***All Poles Dead*** DDB signal is present
- A phase overcurrent condition exists
- A Negative Phase Sequence current exists
- If the phase current changes over the period of 1 cycle

The VTS will operate if:

- All three of the input voltages are lower than the VTS Pickup threshold AND the function is not inhibited by any of the above criteria
- Negative Sequence Voltage is present AND the function is not inhibited by any of the above criteria

The NPS voltage and current detection criteria (used for the case when one or two voltage inputs are lost) is inhibited if an Any Pole Dead signal is present.

14.3 CURRENT TRANSFORMER SUPERVISION

The Current Transformer Supervision function (CTS) is used to detect failure of the AC current inputs to the protection. This may be caused by internal current transformer faults, overloading, or faults on the wiring. If there is a failure of the AC current input, the protection could misinterpret this as a failure of the actual phase currents on the power system, which could result in maloperation. Also, an open circuit in the AC current circuits can cause dangerous CT secondary voltages to be generated.

14.3.1 CTS IMPLEMENTATION

Differential current transformer supervision is based on the measurement of the ratio of negative sequence current to positive sequence current (I2/I1) for each CT. When this ratio is not zero, one of the following two conditions may be present:

- There is an unbalanced fault
- There is a 1 or 2 phase CT problem

If the I2/I1 ratio is greater than the high set value, ***CTS I2/I1>2*** at all ends, it is almost certainly a genuine fault condition, thus the CTS will not operate. If this ratio is detected at one end only, one of the following conditions may be present:

- A CT problem
- A single end fed fault condition

The positive sequence current I1 is used to confirm whether it is a CT problem or not. If I1 is greater than the setting ***CTS I1*** at all terminals, it must be a CT problem and CTS is allowed to operate. If this condition is detected at only one end, the device assumes it is caused by either an inrush condition or a single-end fed internal fault. In this case, CTS operation is blocked.

The ***CTS status*** setting under the *CT SUPERVISION* sub-heading can be set to either `indication` or `restraint`. In indication mode, the CTS alarm time delay is automatically set to zero. If a CT failure is present, an alarm would be issued without delay, but the differential protection would remain unrestricted. In restraint mode, the differential protection is blocked for 20 ms after CT failure has been detected, after which the restraint region of the bias characteristic increases according to the setting ***Is-CTS*** , which has been defined in the *DIFF PROTECTION* column.

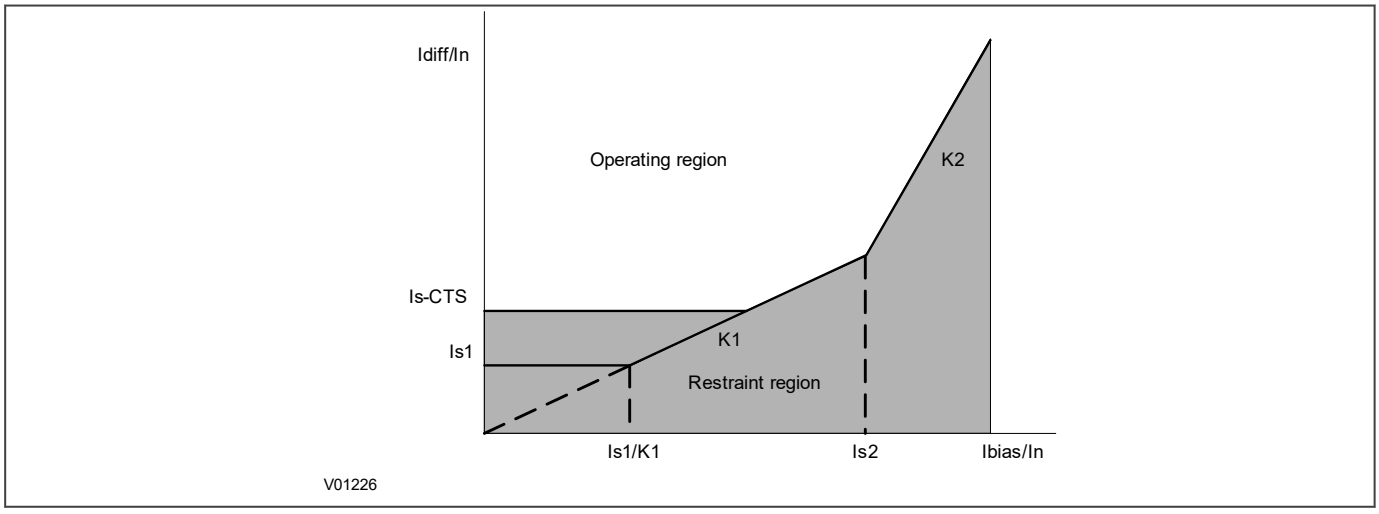


Figure 152: CTS restraint region increase

The low impedance REF, earth fault and NPS overcurrent protection functions are internally blocked by CTS when a CT failure is detected in the relevant CT. However, earth fault protection is immune to CTS blocking if ***IN> input*** is set to measured.

The CTS monitors the positive and negative sequence currents of all CTs (2 to 5, depending on the model). A faulty CT is determined if the following conditions are present at the same time:

- The positive sequence current in at least two current inputs exceeds the set release threshold I1 (***CTS I1*** setting under the *SUPERVISON* column). This also means that CTS can only operate if minimum load current of the protected object is present.
- A high set ratio of negative to positive sequence current, ***CTS I2/I1>2***, is exceeded at one end.
- At all other ends the ratio of negative to positive sequence current is less than a low set value, ***CTS I2/I1> 1***, or no significant current is present (positive sequence current is below the release threshold I1).

Only a single or double phase CT failure can be detected by this logic. The probability of symmetrical three-phase CT failures is very low, therefore in practice this is not a significant problem.

14.3.2 CTS LOGIC

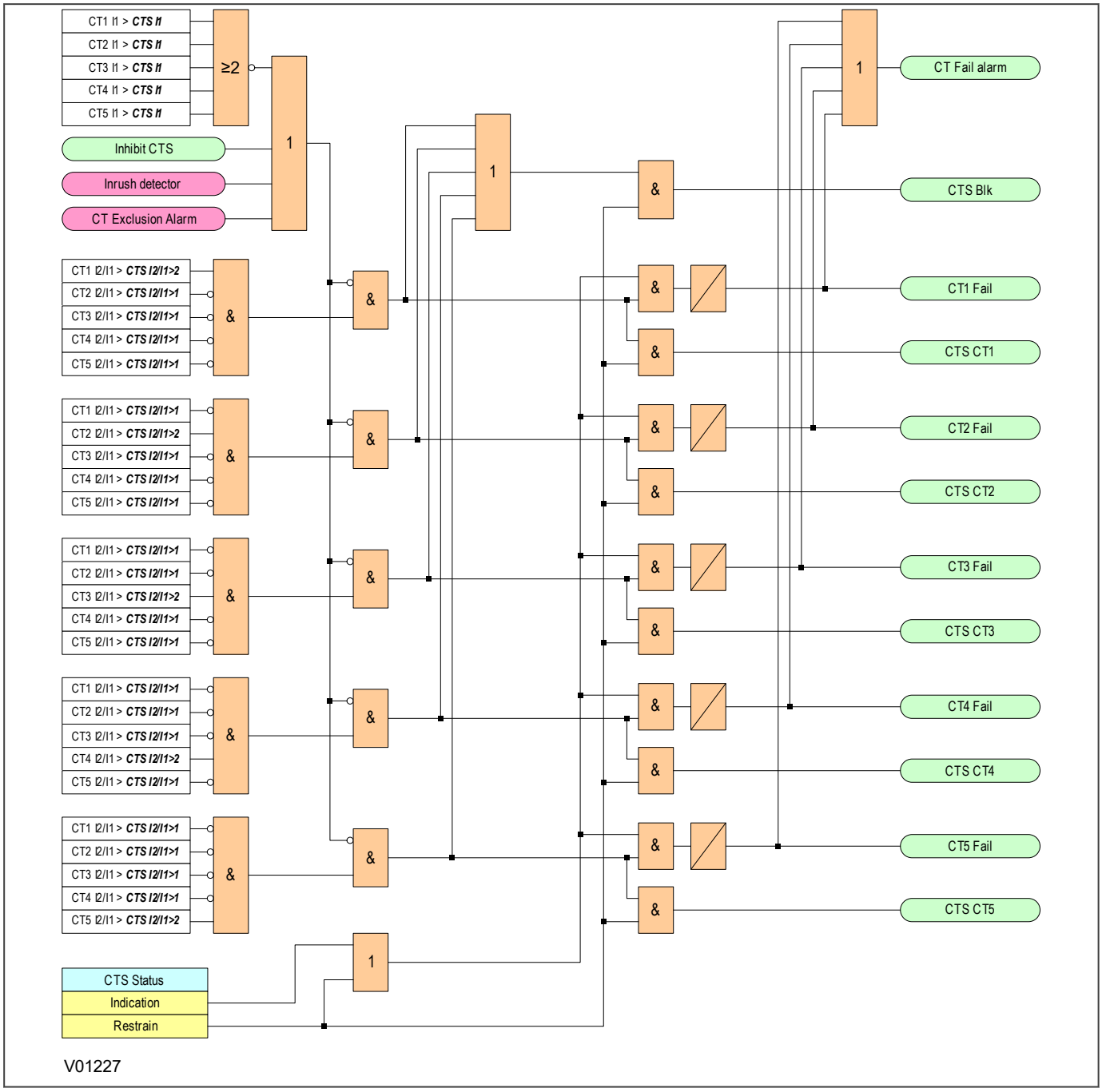


Figure 153: CTS logic diagram

14.3.3 APPLICATION NOTES

14.3.3.1 SETTING GUIDELINES

The positive sequence current in at least two current inputs exceeds the ***CTS I1*** setting. The ***CTS I1*** setting should be below the minimum load current of the protected object. Therefore, 10% of the rated current might be used.

The high set ratio of negative to positive sequence current, ***CTS I2/I1>2***, should be set below the ratio of negative sequence to positive sequence current for the minimum unbalanced fault current. When the balanced full load current is flowing and the secondary of Phase A CT1 is disconnected, the currents measured by the device are:

$I_A = 0$

$I_B = 1 \angle -120°$

$I_C = 1 \angle -240°$

The positive and negative sequence currents are calculated as:

$$I_1 = \left|\frac{1}{3}\left(I_A + aI_B + a^2 I_C\right)\right| = \frac{2}{3}$$

$$I_1 = \left|\frac{1}{3}\left(I_A + a^2 I_B + aI_C\right)\right| = \frac{1}{3}$$

The ratio of negative to positive sequence current is 50%, therefore a typical setting of 40% might be used.

The low set ratio of negative to positive sequence current, ***CTS I2/I1>1***, should be set above the maximum load unbalance. In practise, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the device's measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for. A 20% setting might be used.

If the following information is recorded by the relay during commissioning:

$I_{\text{full load}} = 500$ A

$I_2 = 50$ A

Therefore I2/I1 ratio is given by I2/I1 = 50/500 = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical. Therefore set ***CTS I2/I1>1*** = 20%.

Due to the sensitive settings suggested above, a long time delay is necessary to ensure a true CT failure. We recommend using the default setting for this time time delay. After the CTS Time Delay expires (***CTS Time Delay***), the ***CTS Fail Alarm*** is asserted.

14.4 TRIP CIRCUIT SUPERVISION

In most protection schemes, the trip circuit extends beyond the IED enclosure and passes through components such as links, relay contacts, auxiliary switches and other terminal boards. Such complex arrangements may require dedicated schemes for their supervision.

There are two distinctly separate parts to the trip circuit; the trip path, and the trip coil. The trip path is the path between the IED enclosure and the CB cubicle. This path contains ancillary components such as cables, fuses and connectors. A break in this path is possible, so it is desirable to supervise this trip path and to raise an alarm if a break should appear in this path.

The trip coil itself is also part of the overall trip circuit, and it is also possible for the trip coil to develop an open-circuit fault.

This product supports a number of trip circuit supervision (TCS) schemes.

14.4.1 TRIP CIRCUIT SUPERVISION SCHEME 1

This scheme provides supervision of the trip coil with the CB open or closed, however, it does not provide supervision of the trip path whilst the breaker is open. The CB status can be monitored when a self-reset trip contact is used. However, this scheme is incompatible with latched trip contacts, as a latched contact will short out the opto-input for a time exceeding the recommended Delayed Drop-off (DDO) timer setting of 400 ms, and therefore does not support CB status monitoring. If you require CB status monitoring, further opto-inputs must be used.

Note:
A 52a CB auxiliary contact follows the CB position. A 52b auxiliary contact is the opposite.

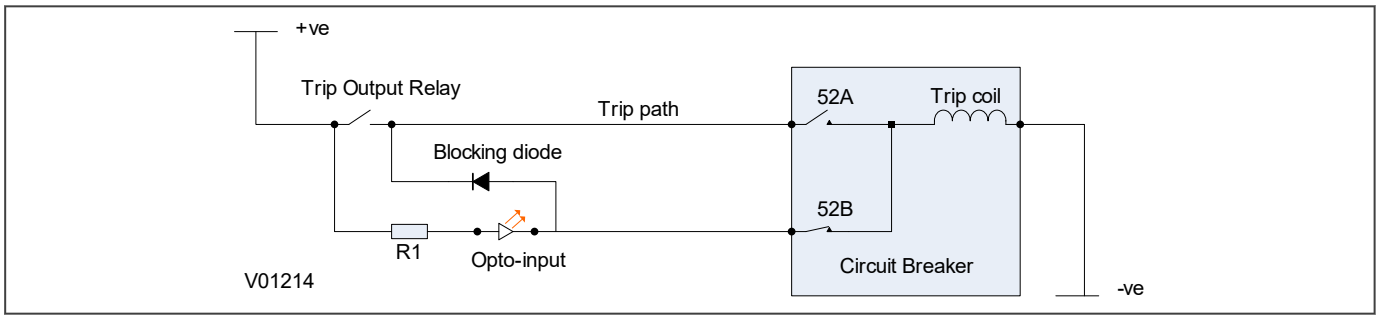


Figure 154: TCS Scheme 1

When the CB is closed, supervision current passes through the opto-input, blocking diode and trip coil. When the CB is open, supervision current flows through the opto-input and into the trip coil via the 52b auxiliary contact. This means that *Trip Coil* supervision is provided when the CB is either closed or open, however *Trip Path* supervision is only provided when the CB is closed. No supervision of the trip path is provided whilst the CB is open (pre-closing supervision). Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

14.4.1.1 RESISTOR VALUES

The supervision current is a lot less than the current required by the trip coil to trip a CB. The opto-input limits this supervision current to less than 10 mA. If the opto-input were to be short-circuited however, it could be possible for the supervision current to reach a level that could trip the CB. For this reason, a resistor R1 is often used to limit the current in the event of a short-circuited opto-input. This limits the current to less than 60mA. The table below shows the appropriate resistor value and voltage setting for this scheme.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 (ohms)
48/54	24/27	1.2k
110/125	48/54	2.7k
220/250	110/125	5.2k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

14.4.1.2 PSL FOR TCS SCHEME 1

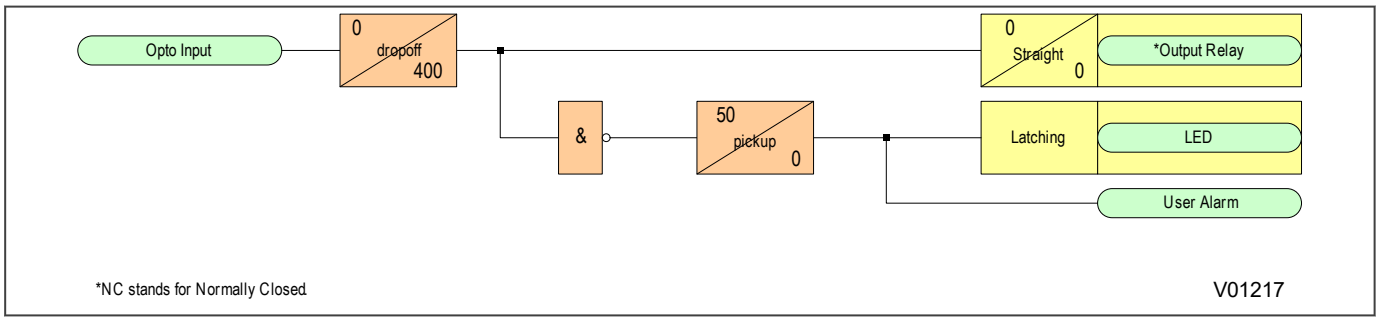


Figure 155: PSL for TCS Scheme 1

The opto-input can be used to drive a Normally Closed Output Relay, which in turn can be used to drive alarm equipment. The signal can also be inverted to drive a latching programmable LED and a user alarm DDB signal.

The DDO timer operates as soon as the opto-input is energised, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto-input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the power up time, following a voltage supply interruption.

14.4.2 TRIP CIRCUIT SUPERVISION SCHEME 3

TCS Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed. It provides pre-closing supervision of the trip path. Since only one opto-input is used, this scheme is not compatible with latched trip contacts. If you require CB status monitoring, further opto-inputs must be used.

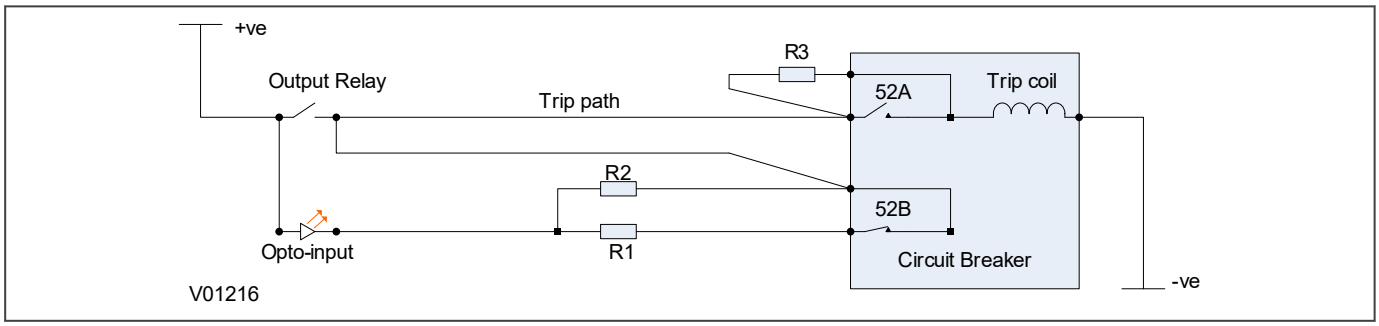


Figure 156: TCS Scheme 3

When the CB is closed, supervision current passes through the opto-input, resistor R2 and the trip coil. When the CB is open, current flows through the opto-input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. The

supervision current is maintained through the trip path with the breaker in either state, therefore providing pre-closing supervision.

14.4.2.1 RESISTOR VALUES

Resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes. This scheme is dependent upon the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Trip Circuit Voltage	Opto Voltage Setting with R1 Fitted	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)
48/54	24/27	1.2k	600
110/250	48/54	2.7k	1.2k
220/250	110/125	5.0k	2.5k

Warning:
This Scheme is not compatible with Trip Circuit voltages of less than 48 V.

14.4.2.2 PSL FOR TCS SCHEME 3

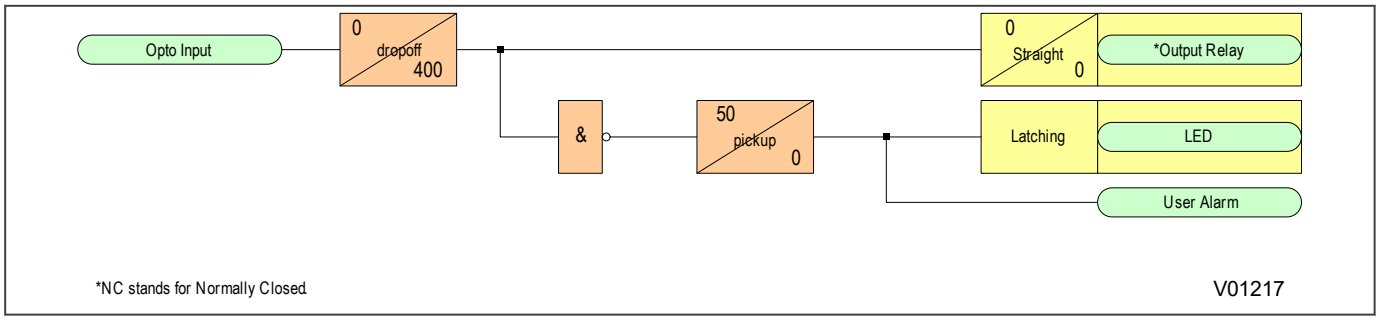


Figure 157: PSL for TCS Scheme 3

CHAPTER 15

DIGITAL I/O AND PSL CONFIGURATION

15.1 CHAPTER OVERVIEW

This chapter introduces the PSL (Programmable Scheme Logic) Editor, and describes the configuration of the digital inputs and outputs. It provides an outline of scheme logic concepts and the PSL Editor. This is followed by details about allocation of the digital inputs and outputs, which require the use of the PSL Editor. A separate "Settings Application Software" document is available that gives a comprehensive description of the PSL, but enough information is provided in this chapter to allow you to allocate the principal digital inputs and outputs.

This chapter contains the following sections:

Chapter Overview 322
Configuring Digital Inputs and Outputs 323
Scheme Logic 324
Configuring the Opto-Inputs 326
Assigning the Output Relays 327
Fixed Function LEDs 328
Configuring Programmable LEDs 329
Function Keys 331
Control Inputs 332
User Alarms 333

15.2 CONFIGURING DIGITAL INPUTS AND OUTPUTS

Configuration of the digital inputs and outputs in this product is very flexible. You can use a combination of settings and programmable logic to customise them to your application. You can access some of the settings using the keypad on the front panel, but you will need a computer running the settings application software to fully interrogate and configure the properties of the digital inputs and outputs.

The settings application software includes an application called the PSL Editor (Programmable Scheme Logic Editor). The PSL Editor lets you allocate inputs and outputs according to your specific application. It also allows you to apply attributes to some of the signals such as a drop-off delay for an output contact.

In this product, digital inputs and outputs that are configurable are:

- Optically isolated digital inputs (opto-inputs). These can be used to monitor the status of associated plant.
- Output relays. These can be used for purposes such as initiating the tripping of circuit breakers, providing alarm signals, etc..
- Programmable LEDs. The number and colour of the programmable LEDs varies according to the particular product being applied.
- Function keys and associated LED indications. These are not provided on all products, but where they are, each function key has an associated tri-colour LED.
- IEC 61850 GOOSE inputs and outputs. These are only provided on products that have been specified for connection to an IEC61850 system, and the details of the GOOSE are presented in the documentation on IEC61850.

15.3 SCHEME LOGIC

The product is supplied with pre-loaded Fixed Scheme Logic (FSL) and Programmable Scheme Logic (PSL).

The Scheme Logic is a functional module within the IED, through which all mapping of inputs to outputs is handled. The scheme logic can be split into two parts; the Fixed Scheme Logic (FSL) and the Programmable Scheme Logic (PSL). It is built around a concept called the digital data bus (DDB). The DDB encompasses all of the digital signals (DDBs) which are used in the FSL and PSL. The DDBs included digital inputs, outputs, and internal signals.

The FSL is logic that has been hard-coded in the product. It is fundamental to correct interaction between various protection and/or control elements. It is fixed and cannot be changed.

The PSL gives you a facility to develop custom schemes to suit your application if the factory-programmed default PSL schemes do not meet your needs. Default PSL schemes are programmed before the product leaves the factory. These default PSL schemes have been designed to suit typical applications and if these schemes suit your requirements, you do not need to take any action. However, if you want to change the input-output mappings, or to implement custom scheme logic, you can change these, or create new PSL schemes using the PSL editor.

The PSL consists of components such as logic gates and timers, which combine and condition DDB signals.

The logic gates can be programmed to perform a range of different logic functions. The number of inputs to a logic gate are not limited. The timers can be used either to create a programmable delay or to condition the logic outputs. Output contacts and programmable LEDs have dedicated conditioners.

The PSL logic is event driven. Only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This minimises the amount of processing time used by the PSL ensuring industry leading performance.

The following diagram shows how the scheme logic interacts with the rest of the IED.

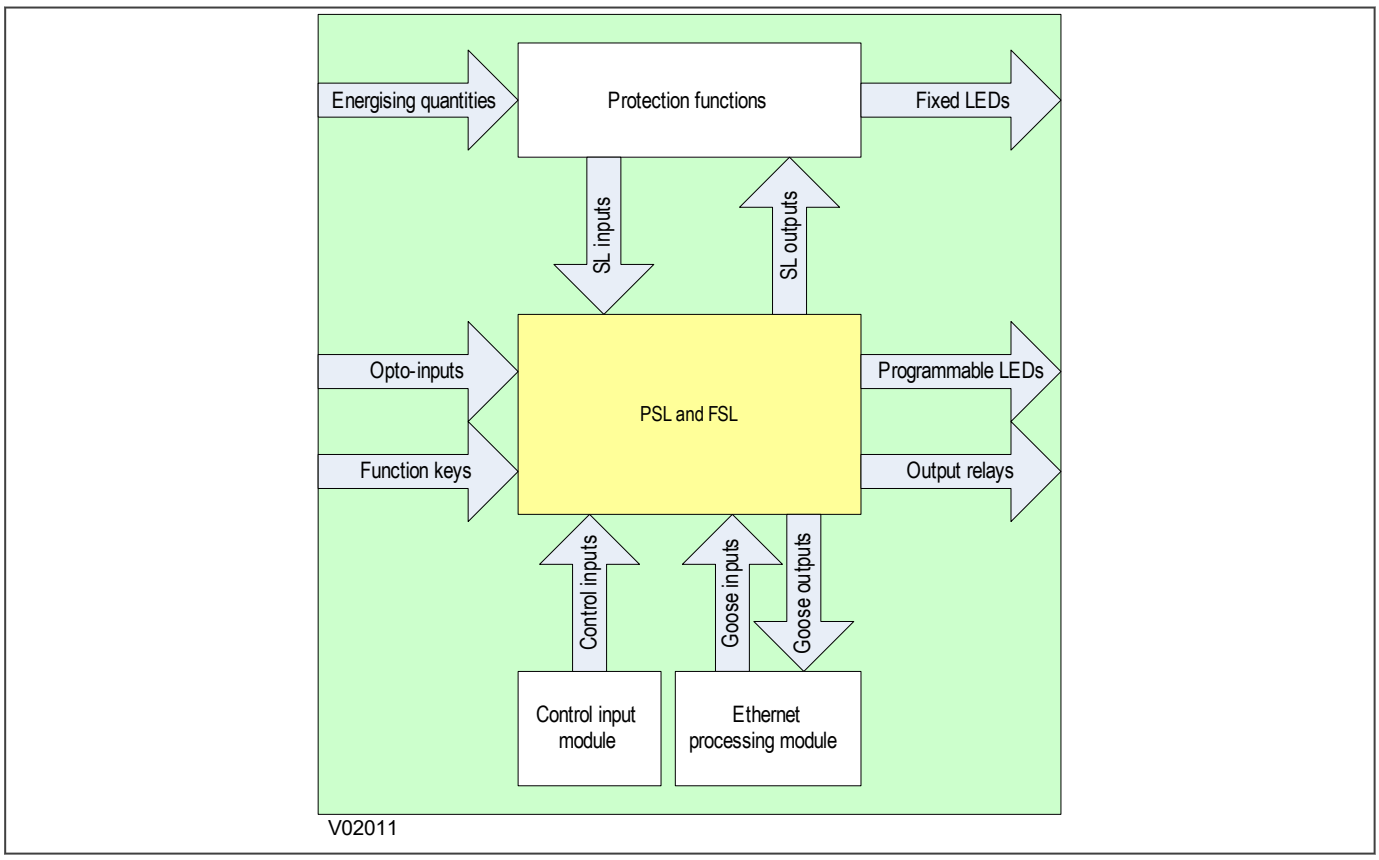


Figure 158: Scheme Logic Interfaces

15.3.1 PSL EDITOR

The Programmable Scheme Logic (PSL) is a module of programmable logic gates and timers in the IED, which can be used to create customised logic to qualify how the product manages its response to system conditions. The IED's digital inputs are combined with internally generated digital signals using logic gates, timers, and conditioners. The resultant signals are then mapped to digital outputs signals including output relays and LEDs.

The PSL Editor is a tool in the settings application software that allows you to create and edit scheme logic diagrams. You can use the default scheme logic which has been designed to suit most applications, but if it does not suit your application you can change it. If you create a different scheme logic with the software, you need to upload it to the device to apply it.

15.3.2 PSL SCHEMES

Your product is shipped with default scheme files. These can be used without modification for most applications, or you can choose to use them as a starting point to design your own scheme. You can also create a new scheme from scratch. To create a new scheme, or to modify an existing scheme, you will need to launch the settings application software. You then need to open an existing PSL file, or create a new one, for the particular product that you are using, and then open a PSL file. If you want to create a new PSL file, you should select **File** then **New** then **Blank scheme...** This action opens a default file appropriate for the device in question, but deletes the diagram components from the default file to leave an empty diagram with configuration information loaded. To open an existing file, or a default file, simply double-click on it.

15.3.3 PSL SCHEME VERSION CONTROL

To help you keep track of the PSL loaded into products, a version control feature is included. The user interface contains a *PSL DATA* column, which can be used to track PSL modifications. A total of 12 cells are contained in the *PSL DATA* column; 3 for each setting group.

Grp(n) PSL Ref: When downloading a PSL scheme to an IED, you will be prompted to enter the relevant group number and a reference identifier. The first 32 characters of the reference identifier are displayed in this cell. The horizontal cursor keys can scroll through the 32 characters as the LCD display only displays 16 characters.

Example:

```
Grp(n) PSL Ref
```

Date/time: This cell displays the date and time when the PSL scheme was downloaded to the IED.

Example:

```
18 Nov 2002
08:59:32.047
```

Grp(n) PSL ID: This cell displays a unique ID number for the downloaded PSL scheme.

Example:

```
Grp(n) PSL ID
ID - 2062813232
```

15.4 CONFIGURING THE OPTO-INPUTS

The number of optically isolated status inputs (opto-inputs) depends on the specific model supplied. The use of the inputs will depend on the application, and their allocation is defined in the programmable scheme logic (PSL). In addition to the PSL assignment, you also need to specify the expected input voltage. Generally, all opto-inputs will share the same input voltage range, but if different voltage ranges are being used, this device can accommodate them.

In the *OPTO CONFIG* column there is a global nominal voltage setting. If all opto-inputs are going to be energised from the same voltage range, you select the appropriate value in the setting. If you select `Custom` in the setting, then the cells ***Opto Input 1***, ***Opto Input 2***, etc. become visible. You use these cells to set the voltage ranges for each individual opto-input.

Within the *OPTO CONFIG* column there are also settings to control the filtering applied to the inputs, as well as the pick-up/drop-off characteristic.

The filter control setting provides a bit string with a bit associated with all opto-inputs. Setting the bit to '1' means that a half-cycle filter is applied to the inputs. This helps to prevent incorrect operation in the event of power system frequency interference on the wiring. Setting the field to '0' removes the filter and provides for faster operation.

The ***Characteristic*** setting is a single setting that applies to all the opto-inputs. It is used to set the pick-up/drop-off ratios of the input signals. As standard it is set to 80% pick-up and 60% drop-off, but you can change it to other available thresholds if that suits your operational requirements.

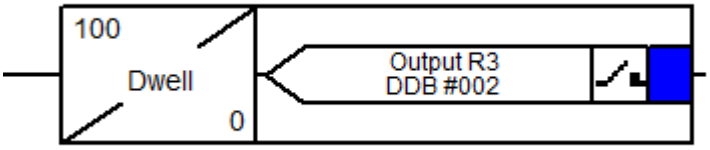
15.5 ASSIGNING THE OUTPUT RELAYS

Relay contact action is controlled using the PSL. DDB signals are mapped in the PSL and drive the output relays. The driving of an output relay is controlled by means of a relay output conditioner. Several choices are available for how output relay contacts are conditioned. For example, you can choose whether operation of an output relay contact is latched, has delay on pick-up, or has a delay on drop-off. You make this choice in the **Contact Properties** window associated with the output relay conditioner.

To map an output relay in the PSL you should use the Contact Conditioner button in the toolbar to import it. You then condition it according to your needs. The output of the conditioner respects the attributes you have assigned.

The toolbar button for a Contact Conditioner looks like this:

The PSL contribution that it delivers looks like this:



Note:
Contact Conditioners are only available if they have not all been used. In some default PSL schemes, all Contact Conditioners might have been used. If that is the case, and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the relay outputs. The button looks like this:

This is the "Contact Signal" button. It allows you to put replica instances of a conditioned output relay into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

15.6 FIXED FUNCTION LEDS

Four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- Trip (Red) switches ON when the IED issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- Alarm (Yellow) flashes when the IED registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- Out of service (Yellow) is ON when the IED's functions are unavailable.
- Healthy (Green) is ON when the IED is in correct working order, and should be ON at all times. It goes OFF if the unit's self-tests show there is an error in the hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the unit.

15.6.1 TRIP LED LOGIC

When a trip occurs, the trip LED is illuminated. It is possible to reset this with a number of ways:

- Directly with a reset command (by pressing the Clear Key)
- With a reset logic input
- With self-resetting logic

You enable the automatic self-resetting with the ***Sys Fn Links*** cell in the *SYSTEM DATA* column. A '0' disables self resetting and a '1' enables self resetting.

The reset occurs when the circuit is reclosed and the ***Any Pole Dead*** signal has been reset for three seconds providing the ***Any Start*** signal is inactive. The reset is prevented if the ***Any Start*** signal is active after the breaker closes.

The Trip LED logic is as follows:

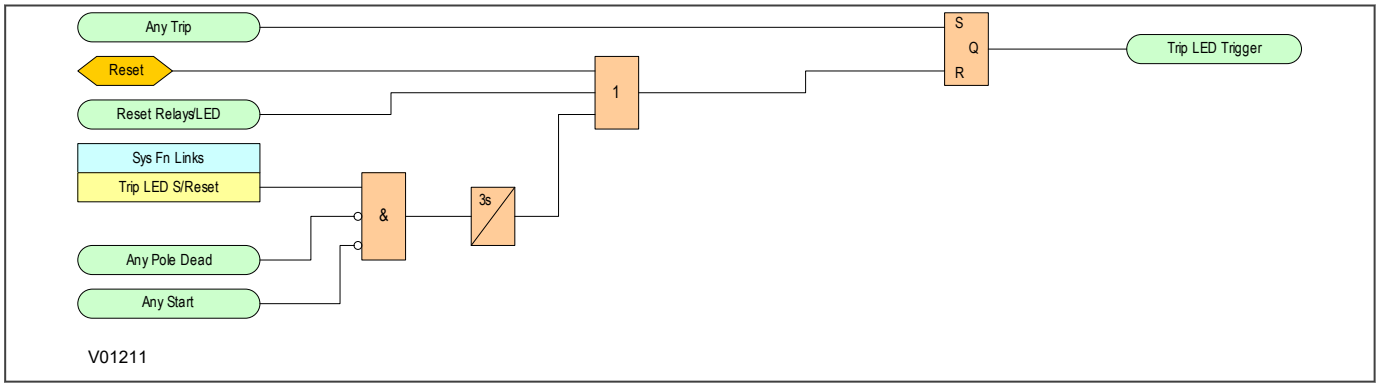


Figure 159: Trip LED logic

15.7 CONFIGURING PROGRAMMABLE LEDS

There are three types of programmable LED signals which vary according to the model being used. These are:

- Single-colour programmable LED. These are red when illuminated.
- Tri-colour programmable LED. These can be illuminated red, green, or amber.
- Tri-colour programmable LED associated with a Function Key. These can be illuminated red, green, or amber.

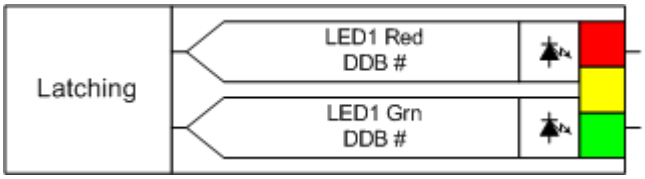
DDB signals are mapped in the PSL and used to illuminate the LEDs. For single-coloured programmable LEDs there is one DDB signal per LED. For tri-coloured LEDs there are two DDB signals associated with the LED. Asserting ***LED # Grn*** will illuminate the LED green. Asserting ***LED # Red*** will illuminate the LED red. Asserting both DDB signals will illuminate the LED amber.

The illumination of an LED is controlled by means of a conditioner. Using the conditioner, you can decide whether the LEDs reflect the real-time state of the DDB signals, or whether illumination is latched pending user intervention.

To map an LED in the PSL you should use the LED Conditioner button in the toolbar to import it. You then condition it according to your needs. The output(s) of the conditioner respect the attribute you have assigned.

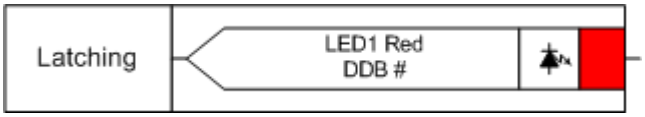
The toolbar button for a tri-colour LED looks like this:

The PSL contribution that it delivers looks like this:



The toolbar button for a single-colour LED looks like this:

The PSL contribution that it delivers looks like this.



Note:
LED Conditioners are only available if they have not all been used up, and in some default PSL schemes they might be. If that is the case and you want to use them for something else, you will need to re-assign them.

On the toolbar there is another button associated with the LEDs. For a tri-coloured LED the button looks like this:

For a single-colour LED it looks like this:

It is the "LED Signal" button. It allows you to put replica instances of a conditioned LED into the PSL, preventing you having to make cross-page connections which might detract from the clarity of the scheme.

Note:
All LED DDB signals are always shown in the PSL Editor. However, the actual number of LEDs depends on the device hardware. For example, if a small 20TE device has only 4 programmable LEDs, LEDs 5-8 will not take effect even if they are mapped in the PSL.

15.8 FUNCTION KEYS

For most models, a number of programmable function keys are available. This allows you to assign function keys to control functionality via the programmable scheme logic (PSL). Each function key is associated with a programmable tri-colour LED, which you can program to give the desired indication on activation of the function key.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands are found in the *FUNCTION KEYS* column.

Each function key is associated with a DDB signal as shown in the DDB table. You can map these DDB signals to any function available in the PSL.

The ***Fn Key Status*** cell displays the status (energised or de-energised) of the function keys by means of a binary string, where each bit represents a function key starting with bit 0 for function key 1.

Each function key has three settings associated with it, as shown:

- ***Fn Key (n)***, which enables or disables the function key
- ***Fn Key (n) Mode***, which allows you to configure the key as toggled or normal
- ***Fn Key (n) label***, which allows you to define the function key text that is displayed

The ***Fn Key (n)*** cell is used to enable (unlock) or disable (unlock) the function key signals in PSL. The Lock setting has been provided to prevent further activation on subsequent key presses. This allows function keys that are set to `Toggled` mode and their DDB signal active 'high', to be locked in their active state therefore preventing any further key presses from deactivating the associated function. Locking a function key that is set to the "Normal" mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical functions.

When the ***Fn Key (n) Mode*** cell is set to `Toggle`, the function key DDB signal output will remain in the set state until a reset command is given. In the `Normal` mode, the function key DDB signal will remain energised for as long as the function key is pressed and will then reset automatically. In this mode, a minimum pulse duration can be programmed by adding a minimum pulse timer to the function key DDB output signal.

The ***Fn Key Label*** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of all function keys are recorded in non-volatile memory. In case of auxiliary supply interruption their status will be maintained.

Note:
All function key DDB signals are always shown in the PSL Editor. However, the actual number of function keys depends on the device hardware. For example, if a small 20TE device has no function keys, the function key DDBs mapped in the PSL will not take effect.

15.9 CONTROL INPUTS

The control inputs are software switches, which can be set or reset locally or remotely. These inputs can be used to trigger any PSL function to which they are connected. There are three setting columns associated with the control inputs: *CONTROL INPUTS*, *CTRL I/P CONFIG* and *CTRL I/P LABELS*. These are listed in the Settings and Records appendix at the end of this manual.

15.10 USER ALARMS

User Alarms can be operated from an opto input or a control input using the PSL. They are useful for giving an alarm led and message on the LCD display, and an alarm indication via the communications of an external condition - for example: trip circuit supervision alarm, and temperature alarm etc. In the ***USER ALARMS*** menu, the ***Manual Reset*** 32 bit binary string (0 self-reset, 1 manual reset) can be used to set the operating mode of the user alarms to self or manual reset. The ***User Alarm 1-32*** labels in the ***USER ALARMS*** menu column are used to individually label each user alarm. The text is restricted to 16 characters.

CHAPTER 16

COMMUNICATIONS

16.1 CHAPTER OVERVIEW

This product supports Substation Automation System (SAS), and Supervisory Control and Data Acquisition (SCADA) communication through multiple interfaces and a choice of data protocols.

All products support rugged serial communications for SCADA and SAS applications. Optionally, any product can support Ethernet communications for IEC 61850, cyber security and remote access, either through a single port or industry-standard redundant ports.

This chapter contains the following sections:

Chapter Overview 336
Communication Interfaces 337
Serial Communication 338
Ethernet Board Versions 341
Board Connections 342
Ethernet Configuration 344
Redundancy Protocols 346
Simple Network Management Protocol (SNMP) 351
Data Protocols 355
Time Synchronisation 383

16.2 COMMUNICATION INTERFACES

The products have a number of standard and optional communication interfaces. The standard and optional hardware and protocols are summarised below:

Port	Availability	Physical Interface	Use	Data Protocols
Front	Standard	USB Type B	Local settings	Courier
Rear Port 1 (RP1 copper)	Standard	RS232/RS485/K-Bus	SCADA Remote settings	Courier, IEC 60870-5-103, DNP3.0
Rear Port 1 (RP1 fibre)	Optional	Fibre	SCADA Remote settings	Courier, IEC 60870-5-103, DNP3.0
Rear Port 2 (RP2)	Optional	RS232/RS485/K-Bus	SCADA Remote settings	SK4: Courier only SK5: InterMiCOM only
Ethernet	Optional	Ethernet	IEC 61850 Remote settings	IEC 61850, Courier Tunnel

Note:
Optional communications boards are always fitted into slot A. It is only possible to fit one optional communications board, therefore RP2 and Ethernet communications are mutually exclusive, except for ZN0098005, where both Ethernet and serial protocols are supported.
On RP1, any one of the data protocols can be selected at one time, from the COMMUNICATIONS Menu (it is no longer necessary to select one as a product order option).

16.3 SERIAL COMMUNICATION

The physical layer standards that are used for serial communications for SCADA purposes are:

- EIA(RS)485 (often abbreviated to RS485)
- K-Bus (a proprietary customization of RS485)

USB is used for local communication with the IED (for transferring settings and downloading firmware updates).

RS485 is similar to RS232 but for longer distances and it allows daisy-chaining and multi-dropping of IEDs.

K-Bus is a proprietary protocol quite similar to RS485, but it cannot be mixed on the same link as RS485. Unlike RS485, K-Bus signals applied across two terminals are not polarised.

It is important to note that these are not data protocols. They only describe the physical characteristics required for two devices to communicate with each other.

For a description of the K-Bus standard see K-Bus and GE Vernova's K-Bus interface guide reference R6509.

A full description of the RS485 is available in the published standard.

16.3.1 USB FRONT PORT

The USB interface uses the proprietary Courier protocol for local communication with the MiCOM S1 Agile settings application software.

This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate of 19200 bps, 11-bit frame (8 data bits, 1 start bit, 1 stop bit, even parity bit), and a fixed device address of '1'.

The USB interface is a Type B connector. Normally a Type A to Type B USB cable will be required to communicate between MiCOM S1 Agile and the IED.

16.3.2 EIA(RS)485 BUS

The RS485 two-wire connection provides a half-duplex, fully isolated serial connection to the IED. The connection is polarized but there is no agreed definition of which terminal is which. If the master is unable to communicate with the product, and the communication parameters match, then it is possible that the two-wire connection is reversed.

The RS485 bus must be terminated at each end with 120 Ω 0.5 W terminating resistors between the signal wires.

The RS485 standard requires that each device be directly connected to the actual bus. Stubs and tees are forbidden. Loop bus and Star topologies are not part of the RS485 standard and are also forbidden.

Two-core screened twisted pair cable should be used. The final cable specification is dependent on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. The total cable length must not exceed 1000 m. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The RS485 signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

It may be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to turn from receive mode to transmit mode. This may be because the master is waiting in receive mode, in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequently not responding. Symptoms of this are; poor response times (due to retries), increasing message error counts, erratic communications, and in the worst case, complete failure to communicate.

16.3.2.1 EIA(RS)485 BIASING REQUIREMENTS

Biasing requires that the signal lines be weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean to prevent noise being injected.

Note:
Some devices may be able to provide the bus bias, in which case external components would not be required.

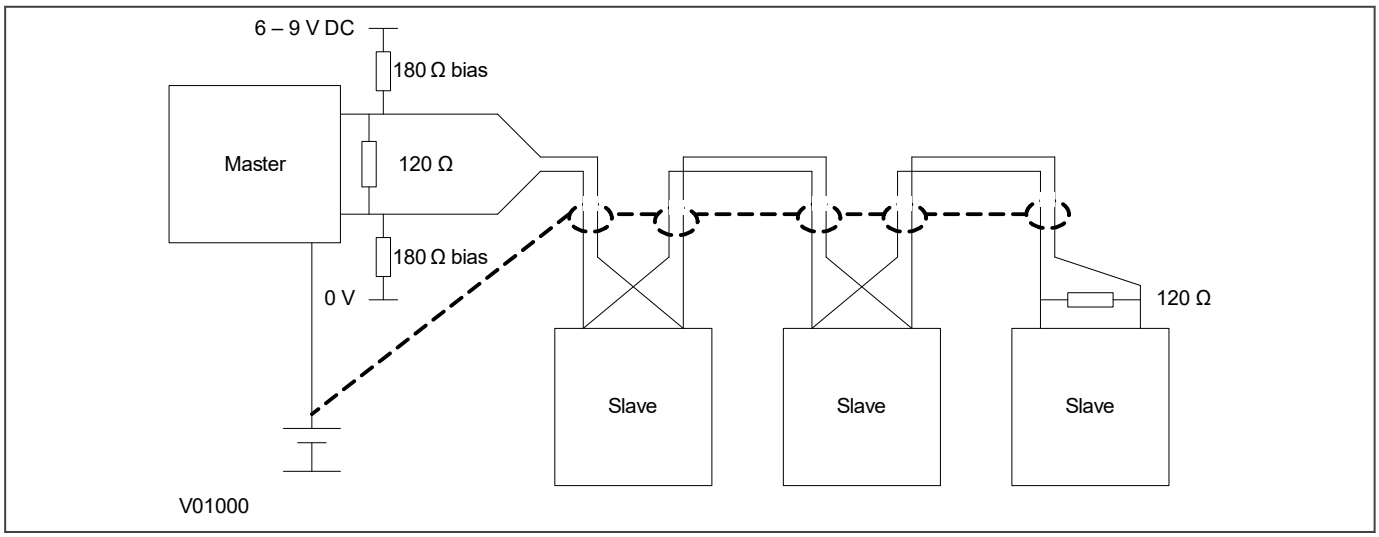


Figure 160: RS485 biasing circuit

Warning:
It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.

16.3.3 K-BUS

K-Bus is a robust signalling method based on RS485 voltage levels. K-Bus incorporates message framing, based on a 64 kbps synchronous HDLC protocol with FM0 modulation to increase speed and security.

The rear interface is used to provide a permanent connection for K-Bus, which allows multi-drop connection.

A K-Bus spur consists of up to 32 IEDs connected together in a multi-drop arrangement using twisted pair wiring. The K-Bus twisted pair connection is non-polarised.

It is not possible to use a standard EIA(RS)232 to EIA(RS)485 converter to convert IEC 60870-5 FT1.2 frames to K-Bus. A protocol converter, namely the KITZ101 or KITZ102, must be used for this purpose. Please consult GE Vernova for information regarding the specification and supply of KITZ devices. The following figure demonstrates a typical K-Bus connection.

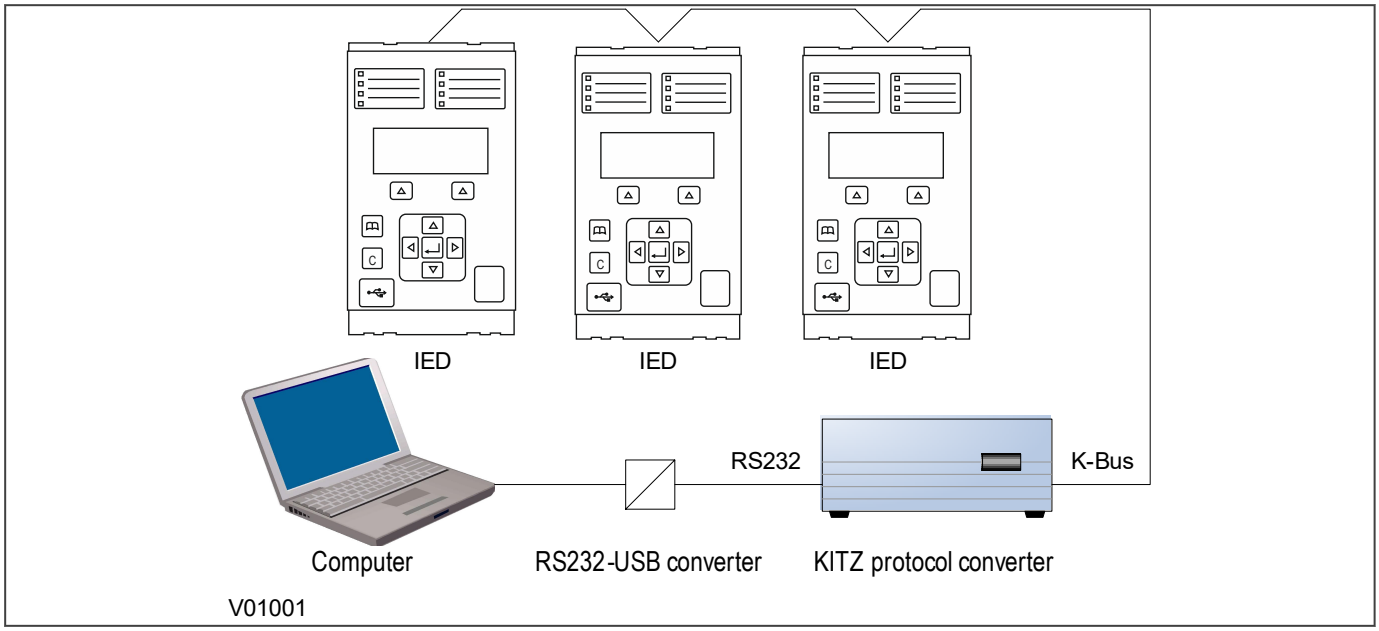


Figure 161: Remote communication using K-Bus

Note:
An RS232-USB converter is only needed if the local computer does not provide an RS232 port.

Further information about K-Bus is available in the publication R6509: K-Bus Interface Guide, which is available on request.

16.4 ETHERNET BOARD VERSIONS

Each board combines Ethernet communications, with universal IRIG-B timing functionality. There is a choice of embedded protocols for the Ethernet communications, and one option that also includes support for serial protocols.

Board variants

Board	Part No.	Compatible With
One LC duplex Ethernet port with universal IRIG-B and IEEE1588 and one RJ45 Maintenance/Engineering Port	ZN0098 001	Ethernet network, no native redundancy.
Two RJ45 duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two copper pairs), with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/engineering port	ZN0098 002	Any PRP, HSR, RSTP or standard Ethernet network
Two LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/engineering port	ZN0098 003	Any PRP, HSR, RSTP or standard Ethernet network
Two LC duplex redundant Ethernet ports running RSTP + PRP + HSR + Failover (two fibre pairs), with serial fibre ST ports with on-board universal IRIG-B and IEEE 1588 and one RJ45 Maintenance/ engineering port	ZN0098 005	Any PRP, HSR, RSTP or standard Ethernet network. On the serial interface Courier, IEC 60870-5-103, DNP3

When using any of the redundant Ethernet boards on an IED, the final product will have two MAC addresses and will require two IP addresses, one for the maintenance port (NP1) for management purposes, and one for the IED station bus communications (NP2). Both of these are set using the IED Configurator tool of MiCOM S1 Agile release 3.1 or later.

All Ethernet connections are made with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (LC connector). The boards support IEC 61850 over Ethernet.

16.5 BOARD CONNECTIONS

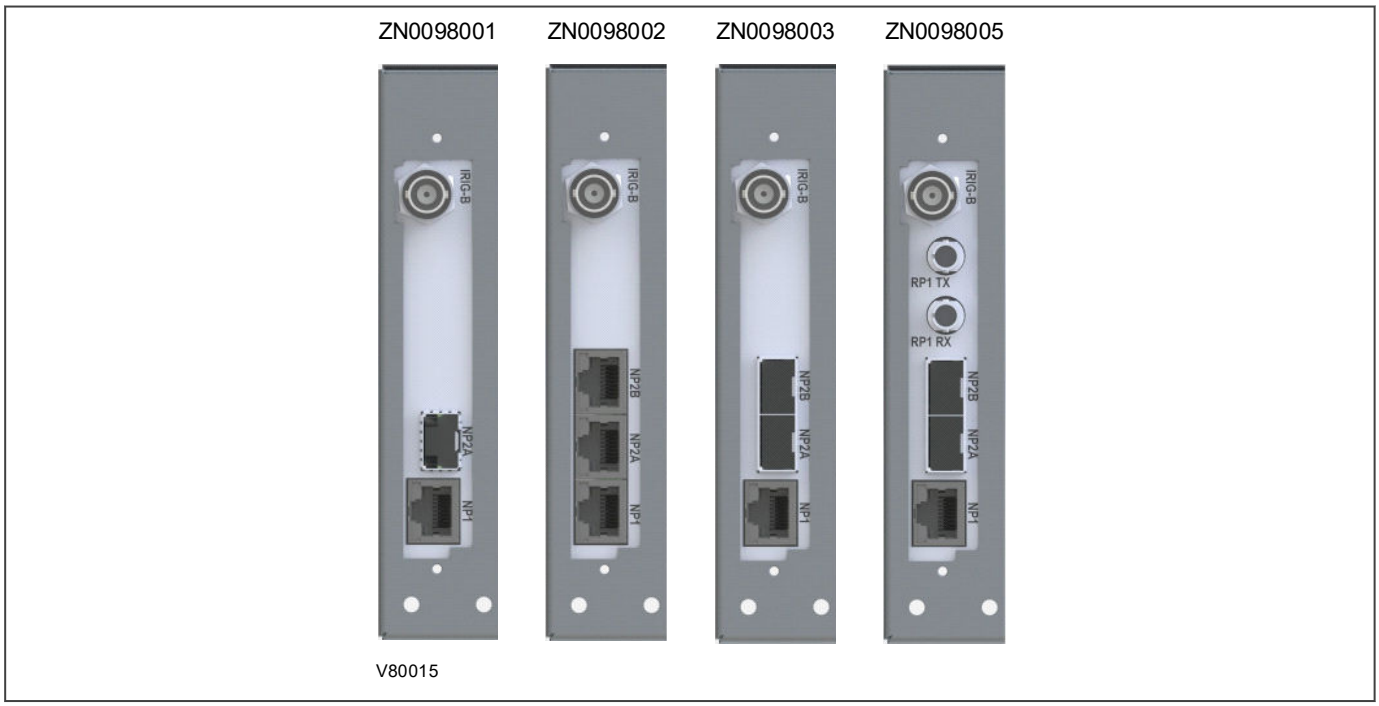


Figure 162: Board connectors

IRIG-B Connector

- Centre connection: Signal
- Outer connection: Earth

RJ45 Connector (NP1, NP2A and NP2B optional)

Pin	Signal Name	Signal Definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

LC Optical Fibre Connectors (NP2A and NP2B optional)

Connector	SFP
A	TX
B	RX

Optical Fibre Connectors (ST only on part ZN0098005)

Connector	Serial Courier, IEC 60870-5-103, DNP3
RP1	TX
RP1	RX

16.6 ETHERNET CONFIGURATION

All configuration for both the monitoring/engineering port and the station bus port is done in **IED Configurator**.

The monitoring/engineering port is named "Network Port 1" and the redundant IEC 61850 station bus port is named "Network Port 2".

Network Port 1 (NP1) and Network Port 2 (NP2) have independent IP address and subnet configuration parameters, as detailed in the sub-section below. These parameters can be configured in IED Configurator, or optionally from the Front Panel UI.

The IP addresses can be in the range 0.0.0.0 to 223.255.255.255. This means it can be configured as either a Class A, B or C address.

Class	Address Range
A	0.0.0.0 to 127.255.255.255
B	128.0.0.0 to 191.255.255.255
C	192.0.0.0 to 223.255.255.255

The NP1 and NP2 IP addresses must not be configured in the same subnet.

The primary and secondary server IP addresses for RADIUS, syslog and SNMP must also be in these ranges.

16.6.1 NETWORK CONFIGURATION

To set the IP address of the monitoring/engineering port:

1. From the main window click the **Communications** section.
2. Navigate to the Network Port 1.
3. Enter the required IP address, network mask and gateway.
4. The media is not configurable for the engineering port, as they are always RJ45 copper ports.

To set the IP address of the station bus port:

1. From the main window click the **Communications** section.
2. Navigate to the Network Port 2.
3. Enter the required IP address, network mask and gateway.
4. In the Network Port 2 General configuration section, the redundancy options become available.
5. If the board supports redundancy, choose the redundant protocol desired (Failover, RSTP, PRP and HSR).
6. Each protocol has its own protocol specific settings, covered in each protocol's section.
7. The media is not configurable for the station bus port, as they are always enabled according to the ordering code. The media section is available for legacy boards only.

16.6.2 PRP CONFIGURATION

To view or configure the PRP Parameters:

1. Set the redundancy mode to **PRP**.
   - **Multicast Address:** Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
   - **Life Check Interval:** This defines how often a node sends a PRP_Supervision frame. All DANPs shall be configured with the same Life Check Interval.

16.6.3 HSR CONFIGURATION

To view or configure the HSR Parameters:

Set the redundancy mode to HSR.

- **Multicast Address:** Use this field to configure the multicast destination address. All DANPs in the network must be configured to operate with the same multicast address for the purpose of network supervision.
- **Life Check Interval**: This defines how often a node sends an HSR Supervision frame. All DANPs shall be configured with the same Life Check Interval.

16.6.4 RSTP CONFIGURATION

To view or configure the RSTP Parameters:

Set the redundancy mode to **RSTP**.

Parameter	Default value (second)	Minimum value (second)	Maximum value (second)
Bridge Max Age	20	6	40
Bridge Hello Time	2	1	10
Bridge Forward Delay	15	4	30
Bridge Priority	32768	0	61440

16.6.5 FAILOVER CONFIGURATION

To view or configure the Failover Parameters:

1. Set the redundancy mode to **Failover**.
   - Port A and Port B radio button allows to select your main port for the Failover. The name of the port in the board is also shown.
   - The Failover time defines how long it takes for the redundancy switch over to trigger. The minimum value is 2s.

16.6.6 SNTP IP ADDRESS CONFIGURATION

To configure the SNTP server IP address:

1. From the main window click the **SNTP** button.
2. The General configuration allows to set the frequency of the polling of the SNTP server. It also has a check-box **IED is a clock source** to configure the IED to be a SNTP server itself, to retransmit its date and time.
3. Under External Server 1 and 2, set the IP address of the SNTP server.

16.7 REDUNDANCY PROTOCOLS

REB variants for each of the following protocols are available:

- PRP (Parallel Redundancy Protocol)
- HSR (High-availability Seamless Redundancy)
- RSTP (Rapid Spanning Tree Protocol)
- Failover

PRP and HSR are open standard, so their implementation is compatible with any standard PRP or HSR device respectively. PRP and HSR provides "bumpless" redundancy. RSTP is also an open standard, so its implementation is compatible with any standard RSTP devices. RSTP provides redundancy, however, it is not "bumpless", the standard instead utilises a loop free topology that is recalculated when a device fails, and does not forward messages during recalculation.

16.7.1 PARALLEL REDUNDANCY PROTOCOL (PRP)

Power system companies have traditionally used proprietary protocols for redundant communications. This is because standardized protocols could not meet the requirements for real-time systems. Even a short loss of connectivity may result in loss of functionality.

However, Parallel Redundancy Protocol (PRP) uses the IEC 62439 standard in Dual Star Topology networks, designed for IEDs from different manufacturers to operate with each other in a substation redundant-Ethernet network. PRP provides bumpless redundancy for real-time systems and is the standard for double Star-topology networks in substations.

16.7.1.1 PRP NETWORKS

Redundant networks usually rely on the network’s ability to reconfigure if there is a failure. However, PRP uses two independent networks in parallel.

PRP implements the redundancy functions in the end nodes rather than in network elements. This is one major difference to RSTP. An end node is attached to two similar LANs of any topology which operate in parallel.

The sending node replicates each frame and transmits them over both networks. The receiving node processes the frame that arrives first and discards the duplicate. Therefore there is no distinction between the working and backup path. The receiving node checks that all frames arrive in sequence and that frames are correctly received on both ports.

The PRP layer manages this replicate and discard function, and hides the two networks from the upper layers. This scheme works without reconfiguration and switchover, so it stays available ensuring no data loss.

There should be no common point of failure between the two LANs. Therefore they are not powered by the same source and cannot be connected directly together. They are identical in protocol at the MAC level but may differ in performance and topology. Both LANs must be on the same subnet so all IP addresses must be unique.

16.7.1.2 NETWORK ELEMENTS

A PRP compatible device has two ports that operate in parallel. Each port is connected to a separate LAN. In the IEC 62439 standard, these devices are called DANP (Doubly Attached Node running PRP). A DAN has two ports, one MAC address and one IP address.

A Single Attached Node (SAN) is a non-critical node attached to only one LAN. SANs that need to communicate with each other must be on the same LAN.

The following diagram shows an example of a PRP network. The Doubly Attached Nodes DANP 1 and DANP 2 have full node redundancy. The Singly Attached Nodes SAN 1 and SAN 4 do not have any redundancy. Singly attached nodes can be connected to both LANs using a Redundancy Box (RedBox). The RedBox converts a singly attached node into a doubly attached node. Devices such as PCs with one network board, printers, and IEDs with

one network board are singly attached nodes. A SAN behind a RedBox appears like a DAN so is called a Virtual DAN (VDAN).

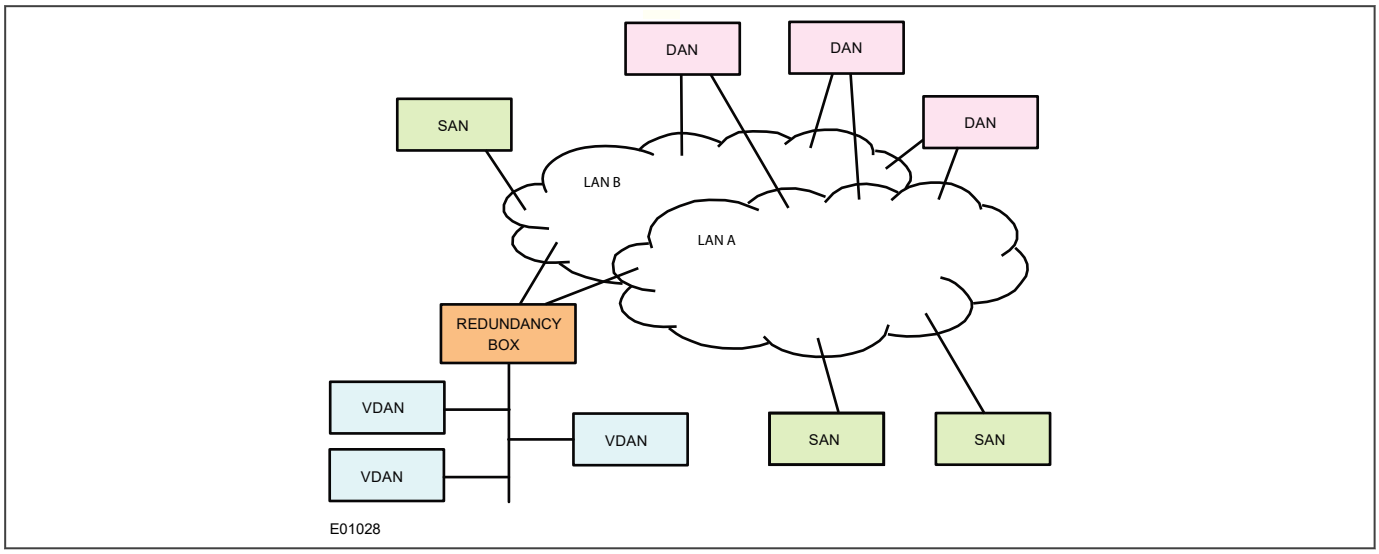


Figure 163: Example PRP redundant network

In a DAN, both ports share the same MAC address so it does not affect the way devices talk to each other in an Ethernet network (Address Resolution Protocol at layer 2). Every data frame is seen by both ports.

When a DAN sends a frame of data, the frame is duplicated on both ports and therefore on both LAN segments. This provides a redundant path for the data frame if one of the segments fails. Under normal conditions, both LAN segments are working and each port receives identical frames. There are two ways of handling this: Duplicate Accept and Duplicate Discard.

The GE Vernova RedBox is the H49 switch. This is compatible with any other vendor's PRP device.

16.7.2 HIGH-AVAILABILITY SEAMLESS REDUNDANCY (HSR)

HSR is standardized in IEC 62439-3 (clause 5) for use in ring topology networks. Similar to PRP, HSR provides bumpless redundancy and meets the most demanding needs of substation automation. HSR has become the reference standard for ring-topology networks in the substation environment. The HSR implementation of the redundancy Ethernet board (REB) is compatible with any standard HSR device.

HSR works on the premise that each device connected in the ring is a doubly attached node running HSR (referred to as DANH). Similar to PRP, singly attached nodes such as printers are connected via Ethernet Redundancy Boxes (RedBox).

16.7.2.1 HSR MULTICAST TOPOLOGY

When a DANH is sending a multicast frame, the frame (C frame) is duplicated (A frame and B frame), and each duplicate frame A/B is tagged with the destination MAC address and the sequence number. The frames A and B differ only in their sequence number, which is used to identify one frame from the other. Each frame is sent to the network via a separate port. The destination DANH receives two identical frames, removes the HSR tag of the first frame received and passes this (frame D) on for processing. The other duplicate frame is discarded. The nodes forward frames from one port to the other unless it was the node that injected it into the ring.

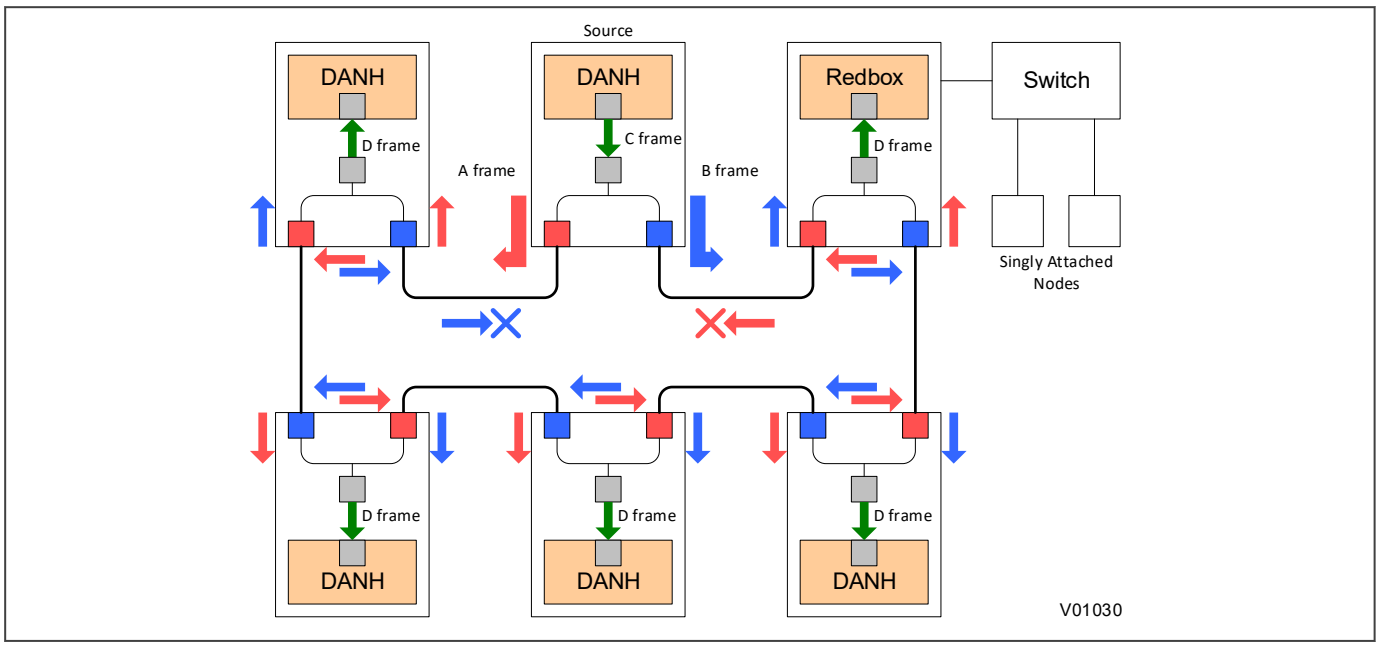


Figure 164: HSR multicast topology

Only about half of the network bandwidth is available in HSR for multicast or broadcast frames because both duplicate frames A & B circulate the full ring.

16.7.2.2 HSR UNICAST TOPOLOGY

With unicast frames, there is just one destination and the frames are sent to that destination alone. All non-recipient devices simply pass the frames on. They do not process them in any way. In other words, D frames are produced only for the receiving DANH. This is illustrated below.

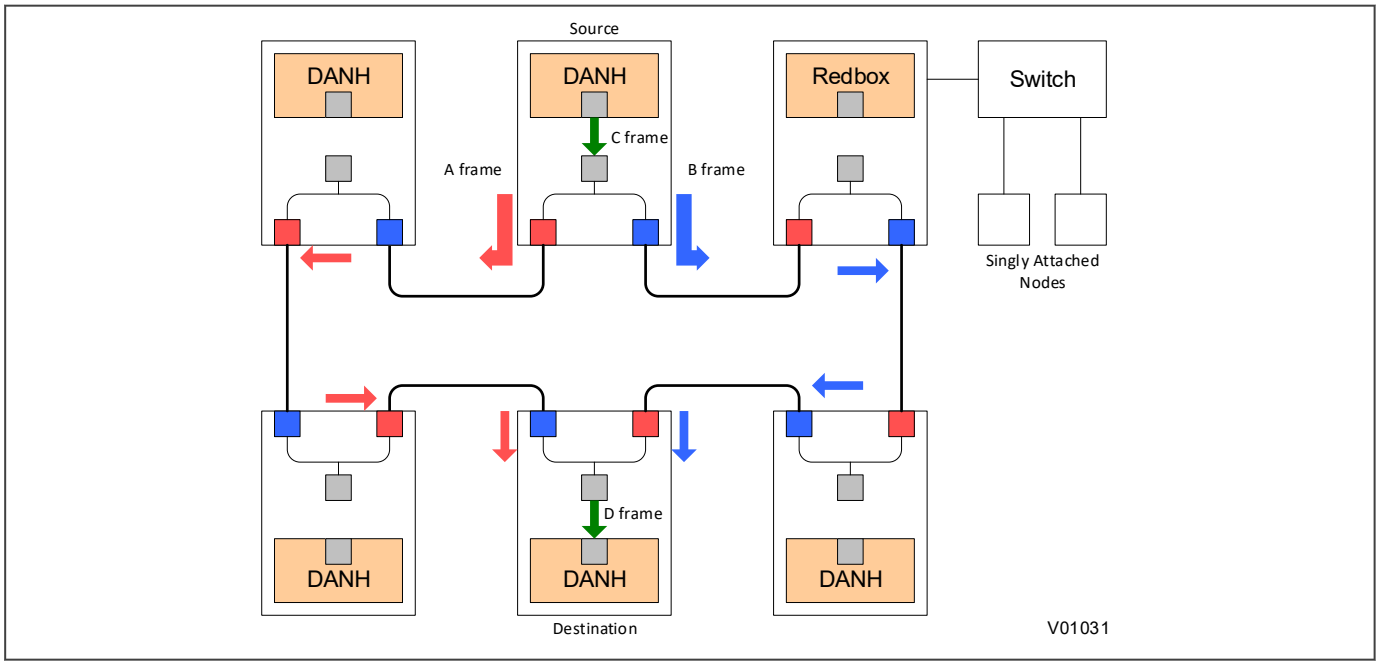


Figure 165: HSR unicast topology

For unicast frames, the whole bandwidth is available as both frames A & B stop at the destination node.

16.7.2.3 HSR APPLICATION IN THE SUBSTATION

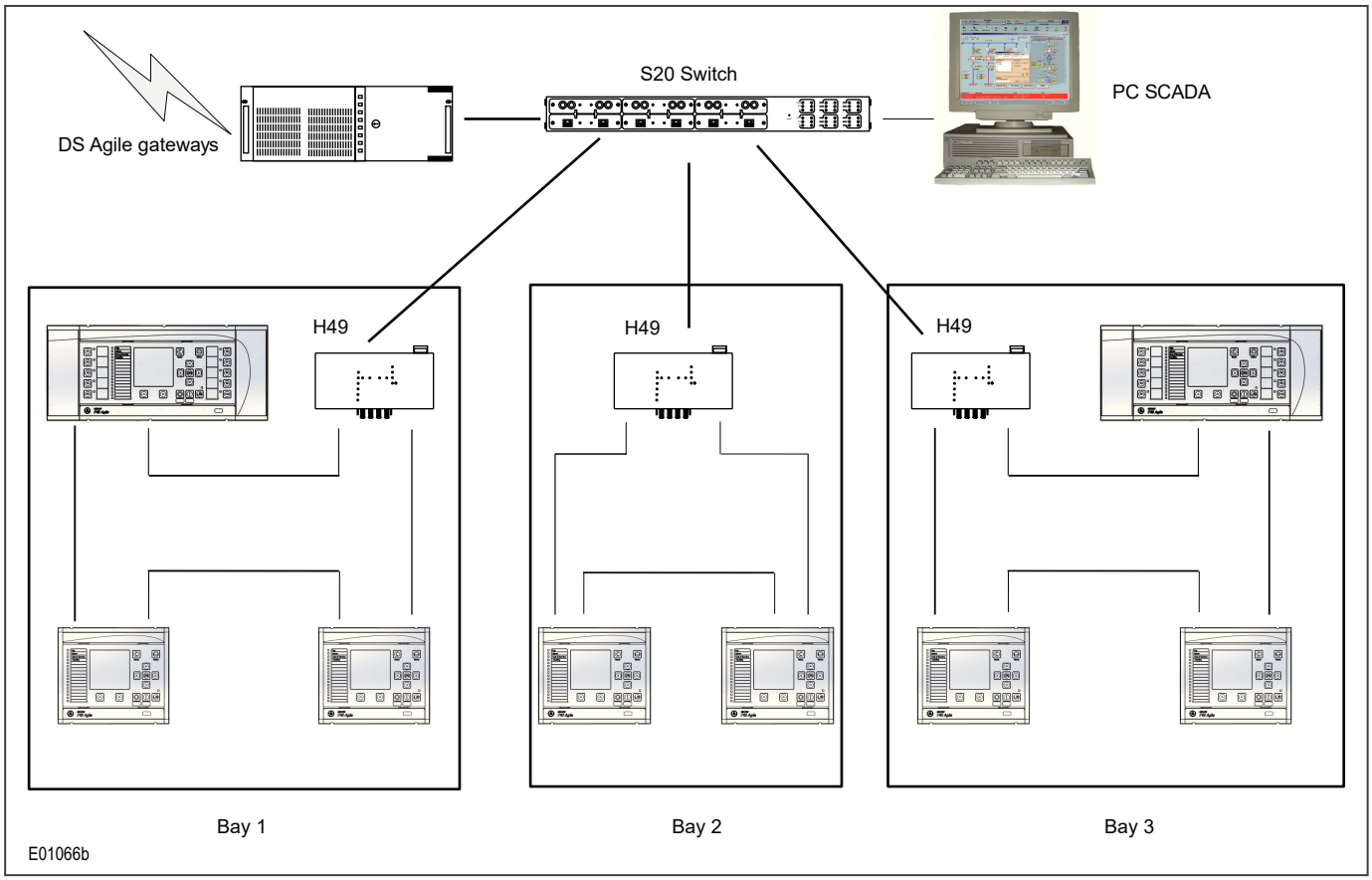


Figure 166: HSR application in the substation

16.7.3 RAPID SPANNING TREE PROTOCOL (RSTP)

RSTP is a standard used to quickly reconnect a network fault by finding an alternative path, allowing loop-free network topology. Although RSTP can recover network faults quickly, the fault recovery time depends on the number of devices and the topology. The recovery time also depends on the time taken by the devices to determine the root bridge and compute the port roles (discarding, learning, forwarding). The devices do this by exchanging Bridge Protocol Data Units (BPDUs) containing information about bridge IDs and root path costs. See the IEEE 802.1D 2004 standard for further information.

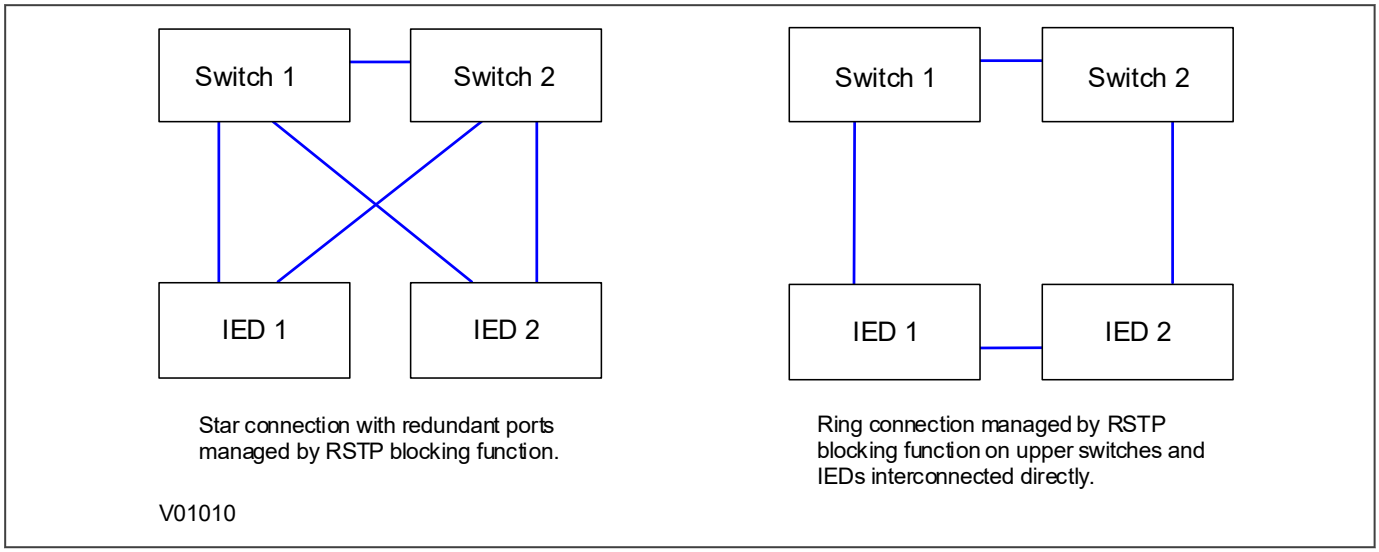


Figure 167: IED attached to redundant Ethernet star or ring circuit

The RSTP solution is based on open standards. It is therefore compatible with other Manufacturers' IEDs that use the RSTP protocol. The RSTP recovery time is typically 300 ms but it increases with network size, therefore cannot achieve the desired bumpless redundancy.

To ensure optimal performance of the protocol, make sure that one of the Ethernet switches is always the root of the RSTP topology.

16.7.4 FAILOVER

Failover is a simple redundancy mechanism that is not tied to any protocol. It works by selecting a main port and a switching time that can be as low as 2 seconds. When the main port link fails, the redundant port becomes physically active. At no point are both ports physically active, which means it can be used on any redundant or non-redundant network.

16.8 SIMPLE NETWORK MANAGEMENT PROTOCOL (SNMP)

Simple Network Management Protocol (SNMP) is a network protocol designed to manage devices in an IP network. SNMP uses a Management Information Base (MIB) that contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object Identifier (OID). Each OID identifies a variable that can be read or set using SNMP with the appropriate software. The information in the MIB is standardised.

Each system in a network (workstation, server, router, bridge, etc.) maintains a MIB that reflects the status of the managed resources on that system, such as the version of the software running on the device, the IP address assigned to a port or interface, the amount of free hard drive space, or the number of open files. The MIB does not contain static data, but is instead an object-oriented, dynamic database that provides a logical collection of managed object definitions. The MIB defines the data type of each managed object and describes the object.

The SNMP-related branches of the MIB tree are located in the internet branch, which contains two main types of branches:

- Public branches (mgmt=2), which are defined by the Internet Engineering Task Force (IETF).
- Private branches (private=4), which are assigned by the Internet Assigned Numbers Authority (IANA). These are defined by the companies and organizations to which these branches are assigned.

The following figure shows the structure of the SNMP MIB tree. There are no limits on the width and depth of the MIB tree.

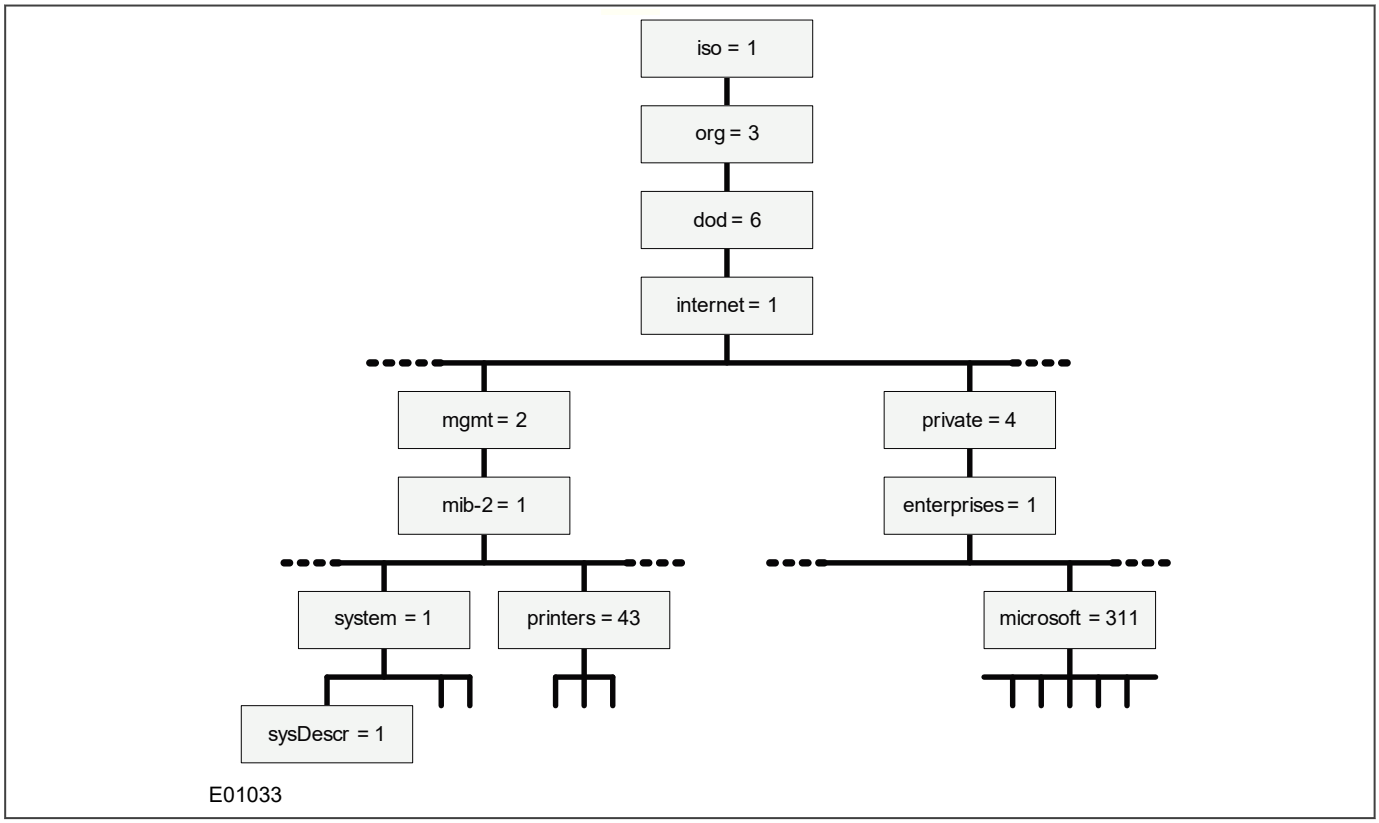


Figure 168: SNMP MIB tree

The top four levels of the hierarchy are fixed. These are:

- International Standards Organization (iso)
- Organization (org)
- Department of Defence (dod)
- Internet

Management (mgmt) is the main public branch. It defines network management parameters common to devices from all vendors. Underneath the Management branch is MIB-II (mib-2), and beneath this are branches for common management functions such as system management, printers, host resources, and interfaces.

The private branch of the MIB tree contains branches for large organizations, organized under the enterprises branch. This is not applicable to GE Vernova.

16.8.1 SNMP MIBS COMPATIBLE WITH THE IED

Our IED supports four different MIBs, all available for download on the GE website:

- IEC-62439-3-MIB: Standard PRP/HSR MIB.
- RMON-MIB: Standard Remote Monitoring MIB.
- GE-PX4X-MIB.mib: Private MIB that contains all the information specific to the relay. For example, model and serial number.
- GE-GRID-MIB.mib: Private MIB that only contains manufacturer information.

The information within the MIBs can be read using a simple text app like Notepad, or the MIB can be explored using an MIB Browser.

The private branch of the MIB tree contains branches for large organizations, organized under the enterprises branch. This is not applicable to GE Vernova.

16.8.2 NEW SNMP SYSTEM OBJECTS

The following elements have been added to the SNMP structure to more accurately describe the new functionalities added in the Ethernet boards:

16.8.2.1 NEW SNMP TRAPS

Changes in the Physical link statuses (Up or Down status) of NP1, NP2A, NP2B ethernet ports will be reported as SNMP traps.

The objects for these link statuses are added in MIB (GE-PX4X-MIB.mib). Below are the IDs for Network Port link objects:

- **np1Link**: 1.3.6.1.4.1.55461.1.6.1
- **np2ALink**: 1.3.6.1.4.1.55461.1.6.2
- **np2Blink**: 1.3.6.1.4.1.55461.1.6.3

16.8.2.2 NEW SNMP OBJECTS

The following objects have been added to MIB (GE-PX4X-MIB.mib) to add more visibility to the behaviour of the Ethernet board.

- **np2Redundancy:** .1.3.6.1.4.1.55461.1.6.4, represents active redundancy protocol set in the device.
- **rstpRootIdentifier**: .1.3.6.1.4.1.55461.1.6.5, represents RSTP Rot Bridge Identifier. It is a combination of Root bridge's priority and its MAC address.
- **rstpTimeSinceTopoChange**: .1.3.6.1.4.1.55461.1.6.6, represents the time elapsed since last RSTP topology change.
- **rstpTopoChangeCount**: .1.3.6.1.4.1.55461.1.6.7, represents RSTP topology change count.

16.8.3 SNMP ALARM ENHANCEMENT

An SNMP alarm is triggered by the relay when a security event occurs, if SNMP trap destination IP is configured in the settings.

16.8.3.1 SNMP ALARM FORMAT

The format of the SNMP trap/alarm for security events consists of three parts as described below.

"Event Description, Username, Interface".

Event Description: Short description of the alarm, same as the description present in Security event.

Username: User associated with the event, provided only when Username is available for the Security event.

Interface: Interface on which Security event has occurred, same as the interface information present in Security event.

16.8.3.2 LIST OF SNMP ALARMS

No.	Security Events	SNMP Trap Text
1	SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
2	SECUR_EVT_PW_MODIFIED	User password changed successfully
3	SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked - wrong credentials
4	SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
5	SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
6	SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - wrong credentials
7	SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired
8	SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
9	SECUR_EVT_IED_SEC_CODE_READ	Security Code read
10	SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
11	SECUR_EVT_PORT_DISABLED	Port Disabled
12	SECUR_EVT_PORT_ENABLED	Port Enabled
13	SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
14	SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
15	SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
16	SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
17	SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
18	SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
19	SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
20	SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
21	SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
22	SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
23	SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
24	SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
25	SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed

No.	Security Events	SNMP Trap Text
26	SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
27	SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
28	SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
29	SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
30	SECUR_EVT_POWER_ON	Device Powered On
31	SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
32	SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
33	SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
34	SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
35	SECUR_EVT_RBAC_LOGIN	Log-in successful
36	SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
37	Bypass mode Activated	Bypass Mode Activated
38	Bypass mode Deactivated	Bypass Mode Deactivated
39	RADIUS Secret Key changed	RADIUS Secret Key changed
40	SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
41	Switch to Golden Image	Device switching to Firmware update mode
42	Fallback to Device Authentication	Fallback to Device Authentication
43	User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
44	Security events upload	Security Events uploaded from device
45	SSH Passcode change	SSH pass code change
46	SSH Client Authentication Fail	Failed client authentication
47	SSH Client Authentication Success	Successful client authentication
48	New User added	User account created successfully
49	User deleted	User account deleted successfully
50	User role change	Permission changed successfully
51	User name change	User renamed successfully

16.9 DATA PROTOCOLS

The products support a wide range of protocols to make them applicable to many industries and applications. The exact data protocols supported by a particular product depend on its chosen application, but the following table gives a list of the data protocols that are typically available.

DATA PROTOCOLS

Data Protocol	Layer 1 Interface	Description
Courier	USB, K-Bus, RS232, RS485, Ethernet	Standard for SCADA communications developed by GE Vernova.
IEC 60870-5-103	RS485	IEC standard for SCADA communications
DNP 3.0	RS485	Standard for SCADA communications
IEC 61850	Ethernet	IEC standard for substation automation. Facilitates interoperability.

The relationship of these protocols to the lower-level physical layer protocols are as follows:

Data Protocols	IEC 60870-5-103 DNP3.0 Courier	IEC 61850 Courier	Courier	Courier	Courier
Data Link Layer	EIA(RS)485	Ethernet	EIA(RS)232	K-Bus	USB
Physical Layer	Copper or Optical Fibre				USB Type B

The product supports switchable serial communication data protocol on the Rear Port 1 (RP1) interface (it is no longer necessary to select the protocol as a product order option). This setting cell is ***RP1 Protocol*** in the *COMMUNICATIONS* column. For example, the product can now be configured to provide IEC 61850 on the Ethernet interface and DNP3.0 on the serial port concurrently.

16.9.1 COURIER

This section should provide sufficient detail to enable understanding of the Courier protocol at a level required by most users. For situations where the level of information contained in this manual is insufficient, further publications (R6511 and R6512) containing in-depth details about the protocol and its use, are available on request.

Courier is a GE Vernova proprietary communication protocol. Courier uses a standard set of commands to access a database of settings and data in the IED. This allows a master to communicate with a number of slave devices. The application-specific elements are contained in the database rather than in the commands used to interrogate it, meaning that the master station does not need to be preconfigured. Courier also provides a sequence of event (SOE) and disturbance record extraction mechanism.

16.9.1.1 PHYSICAL CONNECTION AND LINK LAYER

Courier can be used with four physical layer protocols: USB, K-Bus, EIA(RS)232 or EIA(RS)485.

Several connection options are available for Courier

- The front USB port (for connection to Settings application software on, for example, a laptop)
- Rear Port 1 (RP1) - for permanent SCADA connection via serial RS485 or K-Bus
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via serial optical fibre
- Optional Rear Port 2 (RP2) - for permanent SCADA connection via serial RS485, K-Bus, or RS232

Optional Ethernet board (NIC) - for remote communication with the S1 Agile settings application software across an Ethernet network.

For either of the serial rear ports, both the IED address and baud rate can be selected using the front panel menu or by the settings application software.

Note:
*Changing the **RP2 Port Config** setting (K-Bus, EIA(RS)232) requires the IED to be rebooted, for the change to become effective.*

16.9.1.2 COURIER DATABASE

The Courier database is two-dimensional and resembles a table. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255 (0000 to FFFF Hexadecimal. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The product-specific menu databases contain the complete database definition.

16.9.1.3 SETTINGS CATEGORIES

There are two main categories of settings in protection IEDs:

- Control and support settings
- Protection settings

With the exception of the Disturbance Recorder settings, changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to the Protection settings and the Disturbance Recorder settings are stored in 'scratchpad' memory and are not immediately implemented. These need to be committed by writing to the ***Save Changes*** cell in the *CONFIGURATION* column.

16.9.1.4 SETTING CHANGES

Courier provides two mechanisms for making setting changes. Either method can be used for editing any of the settings in the database.

Method 1

This uses a combination of three commands to perform a settings change:

First, enter Setting mode: This checks that the cell is settable and returns the limits.

1. Preload Setting: This places a new value into the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
2. Execute Setting: This confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
3. Abort Setting: This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are extracted before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

Method 2

The Set Value command can be used to change a setting directly. The response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method; however the limits are not extracted. This method is therefore most suitable for off-line setting editors such as MiCOM S1 Agile, or for issuing preconfigured control commands.

16.9.1.5 EVENT EXTRACTION

You can extract events either automatically (rear serial port only) or manually (either serial port). For automatic extraction, all events are extracted in sequential order using the Courier event mechanism. This includes fault and maintenance data if appropriate. The manual approach allows you to select events, faults, or maintenance data as desired.

16.9.1.5.1 AUTOMATIC EVENT RECORD EXTRACTION

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the ***Event*** bit is set in the ***Status*** byte. This indicates to the Master device that event information is available. The oldest, non-extracted event can be extracted from the IED using the ***Send Event*** command. The IED responds with the event data.

Once an event has been extracted, the ***Accept Event*** command can be used to confirm that the event has been successfully extracted. When all events have been extracted, the ***Event*** bit is reset. If there are more events still to be extracted, the next event can be accessed using the ***Send Event*** command as before.

16.9.1.5.2 MANUAL EVENT RECORD EXTRACTION

The *VIEW RECORDS* column (location 01) is used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. You can select events by event number and directly select a fault or maintenance record by number.

Event Record Selection ('Select Event' cell: 0101)

This cell can be set the number of stored events. For simple event records (Type 0), cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault Record Selection ('Select Fault' cell: 0106)

This cell can be used to select a fault record directly, using a value between 0 and 99 to select one of up to a hundred stored fault records. (0 is the most recent fault and 99 is the oldest). The column then contains the details of the fault record selected.

Maintenance Record Selection ('Select Maint' cell: 01F0)

This cell can be used to select a maintenance record using a value between 0 and 9. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information, the number associated with a particular record changes when a new event or fault occurs.

Event Types

The IED generates events under certain circumstances such as:

- Change of state of output contact
- Change of state of opto-input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out

Event Record Format

The IED returns the following fields when the Send Event command is invoked:

- Cell reference
- Time stamp
- Cell text
- Cell value

The Menu Database contains tables of possible events, and shows how the contents of the above fields are interpreted. Fault and Maintenance records return a Courier Type 3 event, which contains the above fields plus two additional fields:

- Event extraction column
- Event number

These events contain additional information, which is extracted from the IED using column B4. Row 01 contains a ***Select Record*** setting that allows the fault or maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the IED by uploading the text and data from the column.

16.9.1.6 DISTURBANCE RECORD EXTRACTION

The stored disturbance records are accessible through the Courier interface. The records are extracted using column (B4).

The ***Select Record*** cell can be used to select the record to be extracted. Record 0 is the oldest non-extracted record. Older records which have already been extracted are assigned positive values, while younger records are assigned negative values. To help automatic extraction through the rear port, the IED sets the ***Disturbance*** bit of the ***Status*** byte, whenever there are non-extracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from the ***Trigger Time*** cell (B402). The disturbance record can be extracted using the block transfer mechanism from cell B40B and saved in the COMTRADE format. The settings application software software automatically does this.

16.9.1.7 PROGRAMMABLE SCHEME LOGIC SETTINGS

The programmable scheme logic (PSL) settings can be uploaded from and downloaded to the IED using the block transfer mechanism.

The following cells are used to perform the extraction:

- ***Domain*** cell (B204): Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- ***Sub-Domain*** cell (B208): Used to select the Protection Setting Group to be uploaded or downloaded.
- ***Version*** cell (B20C): Used on a download to check the compatibility of the file to be downloaded.
- ***Transfer Mode*** cell (B21C): Used to set up the transfer process.
- ***Data Transfer*** cell (B120): Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the IED using this mechanism. The settings application software must be used to edit the settings. It also performs checks on the validity of the settings before they are transferred to the IED.

16.9.1.8 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the Courier protocol. The device will correct for the transmission delay. The time synchronization message may be sent as either a global command or to any individual IED address. If the time synchronization message is sent to an individual address, then the device will respond with a confirm message. If sent as a global command, the (same) command must be sent twice. A time

synchronization Courier event will be generated/produced whether the time-synchronization message is sent as a global command or to any individual IED address.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

16.9.1.9 COURIER CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `Courier`.
4. Move down to the next cell (***RP1 Address***). This cell controls the address of the RP1 port on the device. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. Courier uses an integer number between 1 and 254 for the Relay Address. It is set to 255 by default, which has to be changed. It is important that no two IEDs share the same address.
5. Move down to the next cell (***RP1 InactivTimer***). This cell controls the inactivity timer. The inactivity timer controls how long the IED waits without receiving any messages on the rear port before revoking any password access that was enabled and discarding any changes. For the rear port this can be set between 1 and 30 minutes.
6. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
7. Move down to the next cell (***RP1 Card Status***). This cell is not settable. It displays the status of the chosen physical layer protocol for RP1.
8. Move down to the next cell (***RP1 Port Config***). This cell controls the type of serial connection. Select between K-Bus or RS485.
9. If using EIA(RS)485, the next cell (***RP1 Comms Mode***) selects the communication mode. The choice is either IEC 60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity. If using K-Bus this cell will not appear.
10. If using EIA(RS)485, the next cell down controls the baud rate. Three baud rates are supported; 9600, 19200 and 38400. If using K-Bus this cell will not appear as the baud rate is fixed at 64 kbps.

16.9.2 IEC 60870-5-103

The specification IEC 60870-5-103 (Telecontrol Equipment and Systems Part 5 Section 103: Transmission Protocols), defines the use of standards IEC 60870-5-1 to IEC 60870-5-5, which were designed for communication with protection equipment.

This section describes how the IEC 60870-5-103 standard is applied to the Px40 platform. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 60870-5-103 standard.

This section should provide sufficient detail to enable understanding of the standard at a level required by most users.

The IEC 60870-5-103 interface is a master/slave interface with the device as the slave device. The device conforms to compatibility level 2, as defined in the IEC 60870-5-103.standard.

The following IEC 60870-5-103 facilities are supported by this interface:

- Initialization (reset)
- Time synchronization
- Event record extraction

- General interrogation
- Cyclic measurements
- General commands
- Disturbance record extraction
- Private codes

16.9.2.1 PHYSICAL CONNECTION AND LINK LAYER

Two connection options are available for IEC 60870-5-103:

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

If the optional fibre optic port is fitted, a menu item appears in which the active port can be selected. However, the selection is only effective following the next power up.

The IED address and baud rate can be selected using the front panel menu or by the settings application software.

16.9.2.2 INITIALISATION

Whenever the device has been powered up, or if the communication parameters have been changed a reset command is required to initialize the communications. The device will respond to either of the two reset commands; Reset CU or Reset FCB (Communication Unit or Frame Count Bit). The difference between the two commands is that the Reset CU command will clear any unsent messages in the transmit buffer, whereas the Reset FCB command does not delete any messages.

The device will respond to the reset command with an identification message ASDU 5. The Cause of Transmission (COT) of this response will be either Reset CU or Reset FCB depending on the nature of the reset command. The content of ASDU 5 is described in the IEC 60870-5-103 section of the Menu Database, available from GE Vernova separately if required.

In addition to the above identification message, it will also produce a power up event.

16.9.2.3 TIME SYNCHRONISATION

The time and date can be set using the time synchronization feature of the IEC 60870-5-103 protocol. The device will correct for the transmission delay as specified in IEC 60870-5-103. If the time synchronization message is sent as a send/confirm message then the device will respond with a confirm message. A time synchronization Class 1 event will be generated/produced whether the time-synchronization message is sent as a send confirm or a broadcast (send/no reply) message.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the IEC 60870-5-103 interface. An attempt to set the time via the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

16.9.2.4 CONFIGURABLE IEC 60870-5-103 SIGNAL LIST

From Software Version 91 onwards, there is a setting cell which allows the IEC 60870-5-103 private range signals to be selected and de-selected from IEC 60870-5-103 communication.

The IEC 60870-5-103 standard (compatible range) signals, that are provided according to the relay type and implementation, are always enabled. These signals cannot be disabled.

This setting cell is ***Config Mode*** in the *PROTOCOL CFG* column.

There are two settings associated with this cell. These are:

Setting	Description
Fixed	In this mode, the IED behaviour for IEC 60870-5-103 protocol is identical to pre-Software Version 91 IEDs. All the implemented signals (IEC 60870-5-103 compatible range and private range signals) are enabled for IEC 60870-5-103 communication. The COT behaviour will be according to the device IEC 60870-5-103 profile. This mode is provided for backward compatibility. This is the default setting.
Std+UserConfig	In this mode, the user can select which IEC 60870-5-103 private range signals are enabled for IEC 60870-5-103 communication. The selection is done using DDB mask setting cells in the *PROTOCOL CFG* column. The DDB mask value controls only the signal selection (enabled or disabled) for IEC 60870-5-103 communication. It does not modify the COT behaviour of the signals. The COT behaviour of the private range signals will be according to the device IEC 60870-5-103 profile. By default, only IEC 60870-5-103 standard signals are enabled. All private range signals are disabled.

When the ***Config Mode*** cell is set to `Std+UserConfig`, the DDB masks become visible in the *PROTOCOL CFG* column. These masks function in a similar way to the DDB masks in the *RECORD CONTROL* column. Editing these masks controls the DDB signals that are enabled for communication of the equivalent IEC 60870-5-103 private range signal, as listed in the IEC 60870-5-103 profile in the Menu Database.

Within these masks, only individual DDBs that are equivalent to IEC 60870-5-103 private range signals are editable. By default, all of the individual DDBs that are equivalent to IEC 60870-5-103 private range signals are set to 0 (zero), that is disabled for communication. Setting any individual DDB to 1 (one), enables the equivalent IEC 60870-5-103 private range signal for communication.

Within these masks, individual DDBs that are either equivalent to IEC 60870-5-103 standard range signals, or do not have any equivalent IEC 60870-5-103 private range signal, are not editable.

16.9.2.5 SPONTANEOUS EVENTS

Events are categorized using the following information:

- Function type
- Information Number

The IEC 60870-5-103 profile in the Menu Database contains a complete listing of all events produced by the device.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for spontaneous communication, by settting the ***Config Mode*** cell to `Std+UserConfig`, and configuring the DDB masks as required.

16.9.2.6 GENERAL INTERROGATION (GI)

The GI request can be used to read the status of the device, the function numbers, and information numbers that will be returned during the GI cycle. These are shown in the IEC 60870-5-103 profile in the Menu Database.

From Software Version 91 onwards, the IEC 60870-5-103 private range signals can be individually selected for GI reporting, by setting the ***Config Mode*** cell to `Std+UserConfig`, and configuring the DDB masks as required.

16.9.2.7 CYCLIC MEASUREMENTS

The device will produce measured values using ASDU 9 on a cyclical basis, this can be read from the device using a Class 2 poll (note ADSU 3 is not used). The rate at which the device produces new measured values can be controlled using the measurement period setting. This setting can be edited from the front panel menu or using MiCOM S1 Agile. It is active immediately following a change.

The device transmits its measurands with maximum value of 2.4 times the rated value of the measurement.

16.9.2.8 COMMANDS

A list of the supported commands is contained in the Menu Database. The device will respond to other commands with an ASDU 1, with a cause of transmission (COT) indicating ‘negative acknowledgement’.

16.9.2.9 TEST MODE

It is possible to disable the device output contacts to allow secondary injection testing to be performed using either the front panel menu or the front serial port. The IEC 60870-5-103 standard interprets this as ‘test mode’. An event will be produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted whilst the device is in test mode will have a COT of ‘test mode’.

16.9.2.10 DISTURBANCE RECORDS

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC 60870-5-103.

Note:
IEC 60870-5-103 only supports up to 8 records.

16.9.2.11 COMMAND/MONITOR BLOCKING

The device supports a facility to block messages in the monitor direction (data from the device) and also in the command direction (data to the device). Messages can be blocked in the monitor and command directions using one of the two following methods

- The menu command ***RP1 CS103Blcking*** in the *COMMUNICATIONS* column
- The DDB signals Monitor Blocked and Command Blocked

16.9.2.12 IEC 60870-5-103 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `IEC 60870-5-103`.
4. Move down to the next cell (***RP1 Address***). This cell controls the IEC 60870-5-103 address of the IED. Up to 32 IEDs can be connected to one spur. It is therefore necessary for each IED to have a unique address so that messages from the master control station are accepted by one IED only. IEC 60870-5-103 uses an integer number between 0 and 254 for the address. It is important that no two IEDs have the same IEC 60870 5 103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the IED.
5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Two baud rates are supported by the IED, `9600 bits/s` and `19200 bits/s`. Make sure that the baud rate selected on the IED is the same as that set on the master station.
6. Move down to the next cell (***RP1 Meas Period***). The next cell down controls the period between IEC 60870-5-103 measurements. The IEC 60870-5-103 protocol allows the IED to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.
7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
8. The next cell down (***RP1 CS103Blcking***) can be used for monitor or command blocking.
9. There are three settings associated with this cell; these are:

Setting	Description
Disabled	No blocking selected.
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energising an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the device returns a "Termination of general interrogation" message to the master station.
Command Blocking	When the command blocking DDB signal is active high, either by energising an opto input or control input, all remote commands will be ignored (i.e. CB Trip/Close, change setting group etc.). When in this mode the device returns a "negative acknowledgement of command" message to the master station.

16.9.3 DNP 3.0

This section describes how the DNP 3.0 standard is applied in the product. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the DNP 3.0 standard.

The descriptions given here are intended to accompany the device profile document that is included in the Menu Database document. The DNP 3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP 3.0 implementation. This is the standard format DNP 3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the device using DNP 3.0. The IED operates as a DNP 3.0 slave and supports subset level 2, as described in the DNP 3.0 standard, plus some of the features from level 3.

The DNP 3.0 protocol is defined and administered by the DNP Users Group. For further information on DNP 3.0 and the protocol specifications, please see the DNP website (www.dnp.org).

16.9.3.1 PHYSICAL CONNECTION AND LINK LAYER

DNP 3.0 can be used with EIA(RS)485.

Several connection options are available for DNP 3.0

- Rear Port 1 (RP1) - for permanent SCADA connection via RS485
- Optional fibre port (RP1 in slot A) - for permanent SCADA connection via optical fibre

The baud rate can be selected using the front panel menu or by the settings application software.

When using a serial interface, the data format is: 1 start bit, 8 data bits, 1 stop bit and optional configurable parity bit.

16.9.3.2 OBJECT 1 BINARY INPUTS

Object 1, binary inputs, contains information describing the state of signals in the IED, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and opto-inputs, alarm signals, and protection start and trip signals. The ‘DDB number’ column in the device profile document provides the DDB numbers for the DNP 3.0 point data. These can be used to cross-reference to the DDB definition list. See the relevant Menu Database document. The binary input points can also be read as change events using Object 2 and Object 60 for class 1-3 event data.

Note:
For the DNP Events to be transmitted it is mandatory to have the corresponding DDBs of the Configured Point Index to be included in the Courier Event Record. The RECORD CONTROL Menu lists all the DDBs, and the mask settings control their inclusion/exclusion as a Courier Event.

16.9.3.3 OBJECT 10 BINARY OUTPUTS

Object 10, binary outputs, contains commands that can be operated using DNP 3.0. Therefore the points accept commands of type pulse on (null, trip, close) and latch on/off as detailed in the device profile in the relevant Menu Database document, and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the Control Inputs. Described as Alias Control Inputs, they reflect the state of the Control Input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.
- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.

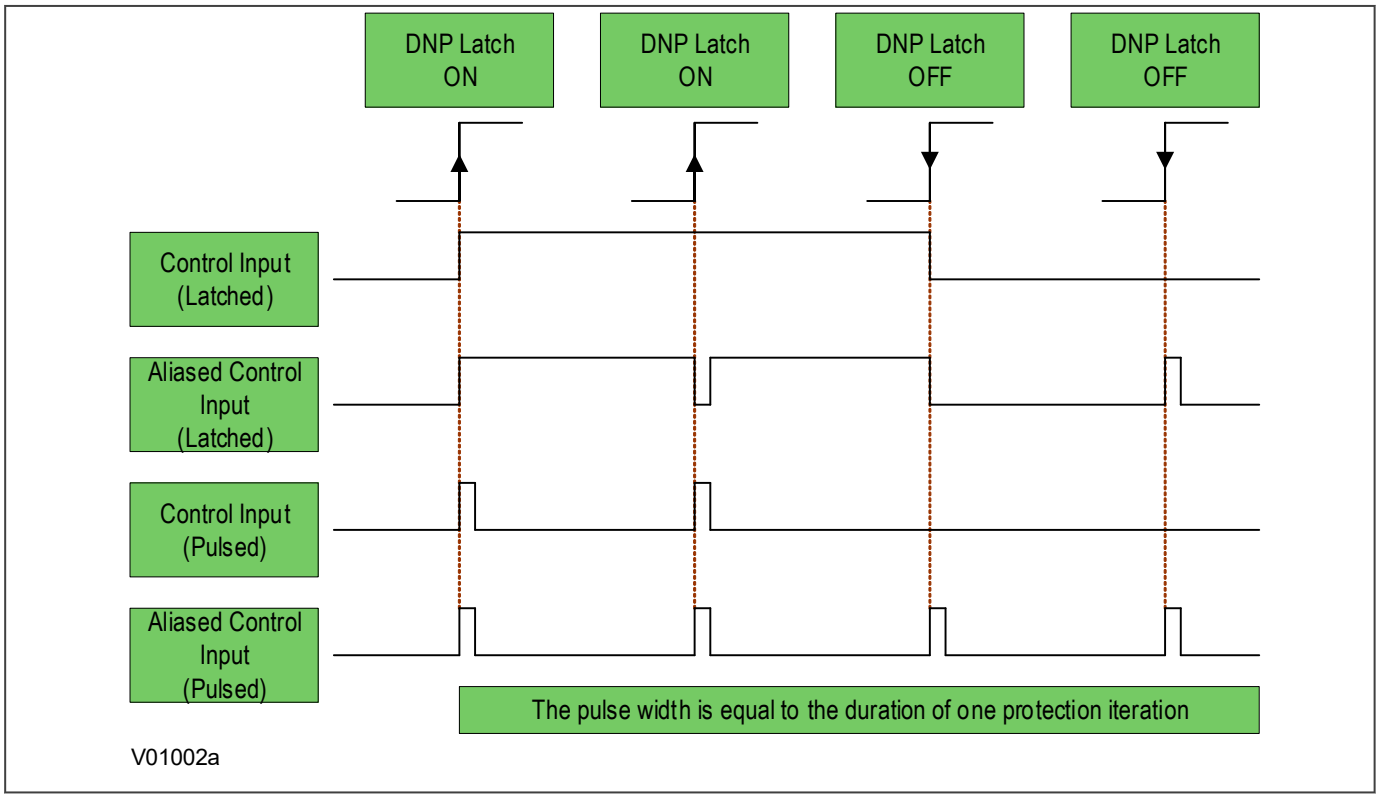


Figure 169: Control input behaviour

Many of the IED's functions are configurable so some of the Object 10 commands described in the following sections may not be available. A read from Object 10 reports the point as off-line and an operate command to Object 12 generates an error response.

Examples of Object 10 points that maybe reported as off-line are:

- Activate setting groups: Ensure setting groups are enabled
- CB trip/close: Ensure remote CB control is enabled
- Reset NPS thermal: Ensure NPS thermal protection is enabled
- Reset thermal O/L: Ensure thermal overload protection is enabled
- Reset RTD flags: Ensure RTD Inputs is enabled
- Control inputs: Ensure control inputs are enabled

16.9.3.4 OBJECT 20 BINARY COUNTERS

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from Object 20, or as a 'frozen' value from Object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding Object 21 frozen counter. The freeze and clear function resets the Object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from Object 22 and Object 23 respectively. Counter change events (Object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (Object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

16.9.3.5 OBJECT 30 ANALOGUE INPUT

Object 30, analogue inputs, contains information from the IED's measurements columns in the menu. All object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the IED's CT and VT ratios), and this is settable in the *COMMUNICATIONS* column in the IED. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using Object 32 or Object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analogue measurement that is unavailable when it is read is reported as offline. For example, the frequency would be offline if the current and voltage frequency is outside the tracking range of the IED. All Object 30 points are reported as secondary values in DNP 3.0 (with respect to CT and VT ratios).

16.9.3.6 OBJECT 40 ANALOGUE OUTPUT

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the IED such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

16.9.3.7 OBJECT 50 TIME SYNCHRONISATION

Function codes 1 (read) and 2 (write) are supported for Object 50 (time and date) variation 1. The DNP Need Time function (the duration of time waited before requesting another time sync from the master) is supported, and is configurable in the range 1 - 30 minutes.

If the clock is being synchronized using the IRIG-B input then it will not be possible to set the device time using the Courier interface. An attempt to set the time using the interface will cause the device to create an event with the current date and time taken from the IRIG-B synchronized internal clock.

16.9.3.8 DNP3 DEVICE PROFILE

This section describes the specific implementation of DNP version 3.0 within GE Vernova MiCOM P40 Agile IEDs for both compact and modular ranges.

The devices use the DNP 3.0 Slave Source Code Library version 3 from Triangle MicroWorks Inc.

This document, in conjunction with the DNP 3.0 Basic 4 Document Set, and the DNP Subset Definitions Document, provides complete information on how to communicate with the devices using the DNP 3.0 protocol.

This implementation of DNP 3.0 is fully compliant with DNP 3.0 Subset Definition Level 2. It also contains many Subset Level 3 and above features.

16.9.3.8.1 DNP3 DEVICE PROFILE TABLE

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a “Document”, it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

The following table provides the device profile in a similar format to that defined in the DNP 3.0 Subset Definitions Document. While it is referred to in the DNP 3.0 Subset Definitions as a "Document", it is just one component of a total interoperability guide. This table, in combination with the subsequent Implementation and Points List tables should provide a complete interoperability/configuration guide for the device.

DNP 3.0 Device Profile Document	
Vendor Name:	GE Vernova
Device Name:	MiCOM P40Agile Protection Relays - compact and modular range
Models Covered:	All models
Highest DNP Level Supported*: * This is the highest DNP level FULLY supported. Parts of level 3 are also supported	For Requests: Level 2 For Responses: Level 2
Device Function:	Slave
Notable objects, functions, and/or qualifiers supported in addition to the highest DNP levels supported (the complete list is described in the DNP 3.0 Implementation Table): For static (non-change event) object requests, request qualifier codes 00 and 01 (start-stop), 07 and 08 (limited quantity), and 17 and 28 (index) are supported in addition to the request qualifier code 06 (no range (all points)) Static object requests sent with qualifiers 00, 01, 06, 07, or 08 will be responded with qualifiers 00 or 01 Static object requests sent with qualifiers 17 or 28 will be responded with qualifiers 17 or 28 For change-event object requests, qualifiers 17 or 28 are always responded 16-bit and 32-bit analogue change events with time may be requested The read function code for Object 50 (time and date) variation 1 is supported Analogue Input Deadbands, Object 34, variations 1 through 3, are supported Floating Point Analogue Output Status and Output Block Objects 40 and 41 are supported Sequential file transfer, Object 70, variations 2 through 7, are supported Device Attribute Object 0 is supported	
Maximum Data Link Frame Size (octets):	Transmitted: 292 Received: 292
Maximum Application Fragment Size (octets)	Transmitted: Configurable (100 to 2048). Default 2048 Received: 249
Maximum Data Link Retries:	Fixed at 2
Maximum Application Layer Retries:	None
Requires Data Link Layer Confirmation:	Configurable to Never or Always
Requires Application Layer Confirmation:	When reporting event data (Slave devices only) When sending multi-fragment responses (Slave devices only)
Timeouts while waiting for:	
Data Link Confirm:	Configurable
Complete Application Fragment:	None
Application Confirm:	Configurable
Complete Application Response:	None
Others:	
Data Link Confirm Timeout:	Configurable from 0 (Disabled) to 120s, default 10s.
Application Confirm Timeout:	Configurable from 1 to 120s, default 2s.

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Select/Operate Arm Timeout:	Configurable from 1 to 10s, default 10s.
Need Time Interval (Set IIN1-4):	Configurable from 1 to 30, default 10min.
Application File Timeout	60 s
Analog Change Event Scan Period:	Fixed at 0.5s
Counter Change Event Scan Period	Fixed at 0.5s
Frozen Counter Change Event Scan Period	Fixed at 1s
Maximum Delay Measurement Error:	2.5 ms
Time Base Drift Over a 10-minute Interval:	7 ms
Sends/Executes Control Operations:	
Write Binary Outputs:	Never
Select/Operate:	Always
Direct Operate:	Always
Direct Operate - No Ack:	Always
Count > 1	Never
Pulse On	Always
Pulse Off	Sometimes
Latch On	Always
Latch Off	Always
Queue	Never
Clear Queue	Never
Note: Paired Control points will accept Pulse On/Trip and Pulse On/Close, but only single point will accept the Pulse Off control command.	
Reports Binary Input Change Events when no specific variation requested:	Configurable to send one or the other
Reports time-tagged Binary Input Change Events when no specific variation requested:	Binary input change with time
Sends Unsolicited Responses:	Never
Sends Static Data in Unsolicited Responses:	Never No other options are permitted
Default Counter Object/Variation:	Configurable, Point-by-point list attached Default object: 20 Default variation: 1
Counters Roll Over at:	32 bits
Sends multi-fragment responses:	Yes
Sequential File Transfer Support:	
Append File Mode	No
Custom Status Code Strings	No
Permissions Field	Yes
File Events Assigned to Class	No
File Events Send Immediately	Yes
Multiple Blocks in a Fragment	No
Max Number of Files Open	1

16.9.3.8.2 DNP3 IMPLEMENTATION TABLE

The implementation table provides a list of objects, variations and control codes supported by the device:

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
1	0	Binary Input (Variation 0 is used to request default variation)	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
1	1 (default - see note 1)	Binary Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
1	2	Binary Input with Flag	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
2	0	Binary Input Change - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
2	1	Binary Input Change without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
2	2	Binary Input Change with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
10	0	Binary Output Status - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
10	2 (default - see note 1)	Binary Output Status	1	(read)	00, 01 06 07, 08 17, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
12	1	Control Relay Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28	(index)	129	response		echo of request
20	0	Binary Counter - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
			7 8 9 10	(freeze) (freeze noack) (freeze clear) (frz. cl. Noack)	00, 01 06 07, 08	(start-stop) (no range, or all) (limited qty)				
20	1	32-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	2	16-Bit Binary Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	5 (default - see note 1)	32-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
20	6	16-Bit Binary Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	0	Frozen Counter - Any Variation	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
21	1	32-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
21	2	16-Bit Frozen Counter with Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	5	32-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 1)
21	6	16-Bit Frozen Counter with Time of Freeze	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) 17, 28 (index - see note 1)
21	9 (default - see note 1)	32-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
21	10	16-Bit Frozen Counter without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
`22	0	Counter Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
22	1 (default - see note 1)	32-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	2	16-Bit Counter Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	5	32-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
22	6	16-Bit Counter Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	0	Frozen Counter Event (Variation 0 is used to request default variation)	1	(read)	06 07, 08	(no range, or all) (limited qty)				
23	1 (default - see note 1)	32-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	2	16-Bit Frozen Counter Event	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	5	32-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
23	6	16-Bit Frozen Counter Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
30	0	Analog Input - Any Variation	1 22	(read) (assign class)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
30	1	32-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	2	16-Bit Analog Input	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	3 (default - see note 1)	32-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	4	16-Bit Analog Input without Flag	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
30	5	Short floating point	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
32	0	Analog Change Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
32	1 (default - see note 1)	32-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	2	16-Bit Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	3	32-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	4	16-Bit Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	5	Short floating point Analog Change Event without Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
32	7	Short floating point Analog Change Event with Time	1	(read)	06 07, 08	(no range, or all) (limited qty)	129	response	17, 28	(index)
34	0	Analog Input Deadband (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
34	1	16 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	2 (default - see note 1)	32 Bit Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
34	3	Short Floating Point Analog Input Deadband	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
			2	(write)	00, 01 07, 08 17, 27, 28	(start-stop) (limited qty) (index)				
40	0	Analog Output Status (Variation 0 is used to request default variation)	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)				
40	1 (default - see note 1)	32-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	2	16-Bit Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
40	3	Short Floating Point Analog Output Status	1	(read)	00, 01 06 07, 08 17, 27, 28	(start-stop) (no range, or all) (limited qty) (index)	129	response	00, 01 17, 28	(start-stop) (index - see note 2)
41	1	32-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request
41	2	16-Bit Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 28 27	(index) (index)	129	response		echo of request

Object			Request (Library will parse)				Response (Library will respond with)			
Object Number	Variation Number	Description	Function Codes (dec)		Qualifier Codes (hex)		Function Codes (dec)		Qualifier Codes (hex)	
41	3	Short Floating Point Analog Output Block	3 4 5 6	(select) (operate) (direct op) (dir. op, noack)	17, 27, 28	(index)	129	response		echo of request
50	1 (default - see note 1)	Time and Date	1	(read)	07	(limited qty = 1)	129	response	07	(limited qty = 1)
			2	(write)	07	(limited qty = 1)				
60	0	Not defined								
60	1	Class 0 Data	1	(read)	06	(no range, or all)				
60	2	Class 1 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	3	Class 2 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
60	4	Class 3 Data	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	0	File Event - Any Variation	1	(read)	06 07, 08	(no range, or all) (limited qty)				
			22	(assign class)	06	(no range, or all)				
70	2	File Authentication	29	(authenticate)	5b	(free-format)	129	response		5B (free-format)
70	3	File Command	25 27	(open) (delete)	5b	(free-format)				
70	4	File Command Status	26 30	(close) (abort)	5b	(free-format)	129	response		5B (free-format)
70	5	File Transfer	1	(read)	5b	(free-format)	129	response		5B (free-format)
70	6	File Transfer Status					129	response		5B (free-format)
70	7	File Descriptor	28	(get file info)	5b	(free-format)	129	response		5B (free-format)
80	1	Internal Indications	1	(read)	00, 01	(start-stop)	129	response	00, 01	(start-stop)
		No Object (function code only)	13	(cold restart)						
		No Object (function code only)	14	(warm restart)						
		No Object (function code only)	23	(delay meas.)						

Note:
A Default variation refers to the variation responded to when variation 0 is requested and/or in class 0, 1, 2, or 3 scans.

Note:
For static (non-change-event) objects, qualifiers 17 or 28 are only responded to when a request is sent with qualifiers 17 or 28, respectively. Otherwise, static object requests sent with qualifiers 00, 01, 06, 07, or 08, will be responded to with qualifiers 00 or 01. For change-event objects, qualifiers 17 or 28 are always responded to.

16.9.3.8.3 DNP3 INTERNAL INDICATIONS

The following table lists the DNP3.0 Internal Indications (IIN) and identifies those that are supported by the device.

The IIN form an information element used to convey the internal states and diagnostic results of a device. This information can be used by a receiving station to perform error recovery or other suitable functions. The IIN is a two-octet field that follows the function code in all responses from the device. When a request cannot be processed due to formatting errors or the requested data is not available, the IIN is always returned with the appropriate bits set.

Bit	Indication	Description	Supported
Octet 1			
0	All stations message received	Set when a request is received with the destination address of the all stations address (6553510). It is cleared after the next response (even if a response to a global request is required). This IIN is used to let the master station know that a "broadcast" message was received by the relay.	Yes
1	Class 1 data available	Set when data that has been configured as Class 1 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
2	Class 2 data available	Set when data that has been configured as Class 2 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
3	Class 3 data available	Set when data that has been configured as Class 3 data is ready to be sent to the master. The master station should request this class data from the relay when this bit is set in a response.	Yes
4	Time-synchronisation required	The relay requires time synchronization from the master station (using the Time and Date object). This IIN is cleared once the time has been synchronised. It can also be cleared by explicitly writing a 0 into this bit of the Internal Indication object.	Yes
5	Local	Set when some or all of the relays digital output points (Object 10/12) are in the Local state. That is, the relays control outputs are NOT accessible through the DNP protocol. This IIN is clear when the relay is in the Remote state. That is, the relays control outputs are fully accessible through the DNP protocol.	No
6	Device in trouble	Set when an abnormal condition exists in the relay. This IIN is only used when the state cannot be described by a combination of one or more of the other IIN bits.	No
7	Device restart	Set when the device software application restarts. This IIN is cleared when the master station explicitly writes a 0 into this bit of the Internal Indications object.	Yes
Octet 2			
0	Function code not implemented	The received function code is not implemented within the relay.	Yes
1	Requested object(s) unknown	The relay does not have the specified objects or there are no objects assigned to the requested class. This IIN should be used for debugging purposes and usually indicates a mismatch in device profiles or configuration problems.	Yes
2	Out of range	Parameters in the qualifier, range or data fields are not valid or out of range. This is a 'catch-all' for application request formatting errors. It should only be used for debugging purposes. This IIN usually indicates configuration problems.	Yes
3	Buffer overflow	Event buffer(s), or other application buffers, have overflowed. The master station should attempt to recover as much data as possible and indicate to the user that there may be lost data. The appropriate error recovery procedures should be initiated by the user.	Yes

Bit	Indication	Description	Supported
4	Already executing	The received request was understood but the requested operation is already executing.	
5	Bad configuration	Set to indicate that the current configuration in the relay is corrupt. The master station may download another configuration to the relay.	Yes
6	Reserved	Always returned as zero.	
7	Reserved	Always returned as zero.	

16.9.3.8.4 DNP3 RESPONSE STATUS CODES

When the device processes Control Relay Output Block (Object 12) requests, it returns a set of status codes; one for each point contained within the original request. The complete list of codes appears in the following table:

Code Number	Identifier Name	Description
0	Success	The received request has been accepted, initiated, or queued.
1	Timeout	The request has not been accepted because the 'operate' message was received after the arm timer (Select Before Operate) timed out. The arm timer was started when the select operation for the same point was received.
2	No select	The request has not been accepted because no previous matching 'select' request exists. (An 'operate' message was sent to activate an output that was not previously armed with a matching 'select' message).
3	Format error	The request has not been accepted because there were formatting errors in the control request ('select', 'operate', or 'direct operate').
4	Not supported	The request has not been accepted because a control operation is not supported for this point.
5	Already active	The request has not been accepted because the control queue is full or the point is already active.
6	Hardware error	The request has not been accepted because of control hardware problems.
7	Local	The request has not been accepted because local access is in progress.
8	Too many operations	The request has not been accepted because too many operations have been requested.
9	Not authorized	The request has not been accepted because of insufficient authorisation.
127	Undefined	The request not been accepted because of some other undefined reason.

Note:
Code numbers 10 through to 126 are reserved for future use.

16.9.3.8.5 DNP3 CONFIGURATION

To configure the device:

1. Select the *CONFIGURATION* column and check that the ***Comms settings*** cell is set to `Visible`.
2. Select the *COMMUNICATIONS* column.
3. Move to the first cell down (***RP1 Protocol***). Set this to the chosen communication protocol – in this case `DNP3.0`.
4. Move down to the next cell (***RP1 Address***). This cell controls the DNP3.0 address of the IED. Up to 32 IEDs can be connected to one spur, therefore it is necessary for each IED to have a unique address so that messages from the master control station are accepted by only one IED. DNP3.0 uses a decimal number between 1 and 65519 for the Relay Address. It is important that no two IEDs have the same address.

5. Move down to the next cell (***RP1 Baud Rate***). This cell controls the baud rate to be used. Six baud rates are supported by the IED 1200 bps, 2400 bps, 4800 bps, 9600 bps, 19200 bps and 38400 bps. Make sure that the baud rate selected on the IED is the same as that set on the master station.
6. Move down to the next cell (***RP1 Parity***). This cell controls the parity format used in the data frames. The parity can be set to be one of `None`, `Odd` or `Even`. Make sure that the parity format selected on the IED is the same as that set on the master station.
7. If the optional fibre optic connectors are fitted, the ***RP1 PhysicalLink*** cell is visible. This cell controls the physical media used for the communication (Copper or Fibre optic).
8. Move down to the next cell (***RP1 Time Sync***). This cell affects the time synchronisation request from the master by the IED. It can be set to `enabled` or `disabled`. If enabled it allows the DNP3.0 master to synchronise the time on the IED.

16.9.3.8.5.1 DNP3 CONFIGURATOR

A PC support package for DNP3.0 is available as part of the supplied settings application software (MiCOM S1 Agile) to allow configuration of the device's DNP3.0 response. The configuration data is uploaded from the device to the PC in a block of compressed format data and downloaded in a similar manner after modification. The new DNP3.0 configuration takes effect after the download is complete. To restore the default configuration at any time, from the *CONFIGURATION* column, select the ***Restore Defaults*** cell then select `All Settings`.

In MiCOM S1 Agile, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

If the device supports DNP Over Ethernet, the configuration related settings are done in the folder **DNP Over Ethernet**.

16.9.4 IEC 61850

This section describes how the IEC 61850 standard is applied to GE Vernova products. It is not a description of the standard itself. The level at which this section is written assumes that the reader is already familiar with the IEC 61850 standard.

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions within a substation, and additionally provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security that is so essential in substations today.

There are two editions of most parts of the IEC 61850 standard; edition 1 and edition 2. This product supports IEC 61850 edition 2 only.

16.9.4.1 BENEFITS OF IEC 61850

The standard provides:

- Standardised models for IEDs and other equipment within the substation
- Standardised communication services (the methods used to access and exchange data)
- Standardised formats for configuration files
- Peer-to-peer communication

The standard adheres to the requirements laid out by the ISO OSI model and therefore provides complete vendor interoperability and flexibility on the transmission types and protocols used. This includes mapping of data onto

Ethernet, which is becoming more and more widely used in substations, in favour of RS485. Using Ethernet in the substation offers many advantages, most significantly including:

- Ethernet allows high-speed data rates (currently 100 Mbps, rather than tens of kbps or less used by most serial protocols)
- Ethernet provides the possibility to have multiple clients
- Ethernet is an open standard in every-day use
- There is a wide range of Ethernet-compatible products that may be used to supplement the LAN installation (hubs, bridges, switches)

16.9.4.2 IEC 61850 INTEROPERABILITY

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs, which allows interoperability between products from multiple vendors.

An IEC 61850-compliant device may be interoperable, but this does not mean it is interchangeable. You cannot simply replace a product from one vendor with that of another without reconfiguration. However, the terminology is pre-defined and anyone with prior knowledge of IEC 61850 should be able to integrate a new device very quickly without having to map all of the new data. IEC 61850 brings improved substation communications and interoperability to the end user, at a lower cost.

16.9.4.3 THE IEC 61850 DATA MODEL

The data model of any IEC 61850 IED can be viewed as a hierarchy of information, whose nomenclature and categorization is defined and standardized in the IEC 61850 specification.

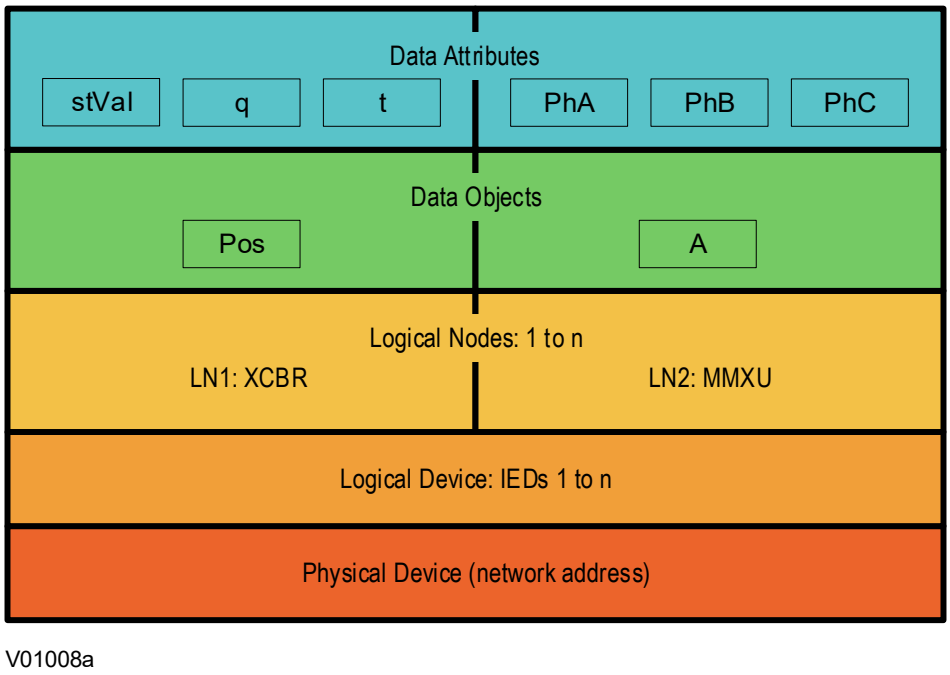

Figure 170: Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

Data Frame format

Layer	Description
Physical Device	Identifies the actual IED within a system. Typically the device's name or IP address can be used (for example Feeder_1 or 10.0.0.2.
Logical Device	Identifies groups of related Logical Nodes within the Physical Device. For the MiCOM IEDs, multiple Logical Devices exist, for System (root LD) and various Control, Measurements, Protection, and Records LDs.
Wrapper/Logical Node Instance	Identifies the major functional areas within the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
Data Object	This next layer is used to identify the type of data you will be presented with. For example, Pos (position) of Logical Node type XCBR.
Data Attribute	This is the actual data (measurement value, status, description, etc.). For example, stVal (status value) indicating actual position of circuit breaker for Data Object type Pos of Logical Node type XCBR.

16.9.4.4 IEC 61850 IN MICOM IEDS

IEC 61850 is implemented by use of a separate Ethernet board. This Ethernet board manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection functions.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a bay computer (MiCOM C264)
- An HMI
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge of the IED

The IEC 61850 compatible interface standard provides capability for the following:

- Read access to measurements
- Refresh of all measurements at a standard rate.
- Generation of non-buffered and buffered multi-client reports on change of status or measurement
- SNTP time synchronization over an Ethernet link. (This is used to synchronize the IED's internal real time clock.
- GOOSE peer-to-peer communication
- Disturbance record extraction by IEC 61850 MMS file transfer. The record is extracted as an ASCII format COMTRADE file
- Controls (Direct and Select Before Operate)

Note:
Setting changes are not supported in the current IEC 61850 implementation. Currently these setting changes are carried out using the settings application software.

16.9.4.5 IEC 61850 DATA MODEL IMPLEMENTATION

The data model naming adopted in the IEDs has been standardised for consistency. The Logical Nodes are allocated under Logical Devices, as appropriate.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available as a separate document.

16.9.4.6 IEC 61850 COMMUNICATION SERVICES IMPLEMENTATION

The IEC 61850 communication services which are implemented in the IEDs are described in the Protocol Implementation Conformance Statement (PICS) document, which is available as a separate document.

16.9.4.7 IEC 61850 PEER-TO-PEER (GOOSE) COMMUNICATIONS

The implementation of IEC 61850 Generic Object Oriented Substation Event (GOOSE) enables faster communication between IEDs offering the possibility for a fast and reliable system-wide distribution of input and output data values. The GOOSE model uses multicast services to deliver event information. Multicast messaging means that messages are sent to selected devices on the network. The receiving devices can specifically accept frames from certain devices and discard frames from the other devices. It is also known as a publisher-subscriber system. When a device detects a change in one of its monitored status points it publishes a new message. Any device that is interested in the information subscribes to the data it contains.

16.9.4.8 GOOSE MESSAGE VALIDATION

Whenever a new GOOSE message is received its validity is checked before the dataset is decoded and used to update the Programmable Scheme Logic. As part of the validation process a check is made for state and sequence number anomalies. If an anomaly is detected, the 'out-of-order' GOOSE message is discarded. When a message is discarded the last valid message remains active until a new valid GOOSE message is received or its validity period (TAL) expires.

Out-of-order GOOSE message indicators and reporting are provided to the subscriber via the IEC61850 LGOS logical node.

16.9.4.9 MAPPING GOOSE MESSAGES TO VIRTUAL INPUTS

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the virtual inputs within the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

An IED can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

16.9.4.10 IEC 61850 GOOSE CONFIGURATION

All GOOSE configuration is performed using the IEC 61850 Configurator tool available in the MiCOM S1 Agile software application.

All GOOSE publishing configuration can be found under the **GOOSE Publishing** tab in the configuration editor window. All GOOSE subscription configuration parameters are under the **External Binding** tab in the configuration editor window.

Settings to enable GOOSE signalling and to apply Test Mode are available using the HMI.

16.9.4.11 ETHERNET FUNCTIONALITY

IEC 61850 **Associations** are unique and made between the client and server. If Ethernet connectivity is lost for any reason, the associations are lost, and will need to be re-established by the client. The IED has a **TCP_KEEPALIVE** function to monitor each association, and terminate any which are no longer active.

The IED allows the re-establishment of associations without disruption of its operation, even after its power has been removed. As the IED acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost, and reports requested by connected clients are reset. The client must re-enable these when it next creates the new association to the IED.

16.9.4.12 IEC 61850 CONFIGURATION

To configure the device for IEC 61850, it is recommended to use the IEC 61850 IED Configurator, which is part of the settings application software. You can also configure it with the HMI. To configure IEC61850 edition 2 using the HMI, you must first enable the IP From HMI setting, after which you can set the media (copper or fibre), IP address, subnet mask and gateway address.

IEC 61850 allows IEDs to be directly configured from a configuration file. The IED's system configuration capabilities are determined from an IED Capability Description file (ICD), supplied with the product. By using ICD files from the products to be installed, you can design, configure and test (using simulation tools), a substation's entire protection scheme before the products are installed into the substation.

To help with this process, the settings application software provides an IEC 61850 Configurator tool, which allows the pre-configured IEC 61850 configuration file to be imported and transferred to the IED. As well as this, you can manually create configuration files for all products, based on their original IED capability description (ICD file).

Other features include:

- The extraction of configuration data for viewing and editing.
- A sophisticated error checking sequence to validate the configuration data before sending to the IED.

Note:
Some configuration data is available in the IEC61850 CONFIG. column, allowing read-only access to basic configuration data.

16.9.4.12.1 IEC 61850 CONFIGURATION BANKS

There are two configuration banks:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the IED is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration.

Following an upgrade, the IEC 61850 Configurator tool can be used to transmit a command, which authorises activation of the new configuration contained in the inactive configuration bank. This is done by switching the active and inactive configuration banks. The capability of switching the configuration banks is also available using the *IEC61850 CONFIG.* column of the HMI.

The SCL Name and Revision attributes of both configuration banks are available in the *IEC61850 CONFIG.* column of the HMI.

16.9.4.12.2 IEC 61850 NETWORK CONNECTIVITY

Configuration of the IP parameters and SNTP (Simple Network Time Protocol) time synchronisation parameters is performed by the IEC 61850 Configurator tool. If these parameters are not available using an SCL (Substation Configuration Language) file, they must be configured manually.

Every IP address on the Local Area Network must be unique. Duplicate IP addresses result in conflict and must be avoided. Most IEDs check for a conflict on every IP configuration change and at power up and they raise an alarm if an IP conflict is detected.

The IED can be configured to accept data from other networks using the ***Gateway*** setting. If multiple networks are used, the IP addresses must be unique across networks.

16.9.4.13 IEC 61850 EDITION 2

Many parts of the IEC 61850 standard have now been released as the second edition. This offers some significant enhancements including:

- Improved interoperability
- Many new logical nodes
- Better defined testing; it is now possible to perform off-line testing and simulation of functions

Edition 2 implementation requires use of version 3.8 of the IEC 61850 configurator, which is installed with version 2.0.1 of MiCOM S1 Agile.

16.9.4.13.1 BACKWARD COMPATIBILITY

IEC61850 System - Backward compatibility

An Edition 1 IED can operate with an Edition 2 IEC 61850 system, provided that the Edition 1 IEDs do not subscribe to GOOSE messages with data objects or data attributes which are only available in Edition 2.

The following figure explains this concept:

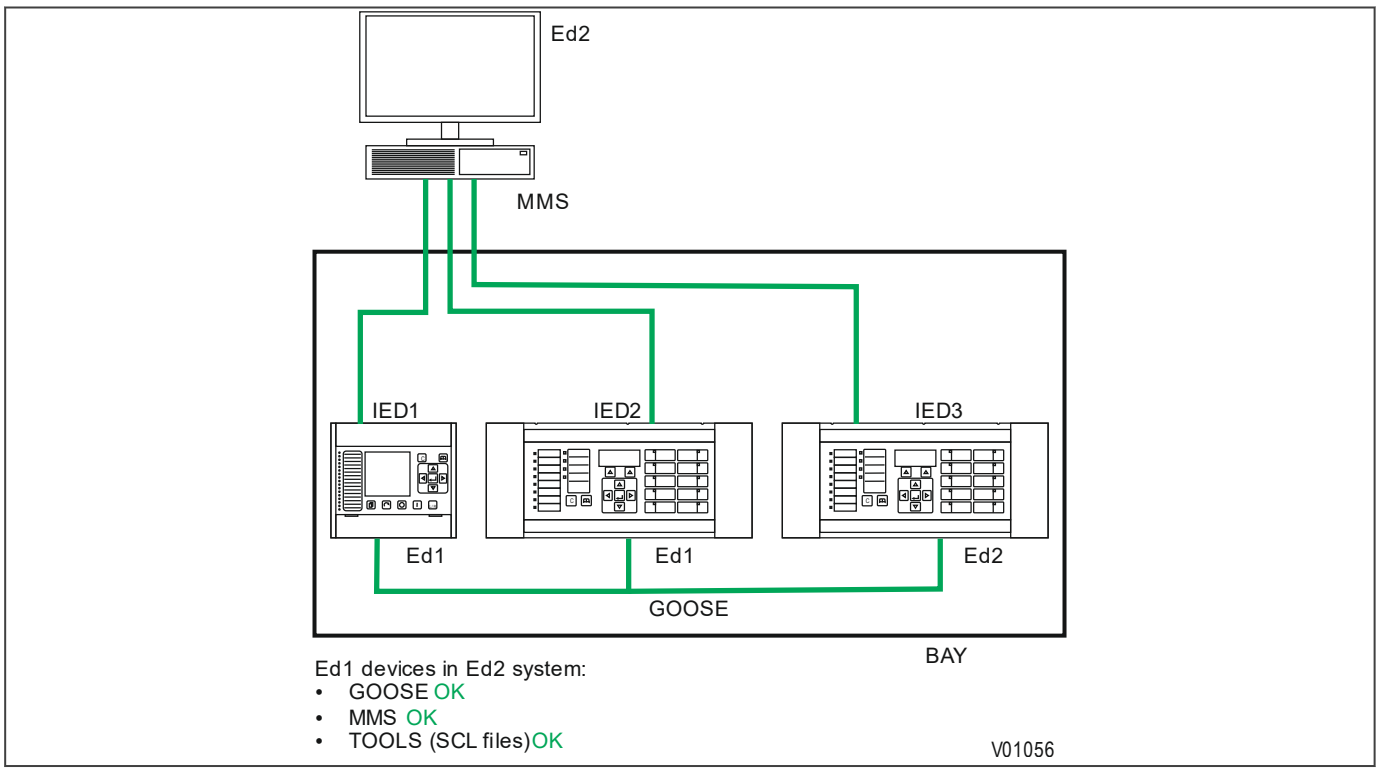

Figure 171: Edition 2 system - backward compatibility

An Edition 2 IED cannot normally operate within an Edition 1 IEC 61850 system. An Edition 2 IED can work for GOOSE messaging in a mixed system, providing the client is compatible with Edition 2.

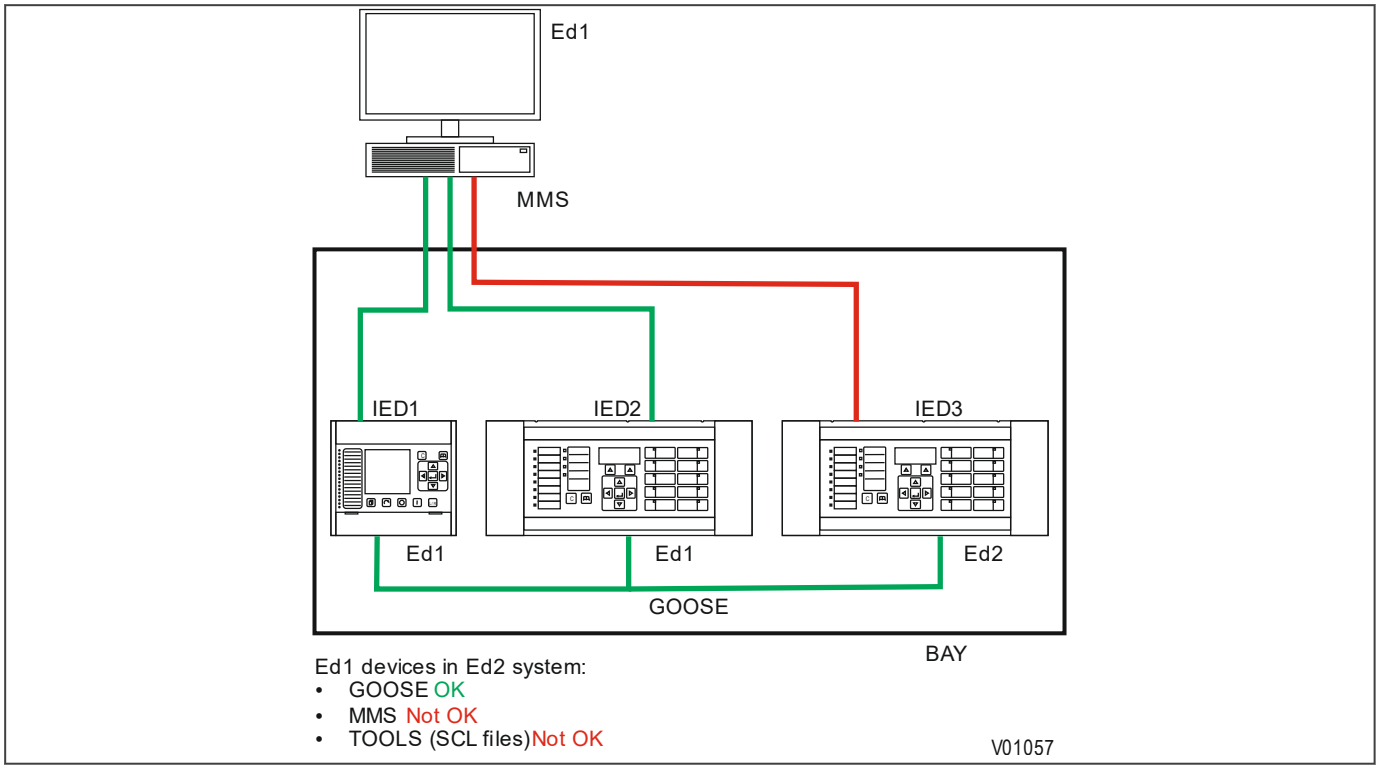

Figure 172: Edition 1 system - forward compatibility issues

16.9.4.13.2 EDITION-2 COMMON DATA CLASSES

The following common data classes (CDCs) are new to Edition 2 and therefore should not be used in GOOSE control blocks in mixed Edition 1 and Edition 2 systems

- Histogram (HST)
- Visible string status (VSS)
- Object reference setting (ORG)
- Controllable enumerated status (ENC)
- Controllable analogue process value (APC)
- Binary controlled analogue process value (BAC)
- Enumerated status setting (ENG)
- Time setting group (TSG)
- Currency setting group (CUG)
- Visible string setting (VSG)
- Curve shape setting (CSG)

Of these, only ENS and ENC types are available from a MiCOM P40 IED when publishing GOOSE messages, so Data Objects using these Common Data Classes should not be published in mixed Edition 1 and Edition 2 systems.

For compatibility between Edition 1 and Edition 2 IEDs, SCL files using SCL schema version "2.1" must be used. For a purely Edition 2 system, use the schema version "2007B4".

16.9.5 READ ONLY MODE

With IEC 61850 and Ethernet/Internet communication capabilities, security has become an important issue. For this reason, all relevant GE Vernova IEDs have been adapted to comply with the latest cyber-security standards.

In addition to this, a facility is provided which allows you to enable or disable the communication interfaces. This feature is available for products using Courier, IEC 60870-5-103, or IEC 61850.

16.9.5.1 IEC 60870-5-103 PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with IEC 60870-5-103, the following commands are blocked at the interface:

- Write parameters (=change setting) (private ASDUs)
- General Commands (ASDU20), namely:
  - INF16 auto-recloser on/off
  - INF19 LED reset
  - Private INFs (for example: CB open/close, Control Inputs)

The following commands are still allowed:

- Poll Class 1 (Read spontaneous events)
- Poll Class 2 (Read measurands)
- GI sequence (ASDU7 'Start GI', Poll Class 1)
- Transmission of Disturbance Records sequence (ASDU24, ASDU25, Poll Class 1)
- Time Synchronisation (ASDU6)
- General Commands (ASDU20), namely:
  - INF23 activate characteristic 1
  - INF24 activate characteristic 2
  - INF25 activate characteristic 3
  - INF26 activate characteristic 4

Note:
For IEC 60870-5-103, Read Only Mode function is different from the existing Command block feature.

16.9.5.2 COURIER PROTOCOL BLOCKING

If Read-Only Mode is enabled for RP1 or RP2 with Courier, the following commands are blocked at the interface:

- Write settings
- All controls, including:
  - Reset Indication (Trip LED)
  - Operate Control Inputs
  - CB operations
  - Auto-reclose operations
  - Reset demands
  - Clear event/fault/maintenance/disturbance records
  - Test LEDs & contacts

The following commands are still allowed:

- Read settings, statuses, measurands
- Read records (event, fault, disturbance)
- Time Synchronisation
- Change active setting group

16.9.5.3 IEC 61850 PROTOCOL BLOCKING

If Read-Only Mode is enabled for the Ethernet interfacing with IEC 61850, the following commands are blocked at the interface:

- All controls, including:
  - Enable/disable protection
  - Operate Control Inputs
  - CB operations (Close/Trip, Lock)
  - Reset LEDs

The following commands are still allowed:

- Read statuses, measurands
- Generate reports
- Extract disturbance records
- Time synchronisation
- Change active setting group

16.9.5.4 READ-ONLY SETTINGS

The following settings are available for enabling or disabling Read Only Mode.

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

16.9.5.5 READ-ONLY DDB SIGNALS

The remote read only mode is also available in the PSL using three dedicated DDB signals:

- RP1 Read Only
- RP2 Read Only (only for products that have RP2)
- NIC Read Only (where Ethernet is available)

Using the PSL, these signals can be activated by opto-inputs, Control Inputs and function keys if required.

16.10 TIME SYNCHRONISATION

In modern protection schemes it is necessary to synchronise the IED's real time clock so that events from different devices can be time stamped and placed in chronological order. This is achieved in various ways depending on the chosen options and communication protocols.

- Using the IRIG-B input (if fitted)
- Using the SNTP time protocol (for Ethernet IEC 61850 versions)
- Using IEEE 1588 Precision Time Protocol (PTP)
- By using the time synchronisation functionality inherent in the data protocols

The time synchronisation sources can be configured in a priority order using the Primary Source and Secondary Source cells in the DATE AND TIME column. If the Primary source becomes unavailable, the Secondary source will be used, if available.

16.10.1 IRIG-B

IRIG stands for Inter Range Instrumentation Group, which is a standards body responsible for standardising different time code formats. There are several different formats starting with IRIG-A, followed by IRIG-B and so on. The letter after the "IRIG" specifies the resolution of the time signal in pulses per second (PPS). IRIG-B, the one which we use has a resolution of 100 PPS. IRIG-B is used when accurate time-stamping is required.

The following diagram shows a typical GPS time-synchronised substation application. The satellite RF signal is picked up by a satellite dish and passed on to receiver. The receiver receives the signal and converts it into time signal suitable for the substation network. IEDs in the substation use this signal to govern their internal clocks and event recorders.

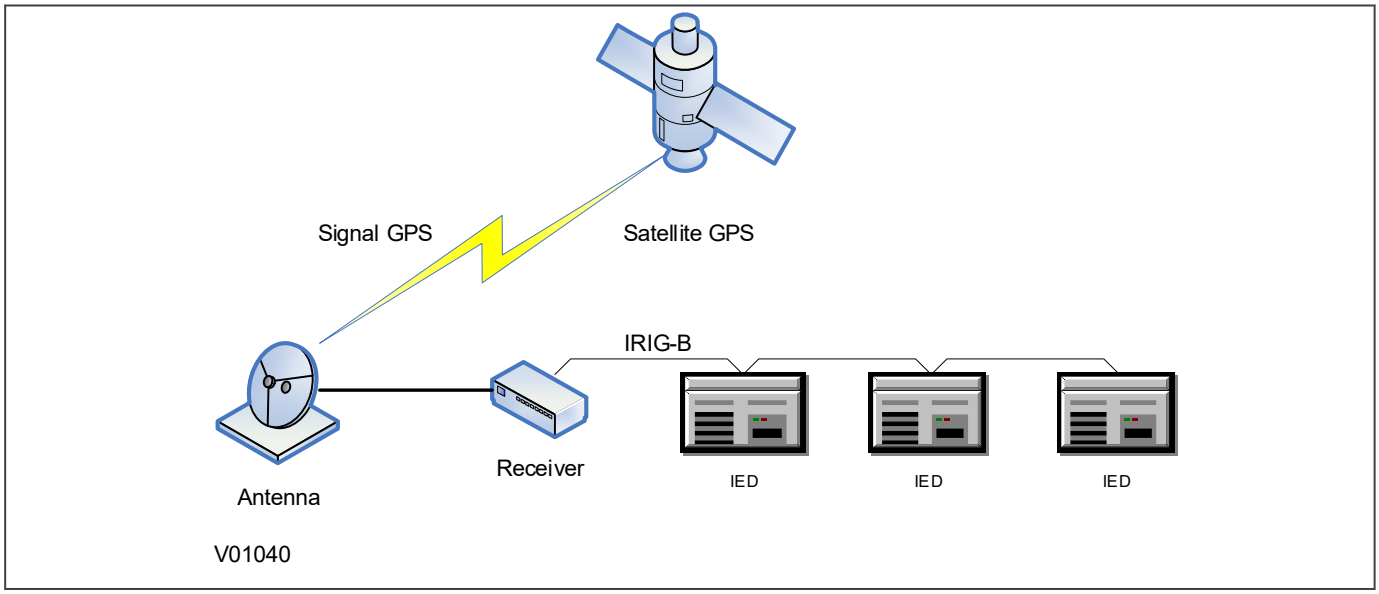

Figure 173: GPS satellite timing signal

The IRIG-B time code signal is a sequence of one second time frames. Each frame is split up into ten 100 mS slots as follows:

- Time-slot 1: Seconds
- Time-slot 2: Minutes

- Time-slot 3: Hours
- Time-slot 4: Days
- Time-slot 5 and 6: Control functions
- Time-slots 7 to 10: Straight binary time of day

The first four time-slots define the time in BCD (Binary Coded Decimal). Time-slots 5 and 6 are used for control functions, which control deletion commands and allow different data groupings within the synchronisation strings. Time-slots 7-10 define the time in SBS (Straight Binary Second of day).

16.10.1.1 IRIG-B IMPLEMENTATION

Depending on the chosen hardware options, the product can be equipped with an IRIG-B input for time synchronisation purposes. The IRIG-B interface is implemented either on a dedicated board, or together with other communication functionality such as Ethernet. The IRIG-B connection is presented by a connector is a BNC connector. IRIG-B signals are usually presented as an RF-modulated signal. The boards support universal IRIG-B, which means they accept demodulated or modulated IRIG-B.

To set the device to use IRIG-B, use the setting ***IRIG-B Sync*** cell in the *DATE AND TIME* column.

The IRIG-B status can be viewed in the ***IRIG-B Status*** cell in the *DATE AND TIME* column.

16.10.2 SNTP

SNTP is used to synchronise the clocks of computer systems over packet-switched, variable-latency data networks, such as IP. SNTP can be used as the time synchronisation method for models using IEC 61850 over Ethernet. A time synchronisation accuracy of within 5 ms is possible.

The device is synchronised by the main SNTP server. This is achieved by entering the IP address of the SNTP server into the IED using the IEC 61850 Configurator software described in the settings application software manual. A second server is also configured with a different IP address for backup purposes.

This function issues an alarm when there is a loss of time synchronisation on the SNTP server. This could be because there is no response or no valid clock signal.

The HMI menu does not contain any configurable settings relating to SNTP, as the only way to configure it is using the IEC 61850 Configurator. However it is possible to view some parameters in the *COMMUNICATIONS* column under the sub-heading SNTP parameters. Here you can view the SNTP server addresses and the SNTP poll rate in the cells ***SNTP Server 1***, ***SNTP Server 2*** and ***SNTP Poll rate*** respectively.

The SNTP time synchronisation status is displayed in the ***SNTP Status*** cell in the *DATE AND TIME* column.

16.10.2.1 LOSS OF SNTP SERVER SIGNAL ALARM

This function issues an alarm when there is a loss of time synchronization on the SNTP server. It is issued when the SNTP sever has not detected a valid time synchronisation response within its 5 second window. This is because there is no response or no valid clock. The alarm is mapped to IEC 61850.

16.10.3 IEEE 1588 PRECISION TIME PROTOCOL

The MiCOM P40 modular products support IEEE 1588 Precision Time Protocol (PTP) as a slave-only clock. MiCOM relays are profile unaware, which means that they will accept synchronisation from any PTP profile. Power Utility Profile (IEC 61850-9-3) is specifically designed to perform well for substation related applications, with PMU applications needing the most stringent requirements.

PTP can be used to replace or supplement IRIG-B and SNTP time synchronisation so that the IED can be synchronised using Ethernet messages from the substation LAN without any additional physical connections being required.

A dedicated DDB signal (***PTP Failure***) is provided to indicate failure of PTP.

16.10.3.1 ACCURACY AND DELAY CALCULATION

A time synchronisation accuracy of within 3 ms is possible. Both peer-to-peer or end-to-end mode delay measurement can be used.In peer-to-peer mode, delays are measured between each link in the network and are compensated for. This provides greater accuracy, but requires that every device between the Grand Master and Slaves supports the peer-to-peer delay measurement.

In end-to-end mode, delays are only measured between each Grand Master and Slave. The advantage of this mode is that the requirements for the switches on the network are lower; they do not need to independently calculate delays. The main disadvantage is that more inaccuracy is introduced, because the method assumes that forward and reverse delays are always the same, which may not always be correct.

When using end-to-end mode, the IED can be connected in a ring or line topology using RSTP or Self Healing Protocol without any additional Transparent Clocks. But because the IED is a slave-only device, additional inaccuracy is introduced. The additional error will be less than 1ms for a network of eight devices.

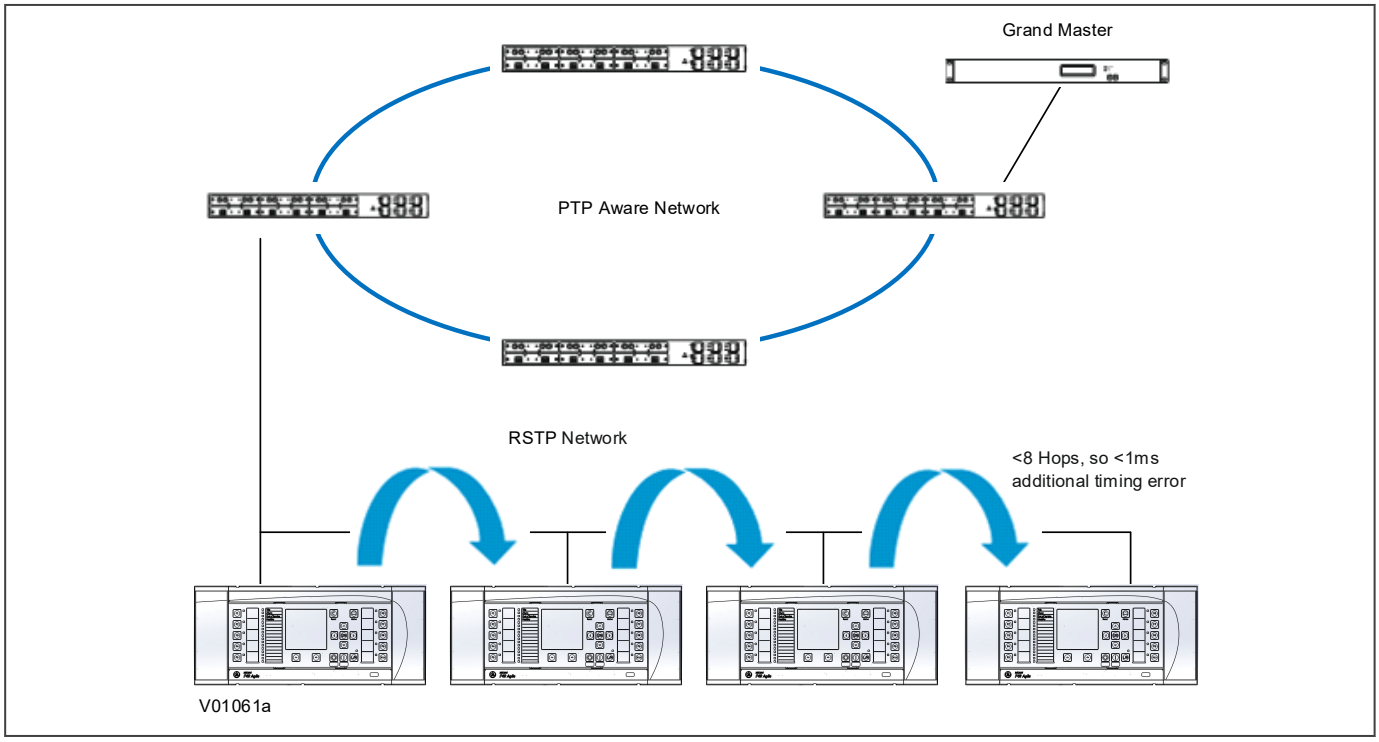

Figure 174: Timing error using ring or line topology

16.10.3.2 PTP DOMAINS

PTP traffic can be segregated into different domains using Boundary Clocks. These allow different PTP clocks to share the same network while maintaining independent synchronisation within each grouped set.

The PTP domain number can be configured in MiCOM P40 modular products the using the ***Domain Number*** cell in the *DATE AND TIME* column. The domain number needs to be configured to match the domain of the local network.

16.10.4 TIME SYNCHRONISATION USING THE COMMUNICATION PROTOCOLS

All communication protocols have in-built time synchronisation mechanisms. If an external time synchronisation mechanism such as IRIG-B, SNTP, or IEEE 1588 PTP is not used to synchronise the devices, the time synchronisation mechanism within the relevant serial protocol is used. The real time is usually defined in the master station and communicated to the relevant IEDs via one of the rear serial ports using the chosen protocol. It is also possible to define the time locally using settings in the *DATE AND TIME* column.

The time synchronisation for each protocol is described in the relevant protocol description section.

CHAPTER 17

CYBER-SECURITY

17.1 DISCLAIMER

GE Vernova Grid Automation products are digital devices designed to be installed and operated in utility substations & industrial plant environments and connected to secure private networks. GE Vernova IEDs should not be connected to the public internet.

GE Vernova strongly recommends that users protect their digital devices using a defense-in-depth strategy which will protect their products, their network, their systems and interfaces against cyber security threats. This includes, but is not limited to, placing digital devices inside the control system network security perimeter, deploying and maintaining access controls, monitoring and intrusion detection, security awareness training, security policies, network segmentation and firewalls installation, strong and active password management, data encryption, antivirus and other mitigating applicable technologies.

GE Vernova IEDs are available with standard features, and in some products additional optional software options, which provide cyber security mechanisms to help users protect against cyber security intrusion. GE Vernova strongly recommends using all available cyber security options.

For additional details and recommendations on how to protect the GE Vernova IEDs, please see Cyber Security sections of the manuals. GE Vernova Grid Automation may also provide additional instructions and recommendations to users from time to time relating to IED and cyber security threats or vulnerabilities.

It is the users' sole responsibility to make sure that all GE Vernova Grid Automation IEDs are installed and operated considering its cyber security capabilities, security context, and the instructions and recommendations provided to the user relating to GE Vernova. Users assume all risks and liability associated with damages or losses incurred in connection with any and all cyber security incidences.

IT IS THE SOLE RESPONSIBILITY OF THE USER TO SECURE THEIR NETWORK AND ASSOCIATED DEVICES AGAINST CYBER SECURITY INTRUSIONS OR ATTACKS. GE VERNOVA GRID AUTOMATION AND ITS AFFILIATES ARE NOT LIABLE FOR ANY DAMAGES AND/OR LOSSES ARISING FROM OR RELATED TO SUCH SECURITY INTRUSION OR ATTACKS.

17.2 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were often proprietary.

For these reasons, the substation environment was very secure against cyber-attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it cannot be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult to interpret them).

However, note that these are not recognised defences against attackers.

The increasing sophistication of protection schemes, coupled with the advancement of technology and the desire for vendor interoperability, has resulted in standardisation of networks and data interchange within substations. Today, devices within substations use standardised protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardised protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for our range of Intelligent Electronic Devices (IEDs).

Note:
Cyber-security compatible devices do not enforce NERC compliance, they merely facilitate it. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary.

This chapter contains the following sections:

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Standards 391
Cyber-Security Implementation 395
Roles and Permissions 396
User Authentication 399
SNMP Configuration 416
Returning The IED To Factory 417
Security Event Management 418

17.3 THE NEED FOR CYBER-SECURITY

Cyber-security provides protection against unauthorised disclosure, transfer, modification, or destruction of information or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorised access to information)
- Integrity (preventing unauthorised modification)
- Availability/Authentication (preventing the denial of service and assuring authorised access to information)
- Non-repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyse incidents)

The threats to cyber-security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber-attacks by hackers).

Good cyber-security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (users keep passwords on their computer)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Bypassing of controls (users turn off security measures)
- Inadequate technology (substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate preventing access to equipment

To help tackle these issues, standards organisations have produced various standards. Compliance with these standards significantly reduces the threats associated with lack of cyber-security.

17.4 STANDARDS

There are several standards, which apply to substation cyber-security. The standards currently applicable to Grid Automation Systems and IEDs are NERC and IEEE1686.

Standard	Country	Description
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber-security capabilities
IEC 62351	International	Power systems management and associated information exchange - Data and communications security
IEC 62443	International	Security for industrial automation and control systems
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber-security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

17.4.1 NERC COMPLIANCE

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of 'Critical Cyber Assets', which control or have an influence on the reliability of North America’s electricity generation and distribution systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

NERC CIP standards

CIP Standard	Description
CIP-002 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005 Electronic Security	Define and document logical security perimeters where Critical Cyber Assets reside. Define and document measures to control access points and monitor electronic access
CIP-006 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside

CIP Standard	Description
CIP-007 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets
CIP-008 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber-security Incidents relating to Critical Cyber Assets are identified
CIP-009 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

17.4.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up

Power Utility Responsibilities	GE Vernova's Contribution
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

17.4.1.2 CIP 003

CIP 003 requires the implementation of a cyber-security policy, with associated documentation, which demonstrates the management's commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained.

Power Utility Responsibilities	GE Vernova's Contribution
To create a cyber-security policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

17.4.1.3 CIP 004

CIP 004 requires that personnel with authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power Utility Responsibilities	GE Vernova's Contribution
To provide appropriate training of its personnel	We can provide cyber-security training

17.4.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required
- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power Utility Responsibilities	GE Vernova's Contribution
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IED

17.4.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power Utility Responsibilities	GE Vernova's Contribution
Provide physical security controls and perimeter monitoring Ensure that people who have access to critical cyber assets don’t have criminal records	GE Vernova cannot provide additional help with this aspect

17.4.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring

Power Utility Responsibilities	GE Vernova's Contribution
To provide an incident response team and have appropriate processes in place	Test procedures, we can provide advice and help on testing. Ports and services, our devices can disable unused ports and services Security patch management, we can provide assistance Antivirus, we can provide advise and assistance Account management, we can provide advice and assistance Monitoring, our equipment monitors and logs access

17.4.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power Utility Responsibilities	GE Vernova's Contribution
To provide an incident response team and have appropriate processes in place.	GE Vernova cannot provide additional help with this aspect.

17.4.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power Utility Responsibilities	GE Vernova's Contribution
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

17.4.2 IEEE 1686-2013

IEEE 1686-2013 is an IEEE Standard for substation IEDs' cyber-security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.
- The audit trail is recorded, listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

17.5 CYBER-SECURITY IMPLEMENTATION

GE Vernova IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

MiCOM 5th Generation P40 products provide enhanced security through the following features:

- An Authentication, Authorization, Accounting (AAA) Remote Authentication Dial-In User Service (RADIUS) client that is managed centrally, enables user attribution, provides accounting of all user activities, and uses secure standards based on strong cryptography for authentication and credential protection. In other words, this option uses a RADIUS.
- Server for user authentication. There is provision for both remote (RADIUS) and local (device) authentication.
- A Role-Based Access Control (RBAC) system in line with IEC 62351-8:2020 that provides a permission model that allows access to the device operations and configurations based on specific roles and individual user accounts configured on the AAA server.
- Security event reporting through both proprietary security event log (separate from the main events file) and the Syslog and SNMP protocols for supporting Security Information Event Management (SIEM) systems for centralised cybersecurity monitoring.
- Encryption of passwords - stored within the IED, in network messages between the MiCOM S1 Agile software and the IED, and in network messages between the RADIUS server and the IED (subject to the RADIUS server configuration).
- Secure firmware upgrade process.

17.5.1 INITIAL SETUP: DEFAULT USERNAMES AND DEFAULT PASSWORDS

The requirements for initial setup of the IED for cyber-security and RBAC will depend on:

1. which interfaces, if any, the cyber-security is required,
2. the intended authentication method, as defined in the setting ***Auth. Method*** in *SECURITY CONFIG* column (see the Authentication Methods section).

When the authentication method is configured as `Device Only`, there are four pre-defined profiles.

User Name	Default Password	IEC 62351-8 Roles
ADMIN1	ChangeMe1#	SECADM
RBACMNT1	ChangeMe2#	RBACMNT
ENGG1	ChangeMe3#	ENGINEER
VIEWER1	ChangeMe4#	VIEWER

During the first logon, it is Mandatory to change the Default Passwords, and the IED or MiCOM S1 Agile software will prompt the user to change it. The new password must comply with the strength defined by the Password Policy setting, detailed in the ***Password Policy*** section of this chapter.

When the authentication method is configured as ‘Server + Device’, and authentication using RADIUS is required, users must be set up on the RADIUS server (see the RADIUS users section). These users are separate from the pre-defined Device users. RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication (see the RADIUS server settings section). It is recommended that the RADIUS shared secret be changed from the default (see the RADIUS client-server validation section).

17.6 ROLES AND PERMISSIONS

17.6.1 ROLES

The P40 Agile products supports all the mandatory pre-defined roles as per IEC 62351-8:2020.

IEC 62351-8 Roles	Value
VIEWER	0
OPERATOR	1
ENGINEER	2
INSTALLER	3
SECADM	4
SECAUD	5
RBACMNT	6

Individual user accounts can be configured to have one or more of these roles.

- VIEWER: Can view all values and settings
- OPERATOR: Can view values and perform control operations
- ENGINEER: Can view values, and change settings of the device
- INSTALLER: Specific role required to perform firmware updates
- SECADM: Security Administrator - Can edit/modify Users and roles and configure security settings
- SECAUD: Security Auditor - Can view Security Log files
- RBACMNT: RBAC Management can change role to permission assignment

Only one role of one type is allowed to be logged in at a time from any interface. For example, one Operator can be logged in but not a second Operator at the same time from any other interface. This prevents subsets of settings from being changed at the same time.

17.6.2 PERMISSIONS

Authentication and authorization are two different processes. An authenticated user cannot perform any action on the IED unless a privilege has been explicitly granted to them. This is the concept of “least privileges” access.

Privileges must be granted to users through roles. A role is a collection of privileges, and roles are granted to users. It is possible to have multiple roles for a user. The privilege/role matrix is stored on the IED. This is known as Role-Based-Access Control (RBAC).

On successful user authentication, the IED will load the user’s role list. If the user’s role changes, the user must logout and log back in to exercise his/her privileges.

The table below shows the predefined permissions assignment for the predefined Roles according to IEC 62351-8:2020

Value	Role Name (revision = 1)	Permission										
		LISTOBJECTS	READVALUES	DATASET	REPORTING	FILEREAD	FILEWRITE	FILEMNGT	CONTROL	CONFIG	SETTINGGROUP	SECURITY
<0>	VIEWER	C	C		X	C_1						

Value	Role Name (revision = 1)	Permission										
		LISTOBJECTS	READVALUES	DATASET	REPORTING	FILEREAD	FILEWRITE	FILEMNGT	CONTROL	CONFIG	SETTINGGROUP	SECURITY
<1>	OPERATOR	X	X		X	C_1			X		X	
<2>	ENGINEER	X	X	X	X	X_1	X_1	X_1		X	X	
<3>	INSTALLER	X	X		X	X_2	X_2			X	X	
<4>	SECADM	X	X	X		X_4	X_4	X_4		X		X
<5>	SECAUD	X	X		X	X_3						
<6>	RBACMNT	X	X		X			X_4		X		
<7 ...32767>	Reserved	For future use of IEC defined roles.										
<-32768 .. -1>	Private	Defined by external agreement. Not guaranteed to be inoperable.										

C = Conditional read access, clarification of specific data objects may be necessary (e.g., VIEWER may not access security settings, but process values)
C_1 = Conditional read access to files of filetype data
X_1 = Access to files of type data and config
X_2 = Access to files of type config and firmware (updates)
X_3 = Access to files of type audit log
X_4 = Access to files of type security (config)

The table below shows the predefined permissions description according to IEC 62351-8:2020

Permission	Description
LISTOBJECTS	Allows the subject/role to discover what objects are present within an IED by presenting the type and ID of those objects. If this permission is granted to a subject/role, the object for which the READVALUES permission has not been granted are not readable. This permission basically relates to all objects defined in IEC 61850 and allows a query on the existence of the data objects.
READVALUES	Allows the subject/role to obtain the values for all or some objects that are present within an IED in addition to the type and ID. This permission basically relates to all objects defined in IEC 61850 that provide a value and allows a read action on the actual values of the data objects.
DATASET	Allows the subject/role to have full service access (e.g., createDataSet, deleteDataSet) for both persistent and non-persistent DataSets.
REPORTING	Allows the subject/role to use buffered reporting as well as unbuffered reporting. Reporting relates to buffered and unbuffered report control blocks of a logical node.
FILEREAD	Allows the subject/role to perform read actions on file objects.
FILEWRITE	Allows the subject/role to perform write actions on file objects. This permission includes the FILEREAD permission.
CONTROL (group)	Allows the subject/role to perform control operations on all or some controllable objects that are present within an IED. Control services are for instance select or operate and relate to data objects defined in IEC 61850.
CONFIG	Allows the subject/role to locally or remotely configure all or some objects that are present within an IED. This relates to data attributes of the IEC 61850 functional constraints CF, DC and SP.
SETTINGGROUP	Allows the subject/role to remotely configure SettingGroup control block. For example, this relates to the switching between different configured SettingGroups. SettingGroups also contains the IEC 61850 functional constraints SE.
FILEMNGT	Allows the subject/role to delete existing files on the IEDS.
SECURITY	Allows the subject/role to perform actions on all security related data objects, reportings, logs or files.

Specific product related permissions are listed in the tables below. Roles are mapped to Access Level definitions: A cross indicates that specific actions can be done by a user with the role allocated.

Extract Files	Role Name							
File Type	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Setting				X	X	X	X	X
PSL				X	X			
MCL (IEC 61850)				X	X			
DNP3				X	X			
SLD				X	X			
Events (operational)		X	X	X				
Security Events							X	
Disturbance Records		X	X	X				

Sending Files	Role Name							
File Type	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Setting				X	X	X		
PSL				X	X			
MCL (IEC 61850)				X	X			
DNP3				X	X			
SLD				X	X			
Menu Text				X	X			

17.7 USER AUTHENTICATION

17.7.1 AUTHENTICATION METHODS

The IED supports Bypass (no authentication), Device authentication and Server authentication.

Authentication Method	Description	User Interface
Bypass Auth.	IED does not provide security, any user (Local) can access the IED without logging in. IED does not validate user and password. In this case, there is no need to enter user name and password to login. Bypass can not be enabled on Rear Port 1, Rear Port 2 and Ethernet Ports.	Front Panel UI Front Port (USB port) (Local interfaces only)
Device Only	IED allows role access using local authentication.	Front Panel UI Front Port (USB port) Rear Port 1 Rear Port 2 Network Port 1 Network Port 2
Server + Device	IED uses RADIUS server authentication to validate the user first. And it allows fallback to device authentication if the RADIUS server(s) are unavailable.	Front Panel UI Front Port (USB port) Rear Port 1 Rear Port 2 Network Port 1 Network Port 2

If ***Bypass Auth.*** is enabled, the IED ignores the ***Auth. Method*** setting.

The ***Auth. Method*** setting offers the following options for user authentication:

- *Server + Device* (This is the default setting for IEDs with NIC (Ethernet Board) fitted)
- *Device Only* (This is the default setting for IEDs without NIC (Ethernet Board) fitted)

Only users with a SECADM role may change the ***Auth. Method*** setting. If the SECADM user changes it, the role remains logged in. Only when the user logs-out is their access-level revoked.

17.7.2 BYPASS

In ***Bypass Auth.*** mode, the IED does not provide user authentication - any user can login. IED does not validate user and password. The bypass security feature provides an easier access, with no authentication and encryption for situations when this is considered safe. Only users with SECADM role can enable Bypass mode.

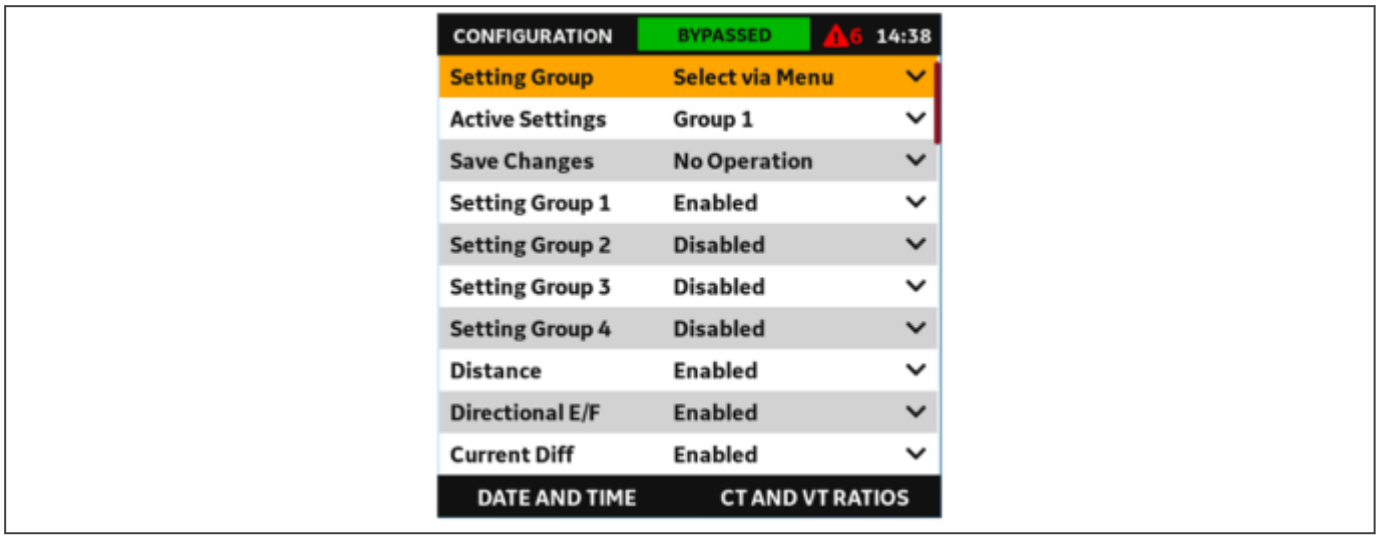
There are three modes for authentication bypass:

1. *Disabled* - no interfaces in ***Bypass Auth.*** mode (normal authentication is active)
2. *Local* - Bypass authentication when using Front Port and Front Panel
3. *Front Panel* - will bypass authentication Front Panel User Interface

Bypass authentication for Bypass mode:	Front Port	Front Panel UI
Disabled		
Local	X	X
Front Panel		X

The DDB signal ***Security Bypass*** is available to indicate that the IED is in ***Bypass Auth.*** mode.

The Front Panel UI will display "BYPASSED" at the top of the screen to indicate that the IED is in ***Bypass Auth***. mode.



17.7.3 LOGIN

A user can only login through the following methods:

- Front Panel User Interface
- Using MiCOM S1 Agile, connected to either the Front Port, Rear Port 1 or 2, or Ethernet Network Port 1 or 2.

17.7.3.1 FRONT PANEL LOGIN

Front panel User Interface supports both Device authentication and Server authentication. The P40 gives the user the option to enter the user credentials via UI panel. To access the Login window, select the Login text in the top banner using the arrow keys.

R80008

For both Device authentication or Server authentication, the user can enter any valid username and password combination. For ease of typing, it is preferable to do login using MiCOM S1 Agile.

After successful log in, a confirmation message is displayed, showing the logged in username at the top of the screen. For example:

R80010

17.7.3.2 LOGIN FAILED

When Authentication fails, a failure message is displayed:

17.7.3.3 OTHER LOGIN PROMPTS

For cases where the bypass is disabled and the user attempts an action which requires a user login, the Login Window appears after the error message. This is applicable while changing any setting values or pressing buttons which require user management - the Function Key, for example.

17.7.3.4 MICOM S1 LOGIN

When the user attempts to login, MiCOM S1 Agile will prompt the user with a login dialog box that contains a username and password entry fields. For both Device authentication or Server authentication, the user can enter any valid combination of username and password.

17.7.3.4.1 WARNING BANNER

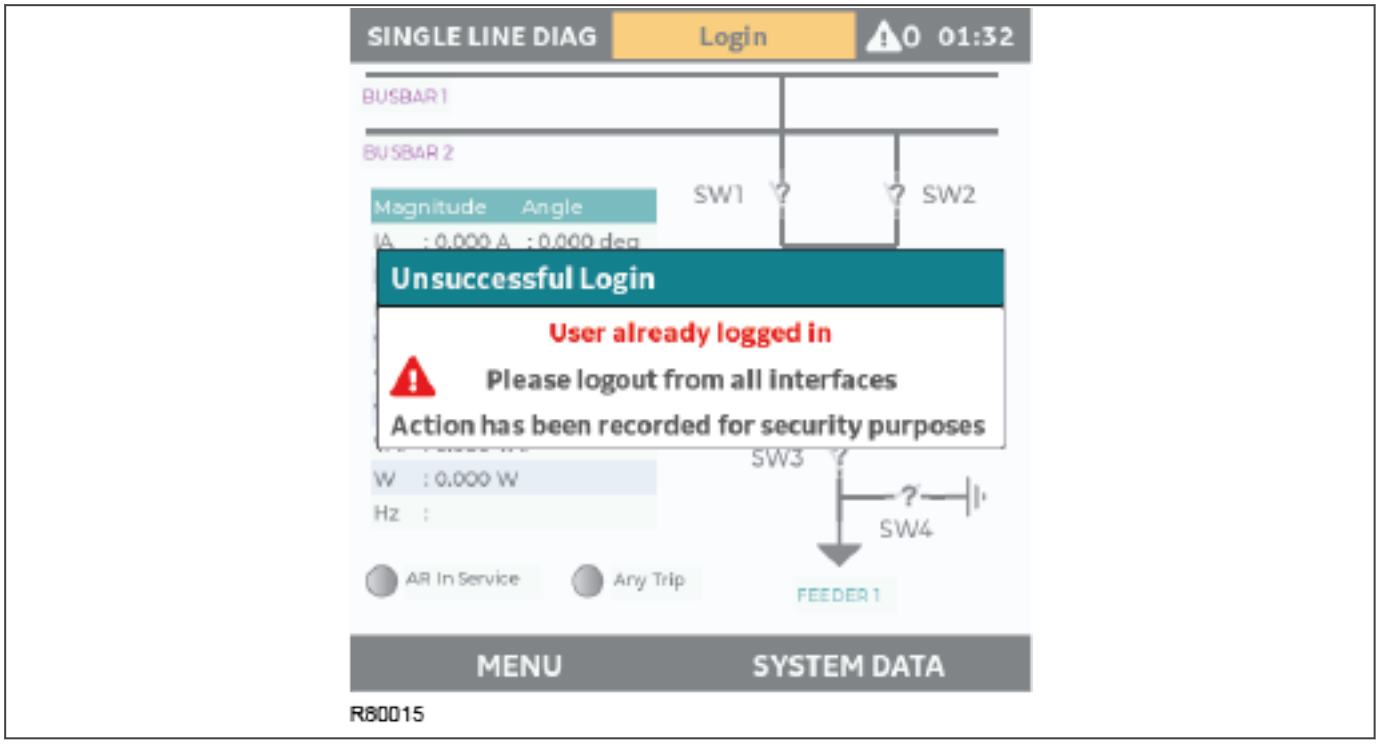
After successful authentication and authorisation to access the IED, MiCOM S1 Agile will display a security warning banner to the user.

If **I Agree** is selected, the integrated authentication and authorisation is completed. Selecting **I Disagree** causes the program to close and the login user to logout.

For S1 Agile authentication, this is a pop-up dialog that the user must click to acknowledge.

17.7.4 USER SESSIONS

Only one role of one type is allowed to be logged in at a time from any interface. If the role has been logged in from one interface, an attempt to login the same role will result in a message being displayed, as below.



Open sessions will be automatically closed by the IED after a configurable session timeout.

The inactivity timer configuration setting defines the period of time that the IED waits in idleness before a logged in user is automatically logged out.

If there is any data change that does not commit to IED, the data change is discarded when user logged out. If there is any access that does not finish, the access will fail when user logged out. Front panel will display the default page when user reaches the defined inactivity time.

If the keypad is inactive for configured UI inactivity timer, the user logout message is displayed and the front panel user interface reverts to the Viewer access level.

The following settings are available in the ***SECURITY CONFIG*** column to support configurable inactivity timers.

- ***FP InactivTimer***
- ***UI InactivTimer***
- ***NIC Tunl Timeout***

Setting Name	Description	Min	Max	Default	Units	User Role Required
Attempts Limit	Number of failed authentications before the device blocks subsequent authentication attempts for the lockout period. A value of 0 means Lockout is disabled.	0 (lockout disabled)	99	3	-	SECADM
Lockout Period	The period of time in seconds a user is prevented from logging in, after being locked out.	1	5940	30	sec	SECADM
FP InactivTimer	FP Inactivity Timer is the time of idleness on Front Port before a logged in user is automatically logged out and revert the access level to the viewer role	0 (no Inactivity Timeout)	30	10	min	SECADM
UI InactivTimer	UI Inactivity Timer is the time of idleness on Front Panel before a logged in user is automatically logged out and revert the access level to the viewer role	0 (no Inactivity Timeout)	30	10	min	SECADM

Setting Name	Description	Min	Max	Default	Units	User Role Required
NIC Tunl Timeout	NIC Tunl Timeout is the time of idleness on Ethernet Port (NIC) before a logged in user is automatically logged out and revert the access level to the viewer role	1	30	5	min	SECADM

The recommended settings for ***Attempts Limit*** is *3* and ***Lockout Period*** is *30 sec* to discourage brute force attacks. If the Lockout period is too large, anybody can lockout Device users.

The following settings are available in the *COMMUNICATIONS* column to configure the inactivity timers for rear serial ports:

- ***KBUS InactTmr*** for RP1, if Courier Protocol is selected
- ***RP2 InactivTimer*** for RP2

17.7.5 USER LOCKING POLICY

A local user locking policy is implemented for Device access:

- This user locking policy applies to both Device users.
- The account is unlocked at the first successful login after the ***Lockout Period***
- If the user consecutively fails to login at the configured number of ***Attempts Limit***, the user account will be locked for the configured ***Lockout Period***

Each user account records how long it has been locked if the account is locked.

Each user account records how many times it has consecutively failed to login. User account failed times include all interfaces login attempts. For example, if the ***Attempts Limit*** setting is *3* and the operator failed to login from front panel 2 times, and they changed to login from the Courier interface, but failed again, then the Operator would be locked out.

When the IED is powered on, these ***Attempts Limit*** counter resets to zero.

When the user account exceeds the ***Attempts Limit*** it is locked for ***Lockout period***, at that time ***Attempt limit*** resets to zero.

The locked user account will be unlocked automatically, after the configured “Lockout Period” is expired.

If the locked account attempts to login the IED from the Front Panel, the unsuccessful login attempt screen is displayed.

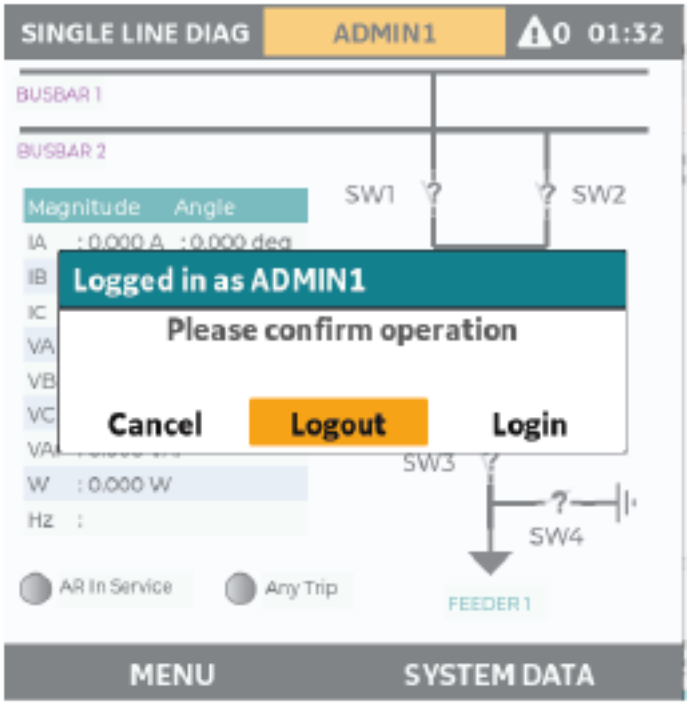
17.7.6 LOGOUT

Each user should ***Log out*** after reading or configuring the IED.

The user can only log out from the front panel, if they logged in from the front panel. If the user logged in from S1 Agile, they have to logout from S1 Agile.

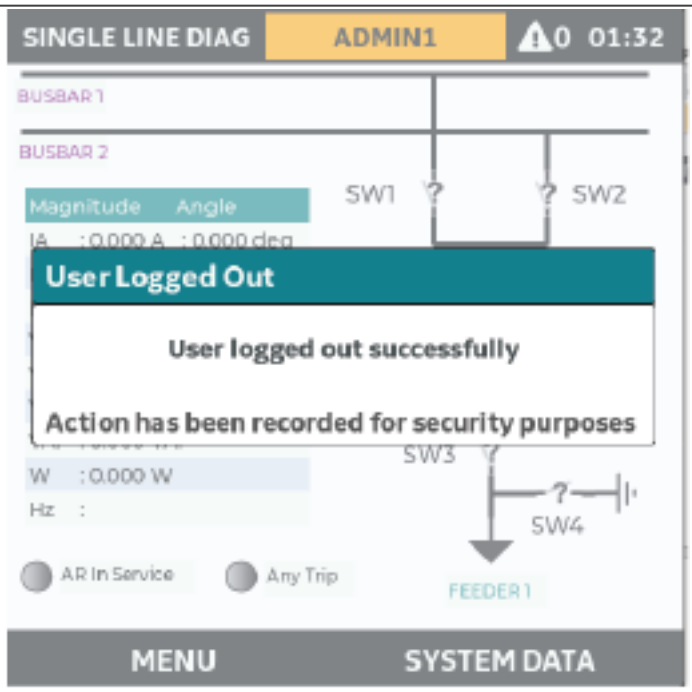
17.7.6.1 FRONT PANEL LOGOUT

Go to the top of the banner and select the current logged in User. You may be prompted to log out with the following display:



R80013

If you confirm, the following screen is displayed for 2 seconds and then the action will be recorded in the security events file:



R80014

If you decide not to log out (i.e. you cancel), the logout screen would be cancelled.

17.7.6.2 MICOM S1 LOGOUT

Right-click on the device name in the System Explorer panel in MiCOM S1 Agile and select Log Off.

In the Log Off confirmation dialog, click Yes. The action will be recorded in the security events file.

17.7.7 PASSWORD POLICY

Cyber-security requires strong passwords and validation for NERC compliance. The IED will enforce one of two levels of password strength according to the ***Password Policy*** setting.

The NERC password complexity policy requires an alpha-numeric password (for all accesses, front panel, and network/local port) that meets the following **mandatory** requirements:

1. Passwords cannot contain the user's account name or parts of the user's full name that exceed two consecutive characters.
2. Passwords must be at least eight characters in length, but not exceed 16 characters in length.

Strict passwords rules must contain characters from all four categories as shown below:

a. English uppercase characters (A through Z).
b. English lowercase characters (a through z).
c. Numeric (digits 0 through 9).
d. Special non-alphanumeric characters (such as @,!,#,{, but not limited to only those)

Normal password rules: Any 3 out of 4 conditions as in strict password rules.

For Device authentication, the IED will enforce that configured passwords meet these requirements. The user can select which policies are required by selecting either Strict or Normal in the Password Policy setting under DEVICE RBAC.

Setting Name	Description	Min	Max	Default	Units	User Role Required
Password Policy	Selection of whether strict or normal rules apply for device authentication password policy	Normal	Strict	Strict	-	SECADM

For Server authentication, the password complexity and user locking policy is defined in the external RADIUS server.

17.7.8 PASSWORD EXPIRY

For Device authentication users, it is possible to select a configurable time (in days) for the password to be changed by the user.

Under *DEVICE RBAC* Settings, select ***Password Expiry*** to be Enabled. The setting of ***Disabled*** disables the password expiry check by the IED. If enabled, Max Password Age can be selected, this is in the range of days.

Setting Name	Description	Min	Max	Default	Units	User Role Required
Password Expiry	Selection of whether Password Expiry is enforced by the IED for device authentication	Disabled	Enabled	Enabled	-	SECADM
Max Password Age	Period in days if Password Expiry is enabled, the device passwords need to be changed	30	730	180	days	SECADM

When the Max Password Age has been reached and if the user attempts to login using the front panel UI, the following window will be shown.

R80011

The user will be presented with a screen to save the new password.

R80012

17.7.9 CHANGE PASSWORD

All the Device users will need to change the default password at the first logon.

The initial password change can be done either from the front panel User Interface, or from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

Any further password change can only be done from MiCOM S1 Agile using the **Change/Set Password** option in the **Supervise Device** dialog box.

Users with SECADM and RBACMNT roles can change the password of any user. Users with other roles can change only their own password.

Caution:
It is recommended that user passwords are changed periodically.

17.7.10 RADIUS AUTHENTICATION

When the ***Auth. Method*** setting is configured as *Server + Device*, a user must log in with a username and password that has been predefined on the RADIUS server.

This log in can be performed from any interface, as described in the Login section. The IED will authenticate the user to the active RADIUS server, over the Ethernet connection.

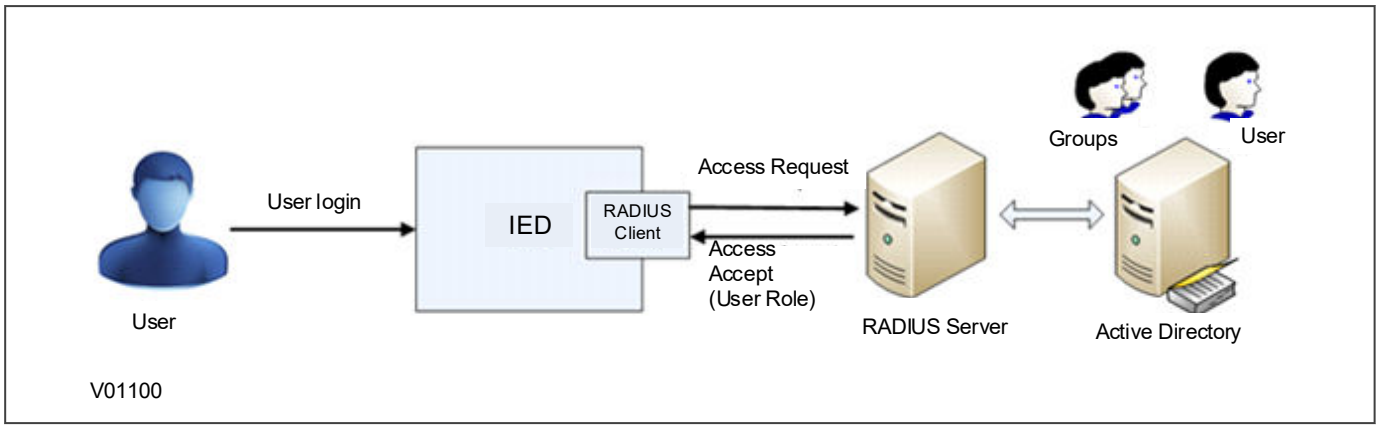


Figure 175: RADIUS server/client communication

17.7.10.1 RADIUS USERS

For Server authentication, RADIUS users and passwords are created in the RADIUS server (in the Active Directory), not in the IED.

The username must be from the ASCII Subset of 32 to 122 which includes upper and lower case letters, digits and several special characters.

Each RADIUS user must have a password that meets the password policy of the Active Directory (not the password policy of the P40) and have one of the supported roles assigned in the Active Directory.

The number of RADIUS users is not limited by the IED.

RADIUS password changes are done in the Active Directory (after password expiration).

17.7.10.2 RADIUS CLIENT

Two RADIUS servers are supported by the IED in the configuration for redundancy. The IED will try each in sequence until one responds.

The IED will first try server 1 up to the configured number of retries, leaving a request timeout between each request. If, after this point there is still no valid answer from server 1, the IED will switch to server 2 and repeat for up to the configured number of retries.

If the number of retries for the second server is exceeded the IED will fallback to Device authentication. A **RADIUS Server unavailable** security event is also logged under this condition.

The RADIUS implementation supports the following authentication protocols:

- EAP-TTLS-MSCHAP2
- PAP
- EAP-PEAP-MSCHAP2
- PAP EAP-TTLS-PAP (Default)

The RADIUS implementation queries the Role ID vendor attribute and establish the logged in user security context with that role.

RADIUS Config.	Value
Vendor ID	2910
Vendor Attribute	1
Standard Values	
VIEWER	0
OPERATOR	1
ENGINEER	2
INSTALLER	3
SECADM	4
SECAUD	5
RBACMNT	6

17.7.10.3 RADIUS SERVER SETTINGS

The following RADIUS server information must be configured in the IED to connect to the RADIUS server(s) for Server authentication.

Setting Name	Description	Min	Max	Default	Units	User Role Required
RADIUS Pri IP	IP address of Server 1. Default value indicates no Primary RADIUS server is configured, and so RADIUS is disabled.	0.0.0.0	255.255.255.255	0.0.0.0	-	SECADM
RADIUS Sec IP	IP address of Server 2. Default value indicates no Secondary RADIUS server is configured	0.0.0.0	255.255.255.255	0.0.0.0	-	SECADM
RADIUS Auth Port	RADIUS authentication port	1	65535	1812	-	SECADM
RADIUS Security	Authentication protocol to be used by RADIUS server	EAP-TTLS-MSCHAP2 PAP EAP-PEAP-MSCHAP2 PAP EAP-TTLS-PAP		PAP EAP-TTLS-PAP	-	SECADM
RADIUS Timeout	Timeout in seconds between re-transmission requests	1	900	2	sec	SECADM
RADIUS Retries	Number of retries before giving up	1	99	10	-	SECADM
RADIUS Secret	Shared Secret used in authentication. It is only displayed as asterisks.	1 character	64 characters	ChangeMe1#	-	SECADM

Setting Name	Description	Min	Max	Default	Units	User Role Required
RADIUS NAS ID	NAS-Identifier for RADIUS	1 character	20 characters	MiCOM P40	-	SECADM

The data cell ***RADIUS Status*** indicates the status of the currently-selected RADIUS server. This will display either `Disabled`, `Server OK`, or `Failed`.

17.7.10.4 RADIUS ACCOUNTING

RADIUS accounting is not supported by the IED. The user can achieve accounting through syslog (see the SYSLOG section).

17.7.10.5 RADIUS CLIENT-SERVER VALIDATION

Client-server validation is achieved using a shared secret. The IED must be configured with the ***RADIUS Secret*** setting to match the shared secret configured in the RADIUS server. It is recommended (but not enforced) that this setting meets the P40 password requirements. The device supports RADIUS secret of 1-64 characters.

MiCOM S1 Agile provides an option to save ***RADIUS Secret*** to the device. This can be achieved by logging to the device with a SECADM profile and accessing Supervise Device -> ***RADIUS Secret***.

Note:
It is recommended that the shared secret be changed from the default before using RADIUS authentication.

The IED does not support exchange of CA certificates. The RADIUS server may send a certificate but the IED will not verify it.

17.7.11 RECOVERY

17.7.11.1 RESTORE TO LOCAL FACTORY DEFAULT

The ***Restore Defaults*** setting is available to facilitate NERC CIP compliance requirements for decommissioning critical cyber devices. Only the **Administrator** role can change this setting.

The ***Restore Defaults*** setting under the *CONFIGURATION* column is used to restore a setting group to factory default settings.

0 = `No Operation`

1 = `All Settings`

2 = `Setting Group 1`

3 = `Setting Group 2`

4 = `Setting Group 3`

5 = `Setting Group 4`

To restore the default values to the settings in any setting group, set the ***Restore Defaults*** setting to the relevant Group number. Alternatively, it is possible to set the ***Restore Defaults*** setting to `All Settings` to restore the default values to all the IEDs settings, not only one setting group.

Note:
Restoring defaults to all settings includes the rear communication port settings, which may result in communication via the rear port being disrupted if the new (default) settings do not match those of the master station.

Data (events, DR, fault records, protection counters etc) is left untouched. When decommissioning critical cyber IEDs, users may want to clear all data and events as well.

17.7.11.2 PASSWORD RESET PROCEDURE

If you mislay a devices password (if Administrator forgets their password), the passwords can be reset to default using a recovery password. To obtain the recovery password you must contact the Contact Centre and supply the Serial Number and the security code. The Contact Centre will use these items to generate a Recovery Password.

The security code is a 16-character string of uppercase characters. It is a read-only parameter. The device generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

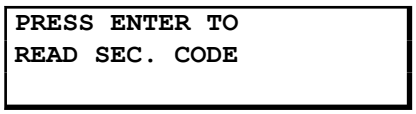
This reset procedure can be only accomplished through front panel exclusively and cannot be done over any other interface. As soon as the security code is displayed on the front panel User Interface, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the Contact Centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the Contact Centre over weekends and bank holidays.

The procedure is:

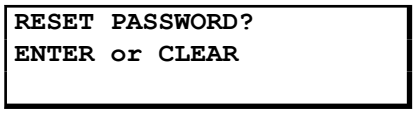
The security code is displayed on confirmation. The validity timer is then started. The security code can only be read from the front panel.

This reset procedure can be only accomplished through front panel exclusively and cannot be done over the Ethernet/serial port, but only when physically present in front of the IED. In the event of losing all passwords (if the Administrator forgets their password) the user could reset the IED to default passwords, following the procedure below:

1. User navigates to ***Security Code*** cell in *SECURITY CONFIG* column
2. To prevent accidental reading of the IED ***Security Code***, the cell will initially display a warning message:



3. Press Enter to read the ***Security Code***.
4. User sends an email to the Contact Centre providing the full IED serial number and displayed ***Security Code***, using a recognisable corporate email account
5. Contact Centre emails the user with the Recovery Password. The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.
6. User logs in with the username **ADMINISTRATOR** and the recovery password in to the ***Password*** setting in *SYSTEM DATA* column.
7. Then IED will prompt



8. Press Enter to continue the reset procedure
9. If the recovery password successfully validates, the default passwords are restored for each access level for Device authentication.
10. Change ***Auth. Method*** setting to `Server + Device` if applicable.

Note:
Restoring passwords to defaults does not affect any other settings and does not provoke reboot of the IED. The protection and control functions of the IED are always maintained.

17.7.11.3 ACCESS LEVEL DDBS

The current level of access for each interface is available for use in the Programmable Scheme Logic (PSL) as these DDB signals:

- ***HMI Access Lvl 1***
- ***HMI Access Lvl 2***
- ***FPort AccessLvl1***
- ***FPort AccessLvl2***
- ***RPrt1 AccessLvl1***
- ***RPrt1 AccessLvl2***
- ***RPrt2 AccessLvl1***
- ***RPrt2 AccessLvl2***

Each pair of DDB signals indicates the access level as follows:

- Level 1 off, Level 2 off = 0
- Level 1 on, Level 2 off = 1
- Level 1 off, Level 2 on = 2
- Level 1 on, Level 2 on = 3

KEY:

HMI = Human Machine Interface

(Front Panel User Interface)

FPort = Front Port

RPrt = Rear Port

Lvl = Level

17.7.12 PORT HARDENING: PHYSICAL PORTS

It is possible to disable unused physical ports. Enabling/Disabling of physical ports can be done either via the Front Panel or by sending the modified settings to the IED. These settings are under the PORT HARDENING: PHYSICAL PORTS Section of SECURITY CONFIG column. A user with SECADM role is needed to perform this action. This action cannot be done via the Supervise Device dialog box using MiCOM S1 Agile.

The following ports can be disabled, depending on the model.

- Front Port (***Front Port*** setting)
- Rear Port 1 (***Rear Port 1*** setting)
- Rear Port 2 (***Rear Port 2*** setting)
- Ethernet Network Port 1 (***Network Port 1*** Setting)
- Ethernet Network Port 2 (***Network Port 2*** Setting)

17.7.13 PORT HARDENING: LOGICAL PORTS (PROTOCOLS)

It is possible to disable unused logical ports. Enabling/Disabling of logical ports can be done either via the Front Panel or via sending the modified settings to the IED. These settings are under the PORT HARDENING: LOGICAL PORTS Section of the SECURITY CONFIG column. A user with SECADM role is needed to perform this action, This action cannot be done via the Supervise Device dialog box using MiCOM S1 Agile.

The following NIC protocols can be disabled:

- Courier Tunnel (for S1 Agile remote connection over Ethernet)
- IEC 61850
- SNTP
- PTP
- SNMP
- RADIUS
- SYSLOG

17.7.14 SERVICE (PROTOCOL) MAPPING: ETHERNET NETWORK PORTS 1 AND 2

This section details which of the Ethernet protocols are available on each of Network Port 1 and Network Port 2, and whether these are configurable or fixed mappings. Settings for the configurable service mappings are under the PORT HARDENING: SERVICE MAP section of the *SECURITY CONFIG* column.

Service	Network Port 1	Network Port 2	Fixed/Configurable	Setting
IEC 61850	No	Yes	Fixed to NP2.	
SNTP	No	Yes	Fixed to NP2.	
PTP	No	Yes	Fixed to NP2.	
SSH (for S1 Agile)	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	Courier Tunnel
SNMP	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	SNMP
RADIUS	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	RADIUS
Syslog	Yes - only one port at a time	Yes - only one port at a time	Configurable - NP1 or NP2	SYSLOG

17.7.15 SUPERVISE DEVICE DIALOG BOX

Supervise Device	Role Name							
	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Active Group			X	X	X			
Reset Cell			X					
Breakers			X					
Device Address				X	X	X		
Date and Time			X	X	X			
Bypass Options						X		

Supervise Device	Role Name							
	None Logged	VIEWER	OPERATOR	ENGINEER	INSTALLER	SECADM	SECAUD	RBACMNT
Active MCL Bank				X	X			
Device User Management						X		X
Own Password Change		X	X	X	X	X	X	X
RADIUS Secret						X		
SNMP Security						X		
Clear Records				X				
Restore Defaults				X	X			
Restore Security Settings						X		
SSH Client Passcode						X		

17.7.16 SECURE FIRMWARE UPGRADE

IEC 62351-8:2020 has defined a specific INSTALLER Role which can do firmware upgrades on the IEDs. The default users in the Device Authentication does not have any users with the INSTALLER Role. If a requirement exists to upgrade the Firmware of the IED, then the following mandatory steps must be taken before starting the firmware update:

- Using MiCOM S1 Agile, create a new user having the INSTALLER Role
- Using MiCOM S1 Agile, log into the device using the user having the INSTALLER Role. Change the default password
- Use the Firmware Download Tool and log into the IED, using the newly created user and changed password
- Once these steps are done, the firmware update process can continue.

The device supports Secure Firmware Update. The firmware files are checked for validity prior to updating of the IED. The main steps in the secure firmware update process are as follows:

- The ‘PX40 Download and Calibration’ firmware tool opens the secure firmware ZIP file and extracts its contents [Compressed Images and Signatures].
- The ‘PX40 Download and Calibration’ firmware tool transfers the firmware files [Compressed Images and Signatures] to IED Main CPU Board.
- IED validates the Compressed Images and extracts them.
- After successful validation, only then will the settings be cleared.
- In case of validation failure, IED will display the ERROR CODE and after that, the user can reboot the relay to its previous state.
- IED updates it Main CPU Board, Co-processor Board and Ethernet Board storage and verifies it.
- Finally, the Main CPU Board initiates an IED reboot.

Key steps in this process will be logged in the security events - see the Security Event Management section of this chapter for further details.

Any firmware upgrade should be organised through the GE Vernova Grid Automation After Sales Service departments, or a regional Local Service Centre. The firmware upgrade should normally be performed by GE Vernova personnel, or by suitably prepared and competent persons after instruction from GE Vernova personnel. A separate MiCOM P40 firmware download procedure guide is available.

Note:
It is not possible to update the firmware on the IED which is under Bypass mode.

Note:
During the firmware update, only the security events file is retained - all other configuration and record files are erased during a firmware upgrade.

17.8 SNMP CONFIGURATION

You configure the SNMP interface using the HMI panel or using the SNMP Security option in the Supervise Device dialog box by a user with SECADM role. Two different versions are available; SNMPv2c and SNMPv3:

To enable the SNMP interface:

1. Select the SECURITY CONFIG column and scroll to the SNMP PARAMETERS heading
2. You can select either v2C, V3 or both. Selecting None will disable the main processor SNMP interface.

SNMP Trap Configuration

SNMP traps allow for unsolicited reporting between the IED and up to two SNMP managers with unique IP addresses. The device MIB details what information can be reported using Traps. To configure the SNMP Traps:

1. Move down to the cell ***Trap Dest. IP 1*** and enter the IP address of the first destination SNMP manager. Setting this cell to `0.0.0.0` disables the first Trap interface.
2. Move down to the cell ***Trap Dest. IP 2*** and enter the IP address of the second destination SNMP manager. Setting this cell to `0.0.0.0` disables the Second Trap interface.

SNMP V3 Security Configuration

SNMPv3 provides a higher level of security via authentication and privacy protocols. The IED adopts a secure SNMPv3 implementation with a user-based security model (USM).

Authentication is used to check the identity of users, privacy allows for encryption of SNMP messages. Both are optional, however you must enable authentication in order to enable privacy. To configure these security options:

1. If SNMPv3 has been enabled, set the ***Security Level*** setting. There are three levels; without authentication and without privacy (`noAuthNoPriv`), with authentication but without privacy (`authNoPriv`), and with authentication and with privacy (`authPriv`).
2. If Authentication is enabled, use the ***Auth Protocol*** setting to select the authentication type. There are two options: `HMAC-MD5-96` or `HMAC-SHA-96`.
3. Using the ***Auth Password*** setting, enter the password (up to 20 characters) to be used by the IED for authentication.
4. Using the ***Auth Protocol*** setting, select one of the two available mechanisms for encryption of messages to be used by the IED (CBC-DES or CFB-AES128).
5. If privacy is enabled, use the ***Encrypt Password*** setting to set the encryption password (up to 20 characters) that will be used by the IED for encryption.

> *Note:*
> *When setting the SNMP browser for RBAC compatible relays, the Context Name should be 'px4x'.*

SNMP V2C Security Configuration

SNMPv2c implements authentication between the master and agent using a parameter called the ***Community Name***. This is effectively the password but it is not encrypted during transmission (this makes it inappropriate for some scenarios in which case version 3 should be used instead). To configure the SNMP 2c security:

1. If SNMPv2c has been enabled, use the ***Community Name*** setting to set the password that will be used by the IED and SNMP manager for authentication. This may be between one and 8 characters.

17.9 RETURNING THE IED TO FACTORY

MiCOM P40 5th Generation products provide enhanced security, and there is no mechanism to bypass the implemented user management. In the event that the IED is returned to the factory for repair or technical analysis, to facilitate the Engineers gaining access to the configuration and stored records in the IED, it is proposed that the IED is returned to the factory with one of the following options:

- Bypass enabled on the front port
- A new user with all Roles is created and left with a default password. If the details of this user are passed to the factory, the IED can be logged in after changing the default password. If the newly created user's password has been modified, it will be required that the modified password is provided

17.10 SECURITY EVENT MANAGEMENT

To implement NERC-compliant cyber-security, a range of security events are logged by the IED in three separate methods:

- In the Security Events file (security audit log) - a Courier events file that can be extracted and viewed by MiCOM S1 Agile
- As syslog events
- As SNMP events (traps)

17.10.1 SECURITY EVENTS: COURIER

The P40 supports the IEC 62351-14 format of security event messages. These are logged into a separate security audio log file named "Security events" that can be extracted and viewed by MiCOM S1 Agile, in addition to the operational events file. The maximum number of security events is 2048.

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_PW_SET_NON_COMPLIANT	62443-AUDIT_LOG	Info	USER_PW_CHANGE_FAIL_POLICY	IEC 62351-14:1.31	User Password change failed - policy check failed	
SECUR_EVT_PW_MODIFIED	62443-CONFIG_CHANGE	Notice	USER_PW_CHANGE_OK	IEC 62351-14:1.25	User password changed successfully	Interface
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	62443-ACCESS_CONTROL	Notice	LOCK_USER_WRONG_CR	IEC 62351-14:1.7	User locked - Wrong credentials	Interface
SECUR_EVT_PW_ENTRY_UNBLOCKED	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-001	User unlocked	Interface
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-002	Log-in attempt when user is locked	Interface
SECUR_EVT_INVALID_PW_ENTERED	62443-ACCESS_CONTROL	Notice	LOGIN_FAIL_WRONG_ CR	IEC 62351-14:1.3	Log-in failed - Wrong credentials	Interface
SECUR_EVT_PW_TIMED_OUT	62443-ACCESS_CONTROL	error	LOGIN_FAIL_CRED_EXPIRE	IEC 62351-14:1.4	Log-in failed - credentials expired.	Interface
SECUR_EVT_RECOVERY_PW_ENTERED	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-004	Recovery password entered	Interface
SECUR_EVT_IED_SEC_CODE_READ	62443-AUDIT_LOG	Info	-	2910-MiCP40-005	Security Code read	Interface
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	62443-AUDIT_LOG	Info	-	2910-MiCP40-006	Security Code Timer expired	Interface
SECUR_EVT_PORT_DISABLED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-007	Port Disabled	Interface
SECUR_EVT_PORT_ENABLED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-008	Port Enabled	Interface, Port number

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_PSL_ SETTINGS_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-009	PSL Settings downloaded to device	Interface, Port number
SECUR_EVT_DNP_ SETTINGS_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-010	DNP Settings downloaded to device	Interface, Group number
SECUR_EVT_TRACE_ DATA_DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-011	TRACE Data downloaded to device	Interface
SECUR_EVT_61850_ CONFIG_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-012	IEC61850 Config downloaded to device	Interface
SECUR_EVT_USER_ CURVES_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-013	User Curves downloaded to device	Interface
SECUR_EVT_SETTIN G_GRP_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-014	Setting Group downloaded to device	Interface, Curve number
SECUR_EVT_DR_ SETTINGS_ DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-015	DR Settings downloaded to device	Interface, Group number
SECUR_EVT_PSL_ SETTINGS_ UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-016	PSL Settings uploaded from device	Interface
SECUR_EVT_DNP_ SETTINGS_ UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-017	DNP Settings uploaded from device	Interface, Group number
SECUR_EVT_TRACE_ DATA_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-018	TRACE Data uploaded from device	Interface
SECUR_EVT_61850_ CONFIG_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-019	IEC61850 Config uploaded from device	Interface
SECUR_EVT_USER_ CURVES_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-020	User Curves uploaded from device	Interface
SECUR_EVT_PSL_ CONFIG_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-021	PSL Config uploaded from device	Interface, Curve number
SECUR_EVT_ SETTINGS_ UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-022	Settings uploaded from device	Interface, Group number
SECUR_EVT_CS_ SETTINGS_CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-023	Control & Support settings changed	Interface
SECUR_EVT_DR_ SETTINGS_CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-024	Disturbance Record Settings changed	Interface
SECUR_EVT_ SETTING_GROUP_ CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-025	Setting Group changed	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
SECUR_EVT_ DEFAULT_SETTINGS_ RESTORED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-026	Default Settings restored	Interface, Group number
SECUR_EVT_ DEFAULT_USRCURVE_ RESTORED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-027	Default User Curve restored	Interface
SECUR_EVT_POWER_ON	62443-CONTROL_SYSTEM	Notice	-	2910-MiCP40-028	Device Powered On	Interface, Curve number
SECUR_EVT_RADIUS_UNAVAIL	62443-AUDIT_LOG	warning	RBAC_NO_RADIUS	IEC 62351-8:1.3	RADIUS server not available	Interface
SECUR_EVT_ SESSION_LIMIT	62443-AUDIT_LOG	Notice	-	2910-MiCP40-030	Active user sessions limit reached	Interface
SECUR_EVT_SLD_ FILE_DOWNLOADED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-031	SLD File downloaded to device	Interface
SECUR_EVT_SLD_ FILE_UPLOADED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-032	SLD File uploaded from device	Interface
SECUR_EVT_RBAC_ LOGIN	62443-ACCESS_CONTROL	Notice	LOGIN_OK	IEC-62351-14:1.1	Log-in successful	Interface
SECUR_EVT_RBAC_ LOGOUT	62443-ACCESS_CONTROL	Notice	LOGOUT_USER	IEC 62351-14:1.8	Log-out (user logged out)	Interface
Bypass mode Activated	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-033	Bypass Mode Activated	Interface
Bypass mode Deactivated	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-034	Bypass Mode Deactivated	Interface
SECUR_EVT_RADIUS_KEY_CHANGED	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-044	RADIUS Secret Key changed	Interface
SECUR_SEC_ SETTINGS_ RESTORED	62443-BACKUP_RESTORE	Notice	-	2910-MiCP40-041	Security settings restored	Interface
Switch to Golden Image	62443-AUDIT_LOG	Notice	-	2910-MiCP40-045	Device switching to Firmware update mode	Interface
FIRMWARE_ VALIDATION_ SUCCESS	62443-AUDIT_LOG	Notice	-	2910-MiCP40-035	Firmware Digital Signature check successful	Interface
FIRMWARE_ VALIDATION_FAIL	62443-AUDIT_LOG	warning	-	2910-MiCP40-036	Firmware Digital Signature check failed	Interface
Firmware update process started	62443-AUDIT_LOG	Notice	-	2910-MiCP40-046	Firmware update initiated	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
Fail to receive firmware files	62443-AUDIT_LOG	Warning	-	2910-MiCP40-047	Firmware files transfer failed	Interface
Fail to update firmware	62443-AUDIT_LOG	Warning	-	2910-MiCP40-048	Firmware update failed	Interface
Firmware update process success	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-049	Firmware update successful	Interface, Previous FW version, Latest FW version
Serial&Model number update success	62443-AUDIT_LOG	Notice	-	2910-MiCP40-050	Serial/Model number update successful	
Serial&Model number update fail	62443-AUDIT_LOG	Warning	-	2910-MiCP40-051	Serial/Model number update failed	Interface
NP1 MAC update success	62443-AUDIT_LOG	Notice	-	2910-MiCP40-052	NP1 MAC address update successful	Interface
NP1 MAC update fail	62443-AUDIT_LOG	Warning	-	2910-MiCP40-053	NP1 MAC address update failed	Interface
NP2 MAC update success	62443-AUDIT_LOG	Notice	-	2910-MiCP40-054	NP2 MAC address update successful	Interface
NP2 MAC update fail	62443-AUDIT_LOG	Warning	-	2910-MiCP40-055	NP2 MAC address update failed	Interface
Fallback to Device Authentication	62443-ACCESS_CONTROL	Warning	-	2910-MiCP40-056	Fallback to Device Authentication	Interface
User logged out due to inactivity timeout	62443-ACCESS_CONTROL	Notice	LOGOUT_TIMEOUT	IEC 62351-14:1.9	Log-out by user inactivity (timeout).	Interface
Security events upload	62443-AUDIT_LOG	Notice	-	2910-MiCP40-042	Security Events uploaded from device	Interface
SSH Passcode change	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-057	SSH pass code change	Interface
SSH Client Authentication Fail	62443-ACCESS_CONTROL	Warning	-	2910-MiCP40-059	Failed client authentication	Interface
SSH Client Authentication Success	62443-ACCESS_CONTROL	Notice	-	2910-MiCP40-058	Successful client authentication	Interface
New User added	62443-CONFIG_CHANGE	Notice	USER_ACCNT_CREATE_OK	IEC 62351-14:2.15	User account created successfully.	Interface

Event	IEC 62443-4 Category	IEC 62351-14 Severity	IEC 62351-14 Mnemonic	IEC 62351-14 ID / Private ID	Text	Extra Info
User deleted	62443-CONFIG_CHANGE	Notice	USER_ACCNT_DEL_OK	IEC 62351-14:2.21	User account deleted successfully.	Interface
User role change	62443-CONFIG_CHANGE	Notice	USER_PERMISSION_CHANGE_OK	IEC 62351-14:2.11	Permission changed successfully.	Interface
User name change	62443-CONFIG_CHANGE	Notice	-	2910-MiCP40-060	User renamed successfully	Interface

Where the Interface values in "Extra Info" parameter are: "UI", "FP", "RP1", "RP2", "NET", "HMI".

17.10.2 SECURITY EVENTS: SYSLOG

Security events are also logged to a remote server and are based on Syslog [RFC 5424].

All login and logout attempts from local and central authentication, whether successful or failed, are logged. The contents of each successful or failed, login and logout security event include a specific username.

The security log cannot be cleared by any of the available roles.

The contents of each login and/or logout security event include the relevant interface. The following interfaces are supported:

Interface	Abbr.
Front Port	FP
Rear Port 1	RP1
Rear Port 2	RP2
Network Port 1 or 2	NET
Front Panel	UI

The following events are available to be logged to the syslog server:

Security Event	SNMP Trap Text
SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
SECUR_EVT_PW_MODIFIED	User password changed successfully
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked – Wrong credentials
SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - Wrong credentials
SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired.
SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
SECUR_EVT_IED_SEC_CODE_READ	Security Code read

Security Event	SNMP Trap Text
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
SECUR_EVT_PORT_DISABLED	Port Disabled
SECUR_EVT_PORT_ENABLED	Port Enabled
SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device
SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
SECUR_EVT_RBAC_LOGIN	Log-in successful
SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
Bypass mode Activated	Bypass Mode Activated
Bypass mode Deactivated	Bypass Mode Deactivated

Security Event	SNMP Trap Text
RADIUS Secret Key changed	RADIUS Secret Key changed
SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
Switch to Golden Image	Device switching to Firmware update mode
Fallback to Device Authentication	Fallback to Device Authentication
User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
Security events upload	Security Events uploaded from device
SSH Passcode change	SSH pass code change
SSH Client Authentication Fail	Failed client authentication
SSH Client Authentication Success	Successful client authentication
New User added	User account created successfully.
User deleted	User account deleted successfully.
User role change	Permission changed successfully.

17.10.3 SYSLOG CLIENT

The IED supports security event reporting through the Syslog protocol for supporting Security Information Event Management (SIEM) systems for centralized cyber security Monitoring over UDP protocol.

The IED is a Syslog client that supports two Syslog servers. The following settings are available in the *SECURITY CONFIG.* column.

Setting Name	Description	Min	Max	Default	Units	User Role Required
SysLog Pri IP	The IP address of the target Syslog server (Primary)	0.0.0.0	223.255.255.254	0.0.0.0	-	SECADM
SysLog Sec IP	The IP address of the target Syslog server (Secondary)	0.0.0.0	223.255.255.254	0.0.0.0	-	SECADM
SysLog Port	The UDP port number of the target Syslog server	1	65535	514	-	SECADM

17.10.4 SYSLOG FUNCTIONALITY

P40 supports IEC 62351-14 based cyber security event monitoring and is based on Syslog [RFC 5424].

Sample Syslog messages are shown below:

Event	Access Method	Syslog Message (As from Syslog Server)
IED Powered On	UI	5492, 2024-06-12T19:18:28.982Z, 423991K, GE_RE_P543_____AB0_o, MiCP40_POWER_ON, 2910-MiCP40-028, notice, IECCTRLSYS, Device Powered On, UI
ADMIN1 Log-in successful	FP	5523, 2024-06-12T20:04:26.851Z, 423991K, GE_RE_P543_____AB0_o, LOGIN_OK, IEC 62351-14:1.1, notice, IECACCCTRL, ADMIN1, SECAM, Log-in successful, FP

Event	Access Method	Syslog Message (As from Syslog Server)
SSH Successful client authentication (S1 Agile)	NET	5460, 2024-06-12T18:04:45.359Z, 423991J, GE_RE_P546_____AB0_o, MiCP40_SSH_CLIENT_AUTH_SUCCESS, 2910-MiCP40-058, notice, IECACCCTRL, Successful client authentication, NET
Firmware update successful	FP	5476, 2024-06-12T19:18:19.004Z, 423991K, GE_RE_P543_____AB0_o, MiCP40_FW_UPDATE_SUCCESS, 2910-MiCP40-049, notice, IECCONFCHG, Firmware update successful, FP, P546_____AB0_o to P543_____AB0_o

17.10.5 SECURITY EVENTS: SNMP

Security events can also be sent as SNMP traps to a remote SNMP server. These traps are supported in both V2c and V3 versions of SNMP. For further information related to the full SNMP interface in P40, refer to the SNMP section in the COMMUNICATIONS chapter.

The format of the SNMP traps for security events consists of three parts as described below:

"Event Description, Username, Interface"

- Event Description: Short description of the alarm, same as the description present in Security event.
- Username: User associated with the event, provided only when Username is available for the Security event.
- Interface: Interface on which Security event has occurred, same as the interface information present in Security event.

The following events are available to be logged to the SNMP server:

Security Event	SNMP Trap Text
SECUR_EVT_PW_SET_NON_COMPLIANT	User Password change failed - policy check failed
SECUR_EVT_PW_MODIFIED	User password changed successfully
SECUR_EVT_PW_ENTRY_NOW_BLOCKED	User locked – Wrong credentials
SECUR_EVT_PW_ENTRY_UNBLOCKED	User unlocked
SECUR_EVT_PW_ENTERED_WHILE_BLOCKED	Log-in attempt when user is locked
SECUR_EVT_INVALID_PW_ENTERED	Log-in failed - Wrong credentials
SECUR_EVT_PW_TIMED_OUT	Log-in failed - credentials expired.
SECUR_EVT_RECOVERY_PW_ENTERED	Recovery password entered
SECUR_EVT_IED_SEC_CODE_READ	Security Code read
SECUR_EVT_IED_SEC_CODE_TMR_EXPIRED	Security Code Timer expired
SECUR_EVT_PORT_DISABLED	Port Disabled
SECUR_EVT_PORT_ENABLED	Port Enabled
SECUR_EVT_PSL_SETTINGS_DOWNLOADED	PSL Settings downloaded to device
SECUR_EVT_DNP_SETTINGS_DOWNLOADED	DNP Settings downloaded to device
SECUR_EVT_61850_CONFIG_DOWNLOADED	IEC61850 Config downloaded to device
SECUR_EVT_USER_CURVES_DOWNLOADED	User Curves downloaded to device

Security Event	SNMP Trap Text
SECUR_EVT_SETTING_GRP_DOWNLOADED	Setting Group downloaded to device
SECUR_EVT_DR_SETTINGS_DOWNLOADED	DR Settings downloaded to device
SECUR_EVT_PSL_SETTINGS_UPLOADED	PSL Settings uploaded from device
SECUR_EVT_DNP_SETTINGS_UPLOADED	DNP Settings uploaded from device
SECUR_EVT_61850_CONFIG_UPLOADED	IEC61850 Config uploaded from device
SECUR_EVT_USER_CURVES_UPLOADED	User Curves uploaded from device
SECUR_EVT_PSL_CONFIG_UPLOADED	PSL Config uploaded from device
SECUR_EVT_SETTINGS_UPLOADED	Settings uploaded from device
SECUR_EVT_CS_SETTINGS_CHANGED	Control & Support settings changed
SECUR_EVT_DR_SETTINGS_CHANGED	Disturbance Record Settings changed
SECUR_EVT_SETTING_GROUP_CHANGED	Setting Group changed
SECUR_EVT_DEFAULT_SETTINGS_RESTORED	Default Settings restored
SECUR_EVT_DEFAULT_USRCURVE_RESTORED	Default User Curve restored
SECUR_EVT_POWER_ON	Device Powered On
SECUR_EVT_RADIUS_UNAVAIL	RADIUS server not available
SECUR_EVT_SESSION_LIMIT	Active user sessions limit reached
SECUR_EVT_SLD_FILE_DOWNLOADED	SLD File downloaded to device
SECUR_EVT_SLD_FILE_UPLOADED	SLD File uploaded from device
SECUR_EVT_RBAC_LOGIN	Log-in successful
SECUR_EVT_RBAC_LOGOUT	Log-out (user logged out)
Bypass mode Activated	Bypass Mode Activated
Bypass mode Deactivated	Bypass Mode Deactivated
RADIUS Secret Key changed	RADIUS Secret Key changed
SECUR_EVT_SEC_SETTINGS_RESTORED	Security settings restored
Switch to Golden Image	Device switching to Firmware update mode
Fallback to Device Authentication	Fallback to Device Authentication
User logged out due to inactivity timeout.	Log-out by user inactivity (timeout)
Security events upload	Security Events uploaded from device

Security Event	SNMP Trap Text
SSH Passcode change	SSH pass code change
SSH Client Authentication Fail	Failed client authentication
SSH Client Authentication Success	Successful client authentication
New User added	User account created successfully.
User deleted	User account deleted successfully.
User role change	Permission changed successfully.

CHAPTER 18

INSTALLATION

18.1 CHAPTER OVERVIEW

This chapter provides information about installing the product.

This chapter contains the following sections:

Chapter Overview 430
Handling the Goods 431
Mounting the Device 432
Cables and Connectors 435
Case Dimensions 440

18.2 HANDLING THE GOODS

Our products are of robust construction but require careful treatment before installation on site. This section discusses the requirements for receiving and unpacking the goods, as well as associated considerations regarding product care and personal safety.

Caution:
Before lifting or moving the equipment you should be familiar with the Safety Information chapter of this manual.

18.2.1 RECEIPT OF THE GOODS

On receipt, ensure the correct product has been delivered. Unpack the product immediately to ensure there has been no external damage in transit. If the product has been damaged, make a claim to the transport contractor and notify us promptly.

For products not intended for immediate installation, repack them in their original delivery packaging.

18.2.2 UNPACKING THE GOODS

When unpacking and installing the product, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any CDROMs or technical documentation (where included). These should accompany the unit to its destination substation and put in a dedicated place.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies where installation is being carried out at the same time as construction work.

18.2.3 STORING THE GOODS

If the unit is not installed immediately, store it in a place free from dust and moisture in its original packaging. Keep any dehumidifier bags included in the packing. The dehumidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals before replacing it in the carton. Ideally regeneration should be carried out in a ventilating, circulating oven at about 115°C. Bags should be placed on flat racks and spaced to allow circulation around them. The time taken for regeneration will depend on the size of the bag. If a ventilating, circulating oven is not available, when using an ordinary oven, open the door on a regular basis to let out the steam given off by the regenerating silica gel.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. Avoid storing in locations of high humidity. In locations of high humidity the packaging may become impregnated with moisture and the dehumidifier crystals will lose their efficiency.

The device can be stored between –25º to +70ºC for unlimited periods or between -40°C to + 85°C for up to 96 hours (see technical specifications).

To avoid deterioration of electrolytic capacitors, power up units that are stored in a de-energised state once a year, for one hour continuously.

18.2.4 DISMANTLING THE GOODS

If you need to dismantle the device, always observe standard ESD (Electrostatic Discharge) precautions. The minimum precautions to be followed are as follows:

- Use an antistatic wrist band earthed to a suitable earthing point.
- Avoid touching the electronic components and PCBs.

18.3 MOUNTING THE DEVICE

The products are dispatched either individually or as part of a panel or rack assembly.

Individual products are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centres.

The products are designed so the fixing holes in the mounting flanges are only accessible when the access covers are open.

If you use a P991 or MMLG test block with the product, when viewed from the front, position the test block on the right-hand side of the associated product. This minimises the wiring between the product and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

18.3.1 FLUSH PANEL MOUNTING

Panel-mounted devices are flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Caution:
Do not use conventional self-tapping screws, because they have larger heads and could damage the faceplate.

Alternatively, you can use tapped holes if the panel has a minimum thickness of 2.5 mm.

For applications where the product needs to be semi-projection or projection mounted, a range of collars are available.

If several products are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.

Caution:
Do not fasten products with pop rivets because this makes them difficult to remove if repair becomes necessary.

18.3.2 RACK MOUNTING

Panel-mounted variants can also be rack mounted using single-tier rack frames (our part number FX0021 001), as shown in the figure below. These frames are designed with dimensions in accordance with IEC 60297 and are supplied pre-assembled ready to use. On a standard 483 mm (19 inch) rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the products by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit).

Caution:
Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS products because they have slightly larger heads.

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

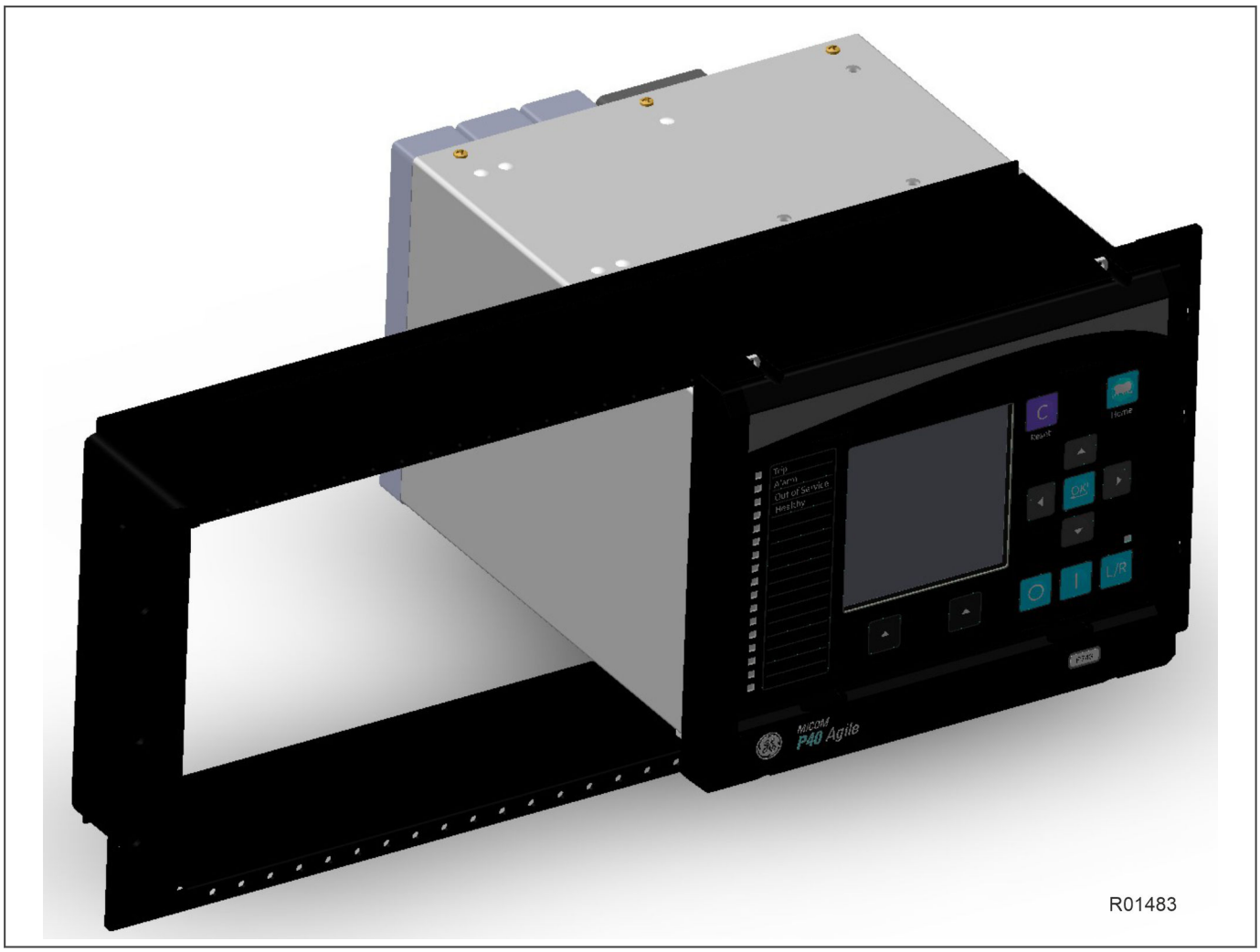


Figure 176: Rack mounting of products

Products can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from different product ranges to be pre-wired together before mounting.

Use blanking plates to fill any empty spaces. The spaces may be used for installing future products or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. The part numbers are as follows:

Case size summation	Blanking plate part number
5TE	GJ2028 001
10TE	GJ2028 002
20TE	GJ2028 004
40TE	GJ2028 008
60TE	GJ2028 012

18.3.3 REFURBISHMENT SOLUTIONS

A major advantage of the 5th Generation MiCOM 5th Generation series is the ease in which you can refurbish both older 5th Generation generation and legacy MBCH/KBCH devices. The P40 5th Generation platform retains form, fit and function compatibility, compared to older generations, while delivering the latest platform and software. For example, the 5th Generation line differential protection is fully compatible with all previous 5th Generation versions and maintains pin to pin refurbishment compatibility.

This allows easy upgrade of the protection system with minimum impact, resulting in only a few minutes of downtime.

To begin the upgrade:

- Take the order code (CORTEC) of the older relay being removed, typically a blue case relay
- Translate to today's latest GE Vernova MiCOM model, adding Ethernet options if required
- Order the new 5th Generation P40 relay
- Use the S1 Agile toolsuite to extract settings and logic and convert the settings
- Detach the medium duty terminal blocks from your old device, making sure you leave the wiring attached. It is recommended the CT/VT terminal blocks on the new IED are used during refurbishment
- Carefully examine the terminal blocks to ensure that no physical damage has occurred since installation
- Attach the terminal blocks and wiring from your old device to the new IED. It is recommended to apply rated current and voltage to the relay CT/VT inputs during secondary injection testing to check the continuity of the CT/VT terminal block connections to the relay
- Download your converted files
- Test, then return circuit to service. See the **Commissioning Instructions** chapter for more information on testing

Please contact us for assistance.

18.4 CABLES AND CONNECTORS

This section describes the type of wiring and connections that should be used when installing the device. For pin-out details please refer to the Hardware Design chapter or the wiring diagrams.

Caution:
Before carrying out any work on the equipment you should be familiar with the Safety Section and the ratings on the equipment's rating label.

18.4.1 TERMINAL BLOCKS

The device may use one or more of the terminal block types shown in the following diagram. The terminal blocks are fastened to the rear panel with screws.

- Heavy duty (HD) terminal blocks for CT and VT circuits
- Medium duty (MD) terminal blocks for the power supply, relay outputs and rear communications port
- MiDOS terminal blocks for CT and VT circuits
- RTD/CLIO terminal block for connection to analogue transducers

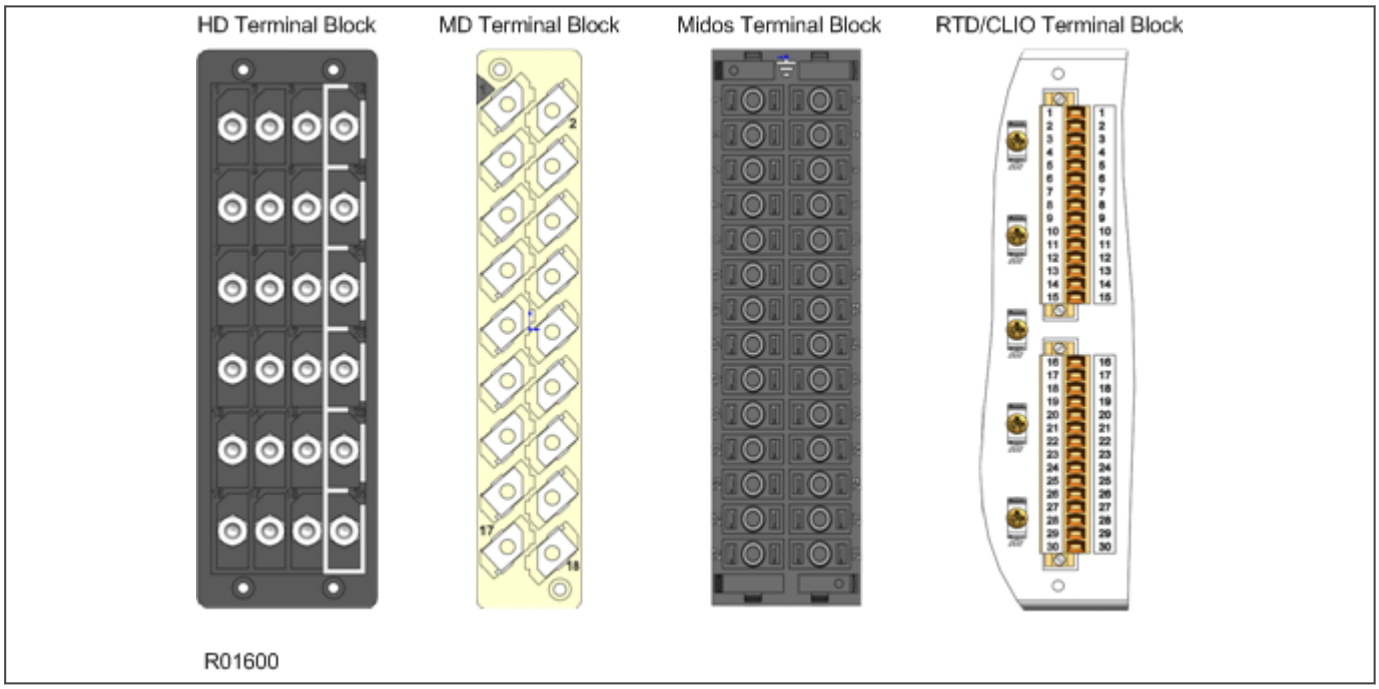


Figure 177: Terminal block types

MiCOM products are supplied with sufficient M4 screws for making connections to the rear mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per terminal.

If required, M4 90° crimp ring terminals can be supplied in three different sizes depending on wire size. Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 - 1.65 mm^2 (22 – 16 AWG)	Red
ZB9124 900	1.04 - 2.63 mm^2 (16 – 14 AWG)	Blue

Note:
IP2x shields and side cover panels may be fitted to provide IP20 ingress protection for MiCOM terminal blocks. The shields and covers can be attached during installation or retrofitted to upgrade existing installations. The shields are supplied with four language fitting instructions, publication number: IP2x-TM-4L-n (where n is the current issue number). For more information, contact your local sales office or our worldwide Contact Centre.

18.4.2 POWER SUPPLY CONNECTIONS

These should be wired with 1.5 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

Caution:
Protect the auxiliary power supply wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

18.4.3 EARTH CONNNECTION

Every device must be connected to the cubicle earthing bar using the M4 earth terminal.

Use a wire size of at least 2.5 mm^2 terminated with a ring terminal.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Note:
To prevent any possibility of electrolytic action between brass or copper ground conductors and the rear panel of the product, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the product case, or using tinned ring terminals.

18.4.4 CURRENT TRANSFORMERS

Current transformers would generally be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Due to the physical limitations of the ring terminal, the maximum wire size you can use is 6.0 mm^2 using ring terminals that are not pre-insulated. If using pre insulated ring terminals, the maximum wire size is reduced to 2.63 mm^2 per ring terminal. If you need a greater cross-sectional area, use two wires in parallel, each terminated in a separate ring terminal.

The wire should have a minimum voltage rating of 300 V RMS.

Caution:
Current transformer circuits must never be fused.

Note:
If there are CTs present, spring-loaded shorting contacts ensure that the terminals into which the CTs connect are shorted before the CT contacts are broken.

Note:
For 5A CT secondaries, we recommend using 2 x 2.5 mm^2 PVC insulated multi-stranded copper wire.

18.4.5 VOLTAGE TRANSFORMER CONNECTIONS

Voltage transformers should be wired with 2.5 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

18.4.6 WATCHDOG CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

The wire should have a minimum voltage rating of 300 V RMS.

18.4.7 EIA(RS)485 AND K-BUS CONNECTIONS

For connecting the EIA(RS485) / K-Bus ports, use 2-core screened cable with a maximum total length of 1000 m or 200 nF total cable capacitance.

To guarantee the performance specifications, you must ensure continuity of the screen, when daisy chaining the connections.

Two-core screened twisted pair cable should be used. It is important to avoid circulating currents, which can cause noise and interference, especially when the cable runs between buildings. For this reason, the screen should be continuous and connected to ground at one end only, normally at the master connection point.

The K-Bus signal is a differential signal and there is no signal ground connection. If a signal ground connection is present in the bus cable then it must be ignored. At no stage should this be connected to the cable's screen or to the product’s chassis. This is for both safety and noise reasons.

A typical cable specification would be:

- Each core: 16/0.2 mm^2 copper conductors, PVC insulated
- Nominal conductor area: 0.5 mm^2 per core
- Screen: Overall braid, PVC sheathed

18.4.8 IRIG-B CONNECTION

The IRIG-B input and BNC connector have a characteristic impedance of 50 ohms. We recommend that connections between the IRIG-B equipment and the product are made using coaxial cable of type RG59LSF with a halogen free, fire retardant sheath.

18.4.9 OPTO-INPUT CONNECTIONS

These should be wired with 1 mm^2 PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

Each opto-input has a selectable preset ½ cycle filter. This makes the input immune to noise induced on the wiring. This can, however slow down the response. If you need to switch off the ½ cycle filter, either use double pole switching on the input, or screened twisted cable on the input circuit.

Caution:
Protect the opto-inputs and their wiring with a maximum 16 A high rupture capacity (HRC) type NIT or TIA fuse.

18.4.10 OUTPUT RELAY CONNECTIONS

These should be wired with 1 mm PVC insulated multi-stranded copper wire terminated with M4 ring terminals.

18.4.11 ETHERNET METALLIC CONNECTIONS

If the device has a metallic Ethernet connection, it can be connected to either a 10Base-T or a 100Base-TX Ethernet hub. Due to noise sensitivity, we recommend this type of connection only for short distance connections, ideally where the products and hubs are in the same cubicle. For increased noise immunity, CAT 6 (category 6) STP (shielded twisted pair) cable and connectors can be used.

The connector for the Ethernet port is a shielded RJ-45. The pin-out is as follows:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

18.4.12 ETHERNET FIBRE CONNECTIONS

We recommend the use of fibre-optic connections for permanent connections in a substation environment. The 100 Mbps fibre optic port uses type LC connectors (one for Tx and one for Rx), compatible with 50/125 µm or 62.5/125 µm multimode fibres at 1300 nm wavelength.

18.4.13 USB CONNECTION

The IED has a type B USB socket inside the bottom compartment. A standard USB printer cable (type A one end, type B the other end) can be used to connect a local PC to the IED. This cable is the same as that used for connecting a printer to a PC.

18.4.14 RTD CONNECTIONS

Resistance Temperature Detector (RTD) inputs use screw clamp connectors. The connection block is situated at the rear of the IED. It can accept wire sizes from 0.1 mm^2 to 1.5 mm^2. The connections between the IED and the RTDs must be made using a screened 3-core cable with a total resistance less than 10 Ω. The cable should have a minimum voltage rating of 300 V RMS.

A 3-core cable should be used even for 2-wire RTD applications, as it allows for the cable's resistance to be removed from the overall resistance measurement. In such cases the third wire is connected to the second wire at the point where the cable is joined to the RTD.

The screen of each cable must only be earthed (grounded) at one end, preferably at the IED end and must be continuous. Multiple earthing (grounding) of the screen can cause circulating current to flow along the screen. This induces noise and is also unsafe.

You should minimize the noise pick-up in the RTD cables by keeping them close to earthed (grounded) metal casings and avoid areas of high electromagnetic and radio interference. The RTD cables should not be run adjacent to or in the same conduit as other high voltage or current cables.

A typical cable specification would be:

- Each core: 7/0.2 mm copper conductors heat resistant PVC insulated
- Nominal conductor area: 0.22 mm2 per core
- Screen: Nickel-plated copper wire braid heat resistant PVC sheathed

The following extract may be useful in defining cable recommendations for the RTDs:

Noise pick up by cables can be categorized into three types:

- Resistive
- Capacitive
- Inductive

Resistive coupling requires an electrical connection to the noise source. Assuming the wire and cable insulation are in good condition and the junctions are clean, this can be dismissed. Capacitive coupling requires sufficient capacitance to the noise source. This is a function of the dielectric strength between the signal cable on the noise source and the power of the noise source. Inductive coupling occurs when the signal cable is adjacent to a wire carrying the noise or it is exposed to a radiated EMF.

Standard screened cable is normally used to protect against capacitively-coupled noise. However for this to be effective, the screen should only be bonded to the system ground at one point. Otherwise a current could flow and the noise would be coupled into the signal wires of the cable. There are different types of screening available, but the most commonly used are aluminium foil wrap, or tin-copper braid. Foil screens are good for low to medium frequencies and braid is good for high frequencies. High-fidelity screen cables provide both types.

Protection against inductive coupling requires careful cable routing and magnetic shielding. The latter can be achieved with steel-armoured cable and steel cable trays. The cable armour must be grounded at both ends so the EMF of the induced current cancels the field of the noise source and shields the cables conductors from it. However, the system ground must be designed such that it does not bridge two isolated ground systems. This could be hazardous and defeat the objectives of the original grounding design. The cable should be laid in the cable trays as close as possible to the metal of the tray. Under no circumstance should any power cable be in or near to the tray. Power cables should only cross the signal cables at 90 degrees and never be adjacent to them.

Both the capacitive and inductive screens must be contiguous from the RTD probes to the IED terminals. The best types of cable are those provided by the RTD manufacturers. These are usually three conductors, known as a triad, which are screened with foil. Such triad cables are available in armoured forms as well as multi-triad armoured forms.

18.4.15 CLIO CONNECTIONS

Current Loop Inputs and Outputs (CLIO) use screw clamp connectors. The connection block is situated at the rear of the IED. It can accept wire sizes from 0.1 mm^2 to 1.5 mm^2. We recommend screened cable, and it should have a minimum voltage rating of 300 V RMS.

18.5 CASE DIMENSIONS

Not all products are available in all case sizes.

18.5.1 CASE DIMENSIONS 40TE

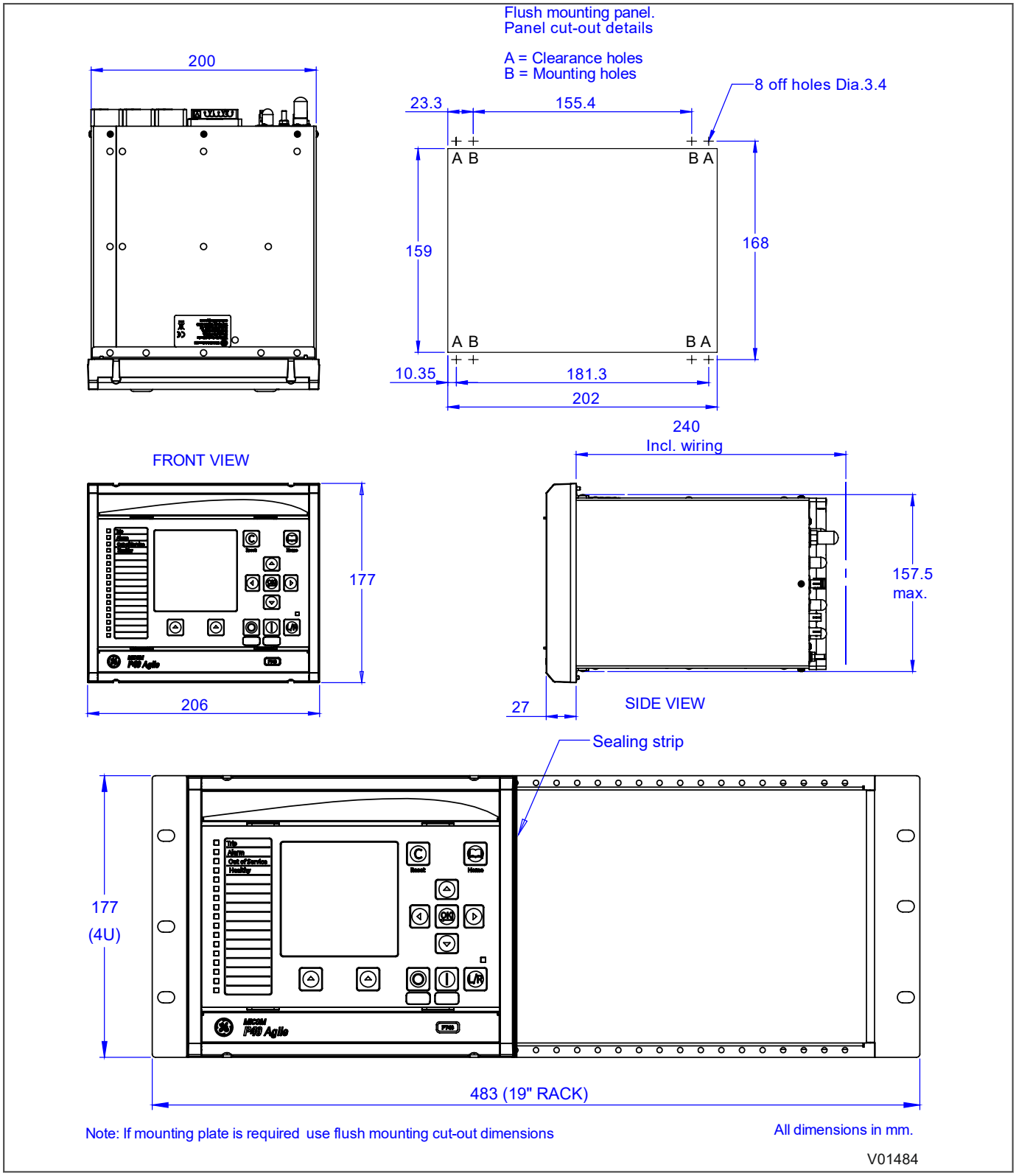


Figure 178: 40TE case dimensions

18.5.2 CASE DIMENSIONS 60TE

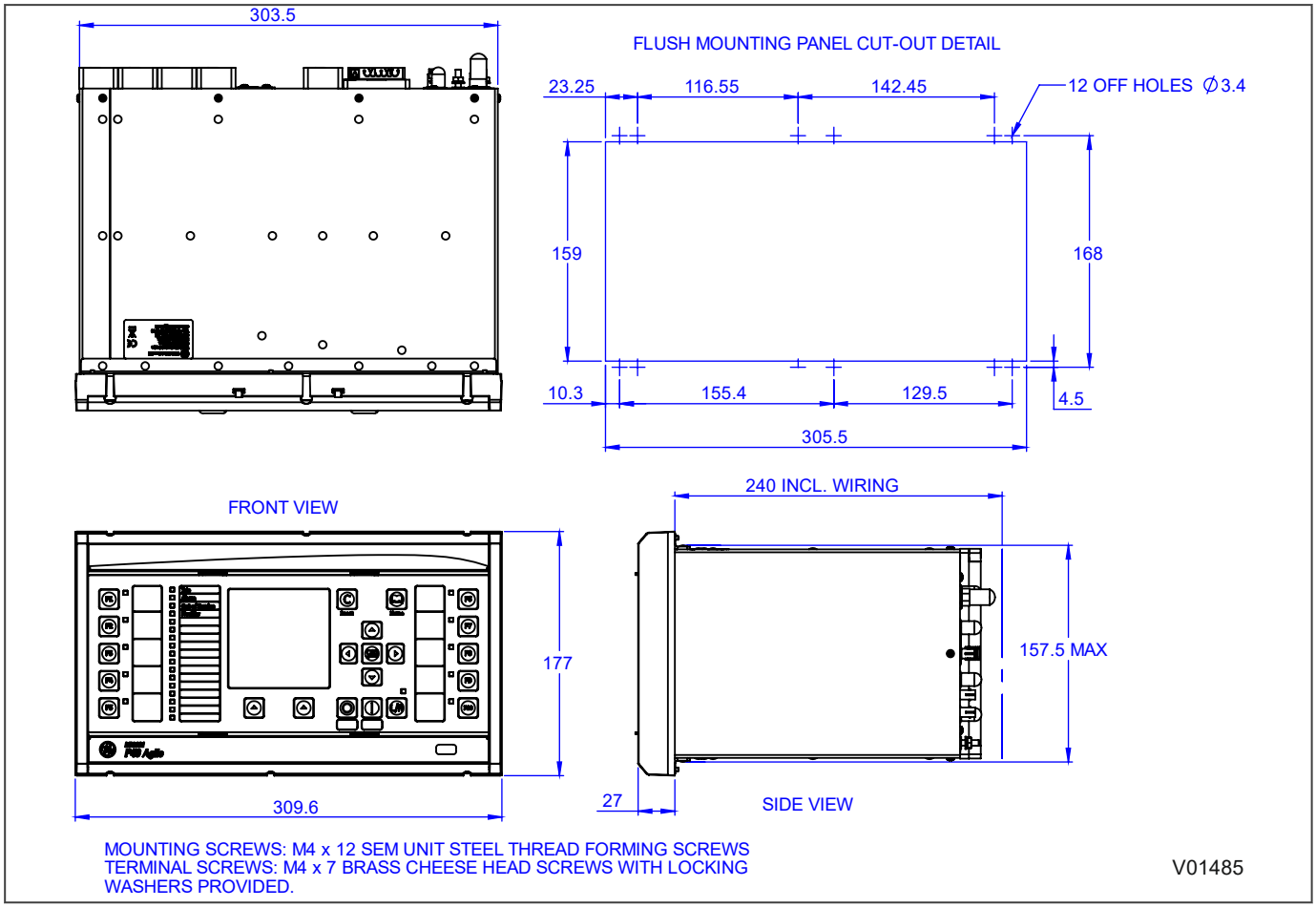


Figure 179: 60TE case dimensions

18.5.3 CASE DIMENSIONS 80TE

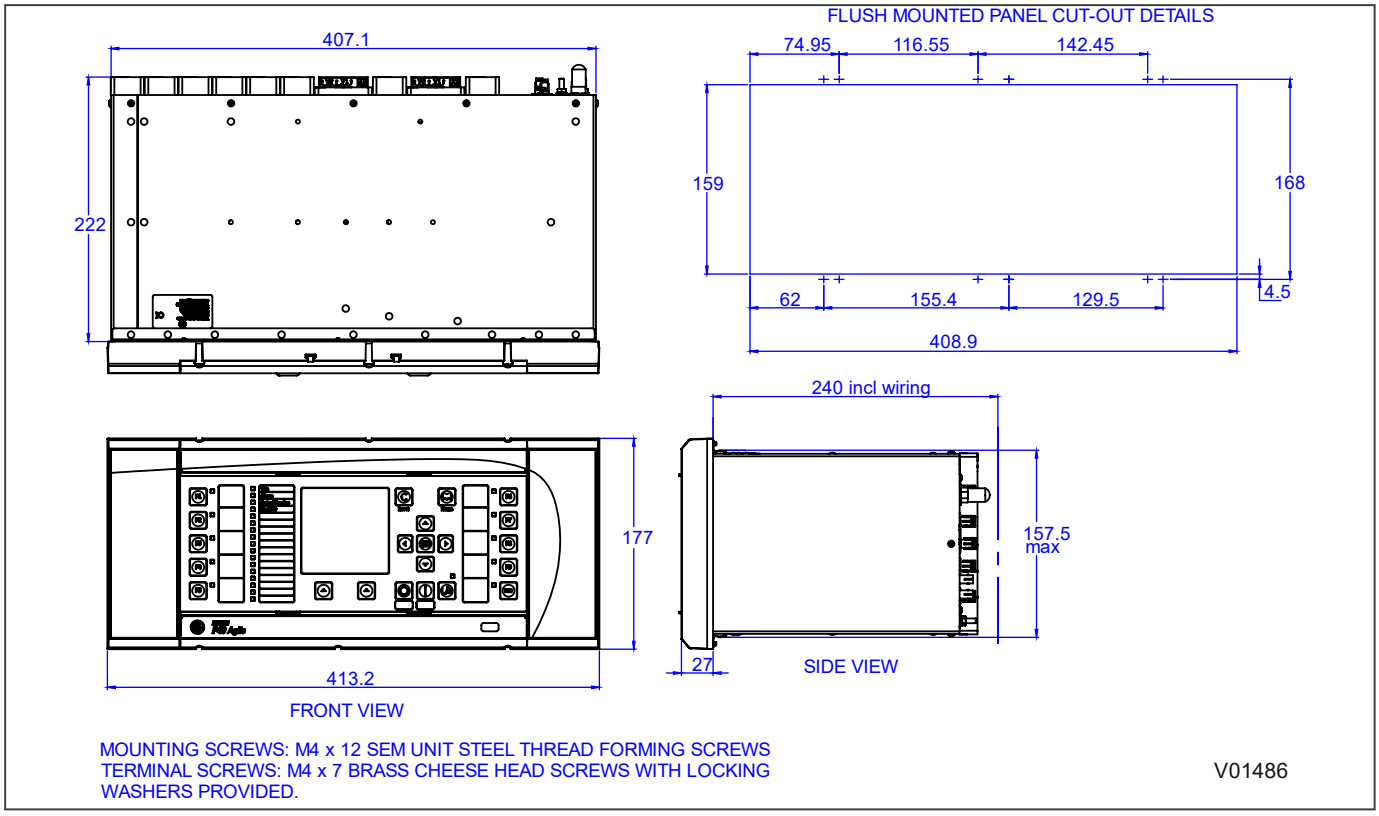


Figure 180: 80TE case dimensions

CHAPTER 19

COMMISSIONING INSTRUCTIONS

19.1 CHAPTER OVERVIEW

This chapter contains the following sections:

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General Guidelines 447
Commissioning Test Menu 448
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19.2 GENERAL GUIDELINES

GE Vernova IEDs are self-checking devices and will raise an alarm in the unlikely event of a failure. This is why the commissioning tests are less extensive than those for non-numeric electronic devices or electro-mechanical relays.

To commission the devices, you (the commissioning engineer) do not need to test every function. You need only verify that the hardware is functioning correctly and that the application-specific software settings have been applied. You can check the settings by extracting them using the settings application software, or by means of the front panel interface (HMI panel).

The menu language is user-selectable, so you can change it for commissioning purposes if required.

Note:
Remember to restore the language setting to the customer's preferred language on completion.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM as well as the ratings on the equipment's rating label.

Warning:
With the exception of the CT shorting contacts check, do not disassemble the device during commissioning.

19.3 COMMISSIONING TEST MENU

The IED provides several test facilities under the *COMMISSION TESTS* menu heading. There are menu cells that allow you to monitor the status of the opto-inputs, output relay contacts, internal Digital Data Bus (DDB) signals and user-programmable LEDs. This section describes these commissioning test facilities.

19.3.1 OPTO I/P STATUS CELL (OPTO-INPUT STATUS)

This cell can be used to monitor the status of the opto-inputs while they are sequentially energised with a suitable DC voltage. The cell is a binary string that displays the status of the opto-inputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each logic input.

19.3.2 RELAY O/P STATUS CELL (RELAY OUTPUT STATUS)

This cell can be used to monitor the status of the relay outputs. The cell is a binary string that displays the status of the relay outputs where '1' means energised and '0' means de-energised. If you move the cursor along the binary numbers, the corresponding label text is displayed for each relay output.

The cell indicates the status of the output relays when the IED is in service. You can check for relay damage by comparing the status of the output contacts with their associated bits.

Note:
*When the **Test Mode** cell is set to `Contacts Blocked`, the relay output status indicates which contacts would operate if the IED was in-service. It does not show the actual status of the output relays, as they are blocked.*

19.3.3 TEST MODE CELL

This cell allows you to perform secondary injection testing. It also lets you test the output contacts directly by applying menu-controlled test signals.

To go into test mode, select the `Test Mode` option in the ***Test Mode*** cell. This takes the IED out of service causing an alarm condition to be recorded and the ***Out of Service*** LED to illuminate. This also freezes any information stored in the *CB CONDITION* column. In IEC 60870-5-103 versions, it changes the Cause of Transmission (COT) to Test Mode.

In Test Mode, the output contacts are still active. To disable the output contacts you must select the `Contacts Blocked` option.

Once testing is complete, return the device back into service by setting the ***Test Mode*** Cell back to `Disabled`.

Caution:
When the cell is in Test Mode, the Scheme Logic still drives the output relays, which could result in tripping of circuit breakers. To avoid this, set the *Test Mode* cell to `Contacts Blocked`.

Note:
`Test mode` and `Contacts Blocked` mode can also be selected by energising an opto-input mapped to the Test Mode signal, and the Contact Block signal respectively.

19.3.4 TEST PATTERN CELL

The ***Test Pattern*** cell is used to select the output relay contacts to be tested when the ***Contact Test*** cell is set to `Apply Test`. The cell has a binary string with one bit for each user-configurable output contact, which can be set to '1' to operate the output and '0' to not operate it.

19.3.5 CONTACT TEST CELL

When the `Apply Test` command in this cell is issued, the contacts set for operation change state. Once the test has been applied, the command text on the LCD will change to ***No Operation*** and the contacts will remain in the Test state until reset by issuing the `Remove Test` command. The command text on the LCD will show ***No Operation*** after the `Remove Test` command has been issued.

Note:
*When the **Test Mode** cell is set to `Contacts Blocked` the **Relay O/P Status** cell does not show the current status of the output relays and therefore cannot be used to confirm operation of the output relays. Therefore it will be necessary to monitor the state of each contact in turn.*

19.3.6 TEST LEDS CELL

When the `Apply Test` command in this cell is issued, the user-programmable LEDs illuminate for approximately 2 seconds before switching off, and the command text on the LCD reverts to ***No Operation***.

19.3.7 RED AND GREEN LED STATUS CELLS

These cells contain binary strings that indicate which of the user-programmable red and green LEDs are illuminated when accessing from a remote location. A '1' indicates that a particular LED is illuminated.

Note:
*When the status in both **Red LED Status** and **Green LED Status** cells is '1', this indicates the LEDs illumination is yellow.*

19.3.8 PSL VERIFICIATION

19.3.8.1 TEST PORT STATUS CELL

This cell displays the status of the DDB signals that have been allocated in the ***Monitor Bit*** cells. If you move the cursor along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed as various operating conditions or sequences are applied to the IED. This allows you to test the Programmable Scheme Logic (PSL).

19.3.8.2 MONITOR BIT 1 TO 8 CELLS

The eight Monitor Bit cells allows you to select eight DDB signals that can be observed in the Test Port Status cell or downloaded via the front port.

Each Monitor Bit cell can be assigned to a particular DDB signal. You set it by entering the required DDB signal number from the list of available DDB signals.

The pins of the monitor/download port used for monitor bits are as follows:

Monitor Bit	1	2	3	4	5	6	7	8
Monitor/Download Port Pin	11	12	15	13	20	21	23	24

The signal ground is available on pins 18, 19, 22 and 25.

Caution:
The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.

19.4 COMMISSIONING EQUIPMENT

Specialist test equipment is required to commission this product. We recognise three classes of equipment for commissioning :

- Recommended
- Essential
- Advisory

Recommended equipment constitutes equipment that is both necessary, and sufficient, to verify correct performance of the principal protection functions.

Essential equipment represents the minimum necessary to check that the product includes the basic expected protection functions and that they operate within limits.

Advisory equipment represents equipment that is needed to verify satisfactory operation of features that may be unused, or supplementary, or which may, for example, be integral to a distributed control/automation scheme. Operation of such features may, perhaps, be more appropriately verified as part of a customer defined commissioning requirement, or as part of a system-level commissioning regime.

19.4.1 RECOMMENDED COMMISSIONING EQUIPMENT

The minimum recommended equipment is a multifunctional three-phase AC current and voltage injection test set featuring :

- Controlled three-phase AC current and voltage sources,
- Transient (dynamic) switching between pre-fault and post-fault conditions (to generate delta conditions),
- Dynamic impedance state sequencer (capable of sequencing through 4 impedance states),
- Integrated or separate variable DC supply (0 - 250 V)
- Integrated or separate AC and DC measurement capabilities (0-440V AC, 0-250V DC)
- Integrated and/or separate timer,
- Integrated and/or separate test switches.

In addition, you will need :

- A portable computer, installed with appropriate software to liaise with the equipment under test (EUT). Typically this software will be proprietary to the product's manufacturer (for example MiCOM S1 Agile).
- Suitable electrical test leads.
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- Continuity tester
- Verified application-specific settings files

19.4.2 ESSENTIAL COMMISSIONING EQUIPMENT

As an absolute minimum, the following equipment is required:

- AC current source coupled with AC voltage source
- Variable DC supply (0 - 250V)
- Multimeter capable of measuring AC and DC current and voltage (0-440V AC, 0-250V DC)
- Timer
- Test switches
- Suitable electrical test leads
- Continuity tester

19.4.3 ADVISORY TEST EQUIPMENT

Advisory test equipment may be required for extended commissioning procedures:

- Current clamp meter
- Multi-finger test plug:
  - P992 for test block type P991
  - MMLB for test block type MMLG blocks
- Electronic or brushless insulation tester with a DC output not exceeding 500 V
- KITZ K-Bus - EIA(RS)232 protocol converter for testing EIA(RS)485 K-Bus port
- EIA(RS)485 to EIA(RS)232 converter for testing EIA(RS)485 Courier/MODBUS/IEC60870-5-103/DNP3 port
- A portable printer (for printing a setting record from the portable PC) and or writeable, detachable memory device
- Phase angle meter
- Phase rotation meter
- Fibre-optic power meter.
- Fibre optic test leads (minimum 2). 10m minimum length, multimode 50/125 µm or 62.5µm terminated with BFOC (ST) 2.5 connectors for testing the fibre-optic RP1 port

19.5 PRODUCT CHECKS

These product checks are designed to ensure that the device has not been physically damaged prior to commissioning, is functioning correctly and that all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the IED prior to commissioning, you should make a copy of the settings. This will allow you to restore them at a later date if necessary. This can be done by:

- Obtaining a setting file from the customer.
- Extracting the settings from the IED itself, using a portable PC with appropriate setting software.

If the customer has changed the password that prevents unauthorised changes to some of the settings, either the revised password should be provided, or the original password restored before testing.

Note:
If the password has been lost, a recovery password can be obtained from GE Vernova.

19.5.1 PRODUCT CHECKS WITH THE IED DE-ENERGISED

Warning:
The following group of tests should be carried out without the auxiliary supply being applied to the IED and, if applicable, with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the IED for these checks. If a P991 test block is provided, the required isolation can be achieved by inserting test plug type P992. This open circuits all wiring routed through the test block.

Before inserting the test plug, you should check the scheme diagram to ensure that this will not cause damage or a safety hazard (the test block may, for example, be associated with protection current transformer circuits). The sockets in the test plug, which correspond to the current transformer secondary windings, must be linked before the test plug is inserted into the test block.

Warning:
Never open-circuit the secondary circuit of a current transformer since the high voltage produced may be lethal and could damage insulation.

If a test block is not provided, the voltage transformer supply to the IED should be isolated by means of the panel links or connecting blocks. The line current transformers should be short-circuited and disconnected from the IED terminals. Where means of isolating the auxiliary supply and trip circuit (for example isolation links, fuses and MCB) are provided, these should be used. If this is not possible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

19.5.1.1 VISUAL INSPECTION

Warning:
Check the rating information under the top access cover on the front of the IED.

Warning:
Check that the IED being tested is correct for the line or circuit.

Warning:
Record the circuit reference and system details.

Warning:
Check the CT secondary current rating and record the CT tap which is in use.

Carefully examine the IED to see that no physical damage has occurred since installation.

Ensure that the case earthing connections (bottom left-hand corner at the rear of the IED case) are used to connect the IED to a local earth bar using an adequate conductor.

19.5.1.2 CURRENT TRANSFORMER SHORTING CONTACTS

Check the current transformer shorting contacts to ensure that they close when the heavy-duty terminal block is disconnected from the current input board.

The heavy-duty terminal blocks are fastened to the rear panel using four crosshead screws. These are located two at the top and two at the bottom.

Note:
Use a magnetic bladed screwdriver to minimise the risk of the screws being left in the terminal block or lost.

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed.

19.5.1.3 INSULATION

Insulation resistance tests are only necessary during commissioning if explicitly requested.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a DC voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the IED.

19.5.1.4 EXTERNAL WIRING

Caution:
Check that the external wiring is correct according to the relevant IED and scheme diagrams. Ensure that phasing/phase rotation appears to be as expected.

19.5.1.5 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states:

Terminals	Contact State with Product De-energised
11 - 12 on power supply board	Closed
13 - 14 on power supply board	Open

19.5.1.6 POWER SUPPLY

Depending on its nominal supply rating, the IED can be operated from either a DC only or an AC/DC auxiliary supply. The incoming voltage must be within the operating range specified below.

Without energising the IED measure the auxiliary supply to ensure it is within the operating range.

Nominal supply rating DC	Nominal Supply Rating AC RMS	DC Operating Range	AC Operating Range
24 - 54 V	N/A	19 to 65 V	N/A
48 - 125 V	30 - 100 V	37 to 150 V	24 - 110 V
110 - 250 V	100 - 240 V	87 to 300 V	80 to 265 V

Note:
The IED can withstand an AC ripple of up to 15% of the upper rated voltage on the DC auxiliary supply.

Warning:
Do not energise the IED or interface unit using the battery charger with the battery disconnected as this can irreparably damage the power supply circuitry.

Caution:
Energise the IED only if the auxiliary supply is within the specified operating ranges. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the IED.

19.5.2 PXXX_CI_PRODUCTCHECKSENERGISED

Warning:
The current and voltage transformer connections must remain isolated from the IED for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.

The following group of tests verifies that the IED hardware and software is functioning correctly and should be carried out with the supply applied to the IED.

19.5.2.1 WATCHDOG CONTACTS

Using a continuity tester, check that the Watchdog contacts are in the following states when energised and healthy.

Terminals	Contact State with Product Energised
11 - 12 on power supply board	Open
13 - 14 on power supply board	Closed

19.5.2.2 TEST GRAPHICAL HMI

The Graphical HMI is designed to operate in a wide range of substation ambient temperatures. For this purpose, the IEDs have an ***LCD Brightness*** setting. The brightness is factory pre-set, but it may be necessary to adjust the contrast to give the best in-service display.

To change the contrast, you can increment or decrement the ***LCD Brightness*** cell in the *CONFIGURATION* column.

Caution:
Before applying a brightness setting, make sure that it will not make the display so light or dark that the menu text becomes unreadable. It is possible to restore the visibility of a display by downloading a setting file, and setting the LCD Brightness within the typical range of 7 - 11.

19.5.2.3 DATE AND TIME

The date and time is stored in memory, which is backed up by a supercapacitor.

The method for setting the date and time depends on whether an IRIG-B signal is being used or not. The IRIG-B signal will override the time, day and month settings, but not the initial year setting. For this reason, you must ensure you set the correct year, even if the device is using IRIG-B to maintain the internal clock.

You set the Date and Time by one of the following methods:

- Using the front panel to set the ***Date and Time*** cells respectively
- By sending a courier command to the ***Date/Time*** cell (Courier reference 0801)

Note:
If the auxiliary supply fails, the time and date will be maintained by the supercapacitor. Therefore, when the auxiliary supply is restored, you should not have to set the time and date again. To test this, remove the IRIG-B signal, and then remove the auxiliary supply. Leave the device de-energised for approximately 30 seconds. On re energisation, the time should be correct.

When using IRIG-B to maintain the clock, the IED must first be connected to the satellite clock equipment (usually an RT430), which should be energised and functioning.

1. Set the IRIG-B Sync cell in the *DATE AND TIME* column to `Enabled`.
2. Ensure the IED is receiving the IRIG-B signal by checking that cell IRIG-B Status reads `Active`.
3. Once the IRIG-B signal is active, adjust the time offset of the universal co coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.
4. Check that the time, date and month are correct in the Date/Time cell. The IRIG-B signal does not contain the current year so it will need to be set manually in this cell.
5. Reconnect the IRIG-B signal.

If the time and date is not being maintained by an IRIG-B signal, ensure that the IRIG-B Sync cell in the *DATE AND TIME* column is set to `Disabled`.

1. Set the date and time to the correct local time and date using Date/Time cell or using the serial protocol.

19.5.2.4 TEST LEDS

On power-up, all LEDs should first flash yellow. Following this, the green "Healthy" LED should illuminate indicating that the device is healthy.

The IED's non-volatile memory stores the states of the alarm, the trip, and the user-programmable LED indicators (if configured to latch). These indicators may also illuminate when the auxiliary supply is applied.

If any of these LEDs are ON then they should be reset before proceeding with further testing. If the LEDs successfully reset (the LED goes off), no testing is needed for that LED because it is obviously operational.

19.5.2.5 TEST ALARM AND OUT-OF-SERVICE LEDS

The alarm and out of service LEDs can be tested using the *COMMISSION TESTS* menu column.

1. Set the ***Test Mode*** cell to `Contacts Blocked`.
2. Check that the out of service LED illuminates continuously and the alarm LED flashes.

It is not necessary to return the ***Test Mode*** cell to `Disabled` at this stage because the test mode will be required for later tests.

19.5.2.6 TEST TRIP LED

The trip LED can be tested by initiating a manual circuit breaker trip. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

19.5.2.7 TEST USER-PROGRAMMABLE LEDS

To test these LEDs, set the Test LEDs cell to `Apply Test`. Check that all user-programmable LEDs illuminate.

19.5.2.8 TEST OPTO-INPUTS

This test checks that all the opto-inputs on the IED are functioning correctly.

The opto-inputs should be energised one at a time. For terminal numbers, please see the external connection diagrams in the "Wiring Diagrams" chapter. Ensuring correct polarity, connect the supply voltage to the appropriate terminals for the input being tested.

The status of each opto-input can be viewed using either the ***Opto I/P Status*** cell in the *SYSTEM DATA* column, or the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column.

A '1' indicates an energised input and a '0' indicates a de-energised input. When each opto-input is energised, one of the characters on the bottom line of the display changes to indicate the new state of the input.

19.5.2.9 TEST OUTPUT RELAYS

This test checks that all the output relays are functioning correctly.

1. Ensure that the IED is still in test mode by viewing the ***Test Mode*** cell in the *COMMISSION TESTS* column. Ensure that it is set to `Contacts Blocked`.
2. The output relays should be energised one at a time. To select output relay 1 for testing, set the Test Pattern cell as appropriate.
3. Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the external connection diagram.
4. To operate the output relay set the Contact Test cell to `Apply Test`.
5. Check the operation with the continuity tester.
6. Measure the resistance of the contacts in the closed state.
7. Reset the output relay by setting the Contact Test cell to `Remove Test`.
8. Repeat the test for the remaining output relays.
9. Return the IED to service by setting the Test Mode cell in the *COMMISSION TESTS* menu to `Disabled`.

19.5.2.10 RTD INPUTS

This test checks that all the RTD inputs are functioning correctly, if the RTD board is fitted.

Please refer to the wiring diagrams for details of the terminal connections.

1. You should connect a 100 ohm resistor across each RTD in turn. The resistor needs to have a very small tolerance (0.1%). You must connect the RTD common return terminal to the correct RTD input, otherwise the device will report an RTD error.
2. Check that the corresponding temperature displayed in the *MEASUREMENTS 3* column of the menu is 0°C +/-2°C. This range takes into account the 0.1% resistor tolerance and device accuracy of +/-1°C. If a resistor of lower accuracy is used during testing, the acceptable setting range needs to be increased.

19.5.2.11 CURRENT LOOP OUTPUTS

This test checks that all the current loop outputs are functioning correctly, if the board is fitted.

Please refer to the wiring diagrams for details of the terminal connections. Note that for the current loop outputs, the physical connection of the 1 mA output is different from that of the other types.

1. Enable the current loop output to be tested.
2. Note the current loop output type (***CLO Type***) for the application.
3. Note the current loop output parameter (***CLO Parameter***)
4. Note the current loop output minimum and maximum settings (***CLO Minimum*** and ***CLO Maximum***)
5. Apply the appropriate analog input quantity to match the ***CLO Parameter*** at a value equal to (CLO maximum + CLO minimum)/2. The current loop output should be at 50% of its maximum rated output.
6. Using a precision resistive current shunt and a high-resolution voltmeter, check that the current loop output is at 50% of its maximum rated output according to the range as follows:

   0.5 mA (0 to 1 mA CLO)

   5 mA (0 to 10 mA CLO)

   10 mA (0 to 20, 4 to 20 mA CLO)
7. The accuracy should be within +/-0.5% of full scale + meter accuracy.

19.5.2.12 CURRENT LOOP INPUTS

This test checks that all the current loop inputs are functioning correctly, if the board is fitted.

Please refer to the wiring diagrams for details of the terminal connections. Note that for the current loop inputs, the physical connection of the 1 mA input is different from that of the other types.

You can use an accurate DC current source to apply various current levels to the current loop inputs. One approach to this is to use a current loop output as a DC current sources. If you stimulate the current loop output by applying an appropriate signal to the input to which it has been assigned with the ***CLO Parameter*** setting, you will get an appropriate DC signal if the output is enabled.

1. Enable the current loop input to be tested.
2. Note the CLIx minimum and maximum settings and the CLIx Input type for the application.
3. Apply a DC current to the current loop input at 50% of the CLI input maximum range, 0.5 mA (0 to 1 mA CLI), 5 mA (0 to 10 mA CLI) or 10 mA (0 to 20, 4 to 20 mA CLI).
4. Check the accuracy of the current loop input using the CLIO Input 1/2/3/4 cells in the *MEASUREMENTS 3* column. The display should show (CLIx maximum + CLIx minimum)/2 +/-1% full scale accuracy.

19.5.2.13 TEST SERIAL COMMUNICATION PORT RP1

You need only perform this test if the IED is to be accessed from a remote location with a permanent serial connection to the communications port. The scope of this test does not extend to verifying operation with connected equipment beyond any supplied protocol converter. It verifies operation of the rear communication port (and if applicable the protocol converter) and varies according to the protocol fitted.

19.5.2.13.1 CHECK PHYSICAL CONNECTIVITY

The rear communication port RP1 is presented on terminals 16, 17 and 18 of the power supply terminal block. Screened twisted pair cable is used to make a connection to the port. The cable screen should be connected to pin 16 and pins 17 and 18 are for the communication signal:

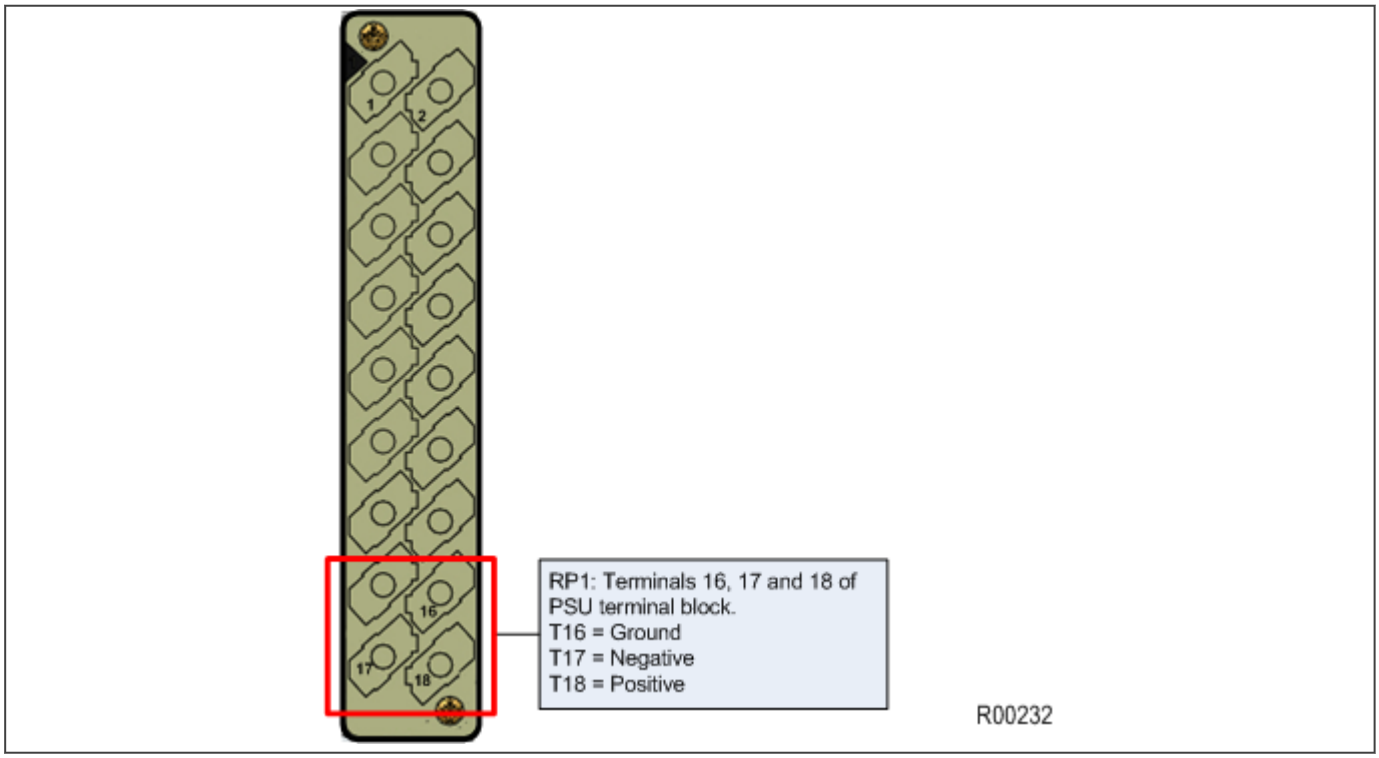


Figure 181: RP1 physical connection

For K-Bus applications, pins 17 and 18 are not polarity sensitive and it does not matter which way round the wires are connected. EIA(RS)485 is polarity sensitive, so you must ensure the wires are connected the correct way round (pin 18 is positive, pin 17 is negative).

If K-Bus is being used, a Kitz protocol converter (KITZ101, KITZ102 OR KITZ201) will have been installed to convert the K-Bus signals into RS232. Likewise, if RS485 is being used, an RS485-RS232 converter will have been installed. In the case where a protocol converter is being used, a laptop PC running appropriate software (such as MiCOM S1 Agile) can be connected to the incoming side of the protocol converter. An example for K-bus to RS232 conversion is shown below. RS485 to RS232 would follow the same principle, only using a RS485-RS232 converter. Most modern laptops have USB ports, so it is likely you will also require a RS232 to USB converter too.

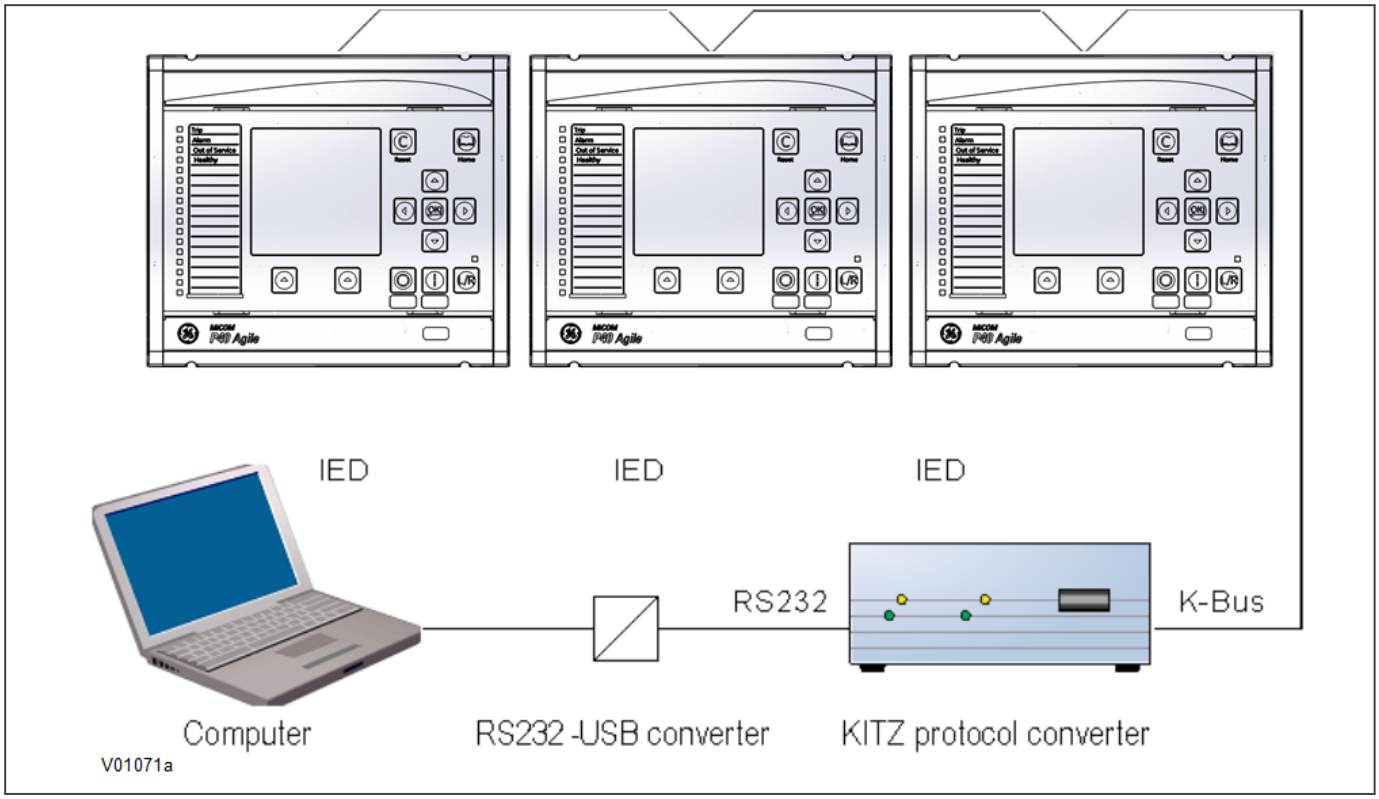


Figure 182: Remote communication using K-bus

Fibre Connection

Some models have an optional fibre optic communications port fitted (on a separate communications board). The communications port to be used is selected by setting the Physical Link cell in the *COMMUNICATIONS* column, the values being `Copper` or `K-Bus` for the RS485/K-bus port and `Fibre Optic` for the fibre optic port.

19.5.2.13.2 CHECK LOGICAL CONNECTIVITY

The logical connectivity depends on the chosen data protocol, but the principles of testing remain the same for all protocol variants:

1. Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter.
2. For Courier models, ensure that you have set the correct RP1 address
3. Check that communications can be established with this IED using the portable PC/Master Station.

19.5.2.14 TEST SERIAL COMMUNICATION PORT RP2

RP2 is an optional second serial port board providing additional serial connectivity. It provides two 9-pin D-type serial port connectors SK4 and SK5. Both ports are configured as DTE (Date Terminal Equipment) ports. That means they can be connected to communications equipment such as a modem with a straight-through cable.

SK4 can be configured as an EIA(RS232), EIA(RS485), or K-Bus connection for Courier protocol only, whilst SK5 is fixed to EIA(RS)232 for InterMiCOM signalling only.

It is not the intention of this test to verify the operation of the complete communication link between the IED and the remote location, just the IED's rear communication port and, if applicable, the protocol converter.

The only checks that need to be made are as follows:

1. Set the ***RP2 Port Config*** cell in the *COMMUNICATIONS* column to the required physical protocol; (K-Bus, EIA(RS)485, or EIA(RS)232.
2. Set the IED's Courier address to the correct value (it must be between 1 and 254).

19.5.2.15 TEST ETHERNET COMMUNICATION

For products that employ Ethernet communications, we recommend that testing be limited to a visual check that the correct ports are fitted and that there is no sign of physical damage.

If there is no board fitted or the board is faulty, a NIC link alarm will be raised (providing this option has been set in the ***NIC Link Report*** cell in the *COMMUNICATIONS* column).

19.5.3 SECONDARY INJECTION TESTS

Secondary injection testing is carried out to verify the integrity of the VT and CT readings. All devices leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, you must set this in the Frequency cell in the *SYSTEM DATA* column.

The PMU must be installed and connected to a 1pps fibre optic synchronising signal and a demodulated IRIG-B signal, provided by a device such as a REASON RT430.

Connect the current and voltage outputs of the test set to the appropriate terminals of the first voltage and current channel and apply nominal voltage and current with the current lagging the voltage by 90 degrees.

19.5.3.1 TEST CURRENT INPUTS

This test verifies that the current measurement inputs are configured correctly.

1. Using secondary injection test equipment such as an Omicron, apply and measure nominal rated current to each CT in turn.
2. Check its magnitude using a multi-meter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the displayed value. The measured current values will either be in primary or secondary Amperes. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied current.

> *Note:*
> *If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

19.5.3.1.1 CHECK POLARITY OF THREE-PHASE CTS

This test checks the polarity of all three-phase CTs associated with a winding.

1. Apply the same current to phases A, B, and C, phase displaced as for a balanced 3-phase set with standard ABC phase rotation (phase A = 0°, phase B = -120°, phase C = +120°).
2. Starting from CT input 1, apply the balanced current and check the measured residual current in the relevant cell. This will be ***IN-TN1 Deriv Mag***, ***IN-TN2 Deriv Mag***, or ***IN-TN3 Deriv Mag*** depending on the transformer winding to which the current input is assigned.
3. The residual current measured should be less than 0.05 p.u. If high residual current is measured, one or more of the CT circuits for the end concerned may have a problem (for example, an inverted connection). Repeat the same test on the rest of the CT inputs.

19.5.3.2 TEST VOLTAGE INPUTS

This test verifies that the voltage measurement inputs are configured correctly.

1. Using secondary injection test equipment, apply and measure the rated voltage to each voltage transformer input in turn.
2. Check its magnitude using a multimeter or test set readout. Check this value against the value displayed on the HMI panel (usually in *MEASUREMENTS 1* column).
3. Record the value displayed. The measured voltage values will either be in primary or secondary Volts. If the Local Values cell in the *MEASURE'T SETUP* column is set to `Primary`, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio (set in the *CT AND VT RATIOS* column). If the Local Values cell is set to Secondary, the value displayed should be equal to the applied voltage.

> *Note:*
> *If a PC connected to the IED using the rear communications port is being used to display the measured current, the process will be similar. However, the setting of the Remote Values cell in the MEASURE'T SETUP column will determine whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the IED is +/- 1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

19.6 SETTING CHECKS

The setting checks ensure that all of the application-specific settings (both the IED's function and Programmable Scheme Logic settings) have been correctly applied.

> *Note:*
> *If applicable, the trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.*

19.6.1 APPLY APPLICATION-SPECIFIC SETTINGS

There are two different methods of applying the settings to the IED

- Transferring settings to the IED from a pre-prepared setting file using MiCOM S1 Agile
- Enter the settings manually using the IED's front panel HMI

19.6.1.1 TRANSFERRING SETTINGS FROM A SETTINGS FILE

This is the preferred method for transferring function settings. It is much faster and there is a lower margin for error.

1. Connect a PC running the Settings Application Software to the IED's front port, or a rear Ethernet port. Alternatively connect to the rear Courier communications port, using a KITZ protocol converter if necessary.
2. Power on the IED
3. Enter the IP address of the device if it is Ethernet enabled
4. Right-click the appropriate device name in the System Explorer pane and select **Send**
5. In the **Send to** dialog select the setting files and click **Send**

> *Note:*
> *The device name may not already exist in the system shown in **System Explorer**. In this case, perform a **Quick Connect** to the IED, then manually add the settings file to the device name in the system. Refer to the Settings Application Software help for details of how to do this.*

19.6.1.2 ENTERING SETTINGS USING THE HMI

1. Starting at the default display, press the Down cursor key to show the first column heading.
2. Use the horizontal cursor keys to select the required column heading.
3. Use the vertical cursor keys to view the setting data in the column.
4. To return to the column header, either press the Up cursor key for a second or so, or press the **Cancel** key once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the Up cursor key or the Cancel key from any of the column headings. If you use the auto-repeat function of the Up cursor key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. To change the value of a setting, go to the relevant cell in the menu, then press the **Enter** key to change the cell value. A flashing cursor on the LCD shows that the value can be changed. You may be prompted for a password first.
7. To change the setting value, press the vertical cursor keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the left and right cursor keys.

8. Press the **Enter** key to confirm the new setting value or the **Clear** key to discard it. The new setting is automatically discarded if it is not confirmed within 15 seconds.
9. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used. When all required changes have been entered, return to the column heading level and press the down cursor key. Before returning to the default display, the following prompt appears.

```
Update settings?
ENTER or CLEAR
```

10. Press the **Enter** key to accept the new settings or press the **Clear** key to discard the new settings.

Note:
If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.
Control and support settings are updated immediately after they are entered, without the Update settings prompt.
It is not possible to change the PSL using the IED's front panel HMI.

Caution:
Where the installation needs application-specific PSL, the relevant .psl files, must be transferred to the IED, for each and every setting group that will be used. If you do not do this, the factory default PSL will still be resident. This may have severe operational and safety consequences.

19.7 IEC 61850 EDITION 2 TESTING

19.7.1 USING IEC 61850 EDITION 2 TEST MODES

In a conventional substation, functionality typically resides in a single device. It is usually easy to physically isolate these functions, as the hardwired connects can simply be removed. Within a digital substation architecture however, functions may be distributed across many devices. This makes isolation of these functions difficult, because there are no physical wires that can be disconnected on a Ethernet network. Logical isolation of the various functions is therefore necessary.

With devices that support IEC 61850 Edition 2, it is possible to use a test mode to conduct online testing, which helps with the situation. The advantages of this are as follows:

- The device can be placed into a test mode, which can disable the relay outputs when testing the device with test input signals.
- Specific protection and control functions can be logically isolated.
- GOOSE messages can be tagged so that receiving devices can recognise they are test signals.
- An IED receiving simulated GOOSE or Sampled Value messages from test devices can differentiate these from normal process messages, and be configured to respond appropriately.

19.7.1.1 IED TEST MODE BEHAVIOUR

Test modes define how the device responds to test messages, and whether the relay outputs are activated or not. You can select the mode of operation by:

- Using the front panel HMI, with the setting ***IED Test Mode*** under the *COMMISSION TESTS* column.
- Using an IEC 61850 control service to ***System/LLN0.Mod***
- Using an opto-input via PSL with the signal ***Block Contacts***

The following table summarises the IED behaviour under the different modes:

IED Test Mode Setting	Result
Disabled	Normal IED behaviour
Test	Protection remains enabled Output from the device is still active IEC 61850 message output has the 'quality' parameter set to 'test' The device only responds to IEC61850 MMS messages from the client with the 'test' flag set
Contacts Blocked	Protection remains enabled Output from the device is disabled IEC 61850 message output has quality set to ‘test’ The device only responds to IEC 61850 MMS messages from the client with the 'test' flag set

Setting the Test or Contacts Blocked mode puts the whole IED into test mode. The IEC 61850 data object ***Beh*** in all Logical Nodes (except LPHD and any protection Logical Nodes that have Beh = 5 (off) due to the function being disabled) will be set to 3 (test) or 4 (test/blocked) as applicable.

19.7.1.2 SAMPLED VALUE TEST MODE BEHAVIOUR

The SV Test Mode defines how the device responds to test sampled value messages. You can select the mode of operation by using the front panel HMI, with the setting ***SV Test Mode*** under the *IEC 61850-9.2LE* column.

The following table summarises the behaviour for sampled values under the different modes:

SV Test Mode Setting	Result
Disabled	Normal IED behaviour All sampled value data frames received with an IEC 61850 Test quality bit set are treated as invalid The IED will display the measurement values for sampled values with the Simulated flag set but the protection elements within the IED will be blocked
Enabled	All sampled value data frames received are treated as good, no matter if they have an IEC 61850-9-2 Simulated flag set or not

19.7.2 SIMULATED INPUT BEHAVIOUR

Simulated GOOSE messages and sampled value streams can be used during testing.

The ***Subscriber Sim*** setting in the *COMMISSION TESTS* column controls whether a device listens to simulated signals or to real ones. An IEC 61850 control service to System/LPHD.Sim can also be used to change this value.

The device may be presented with both real signals and test signals. An internal state machine is used to control how the device switches between signals:

- The IED will continue subscribing to the 'real' GOOSE1 (in green) until it receives the first simulated GOOSE 1 (in red). This will initiate subscription changeover.
- After changeover to this new state, the IED will continue to subscribe to the simulated GOOSE 1 message (in red). Even if this simulated GOOSE 1 message disappears, the real GOOSE 1 message (in green) will still not be processed. This means all Virtual Inputs derived from the GOOSE 1 message will go to their default state.
- The only way to bring the IED out of this state is to set the ***Subscriber Sim*** setting back to False. The IED will then immediately stop processing the simulated messages and start processing real messages again.
- During above steps, IED1 will continuously process the real GOOSE 2 and GOOSE 3 messages as normal because it has not received any simulated messages for these that would initiate a changeover.

The process is represented in the following figure:

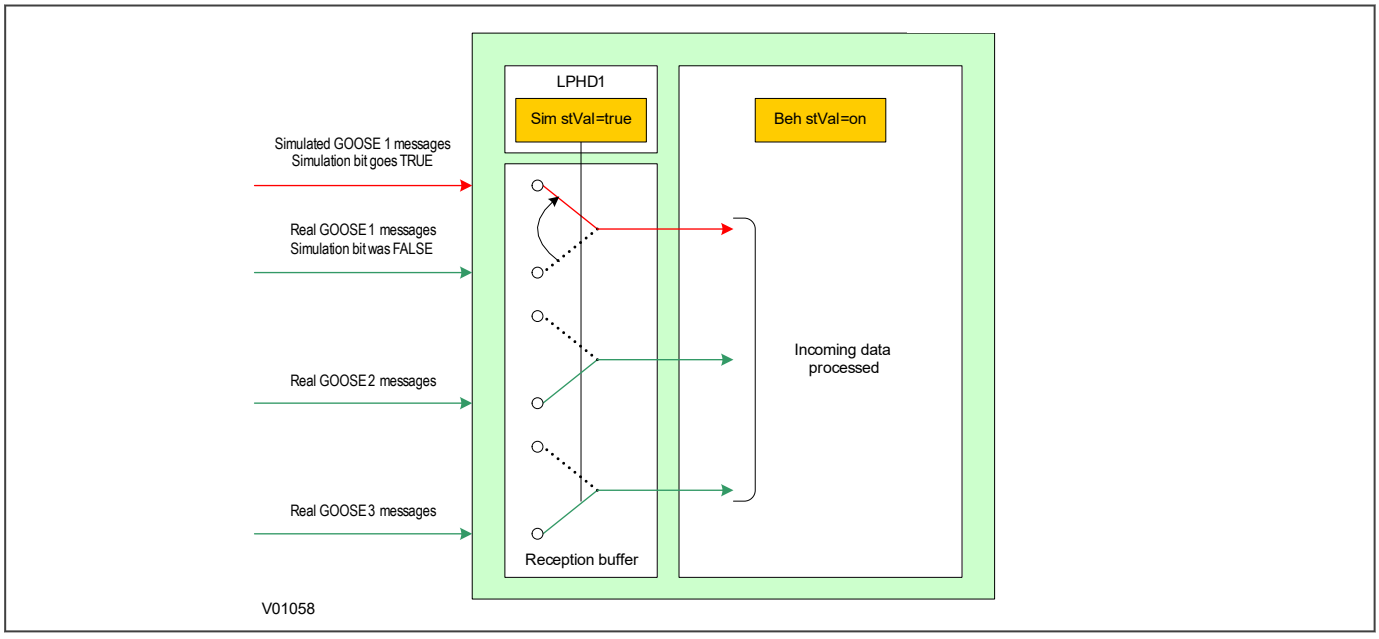


Figure 183: Simulated input behaviour

19.7.3 TESTING EXAMPLES

These examples show how you test the IED with and without simulated values. Depending on the IED Test Mode, it may respond by operating plant (for example by tripping the circuit breaker) or it may not operate plant.

19.7.3.1 TEST PROCEDURE FOR REAL VALUES

This procedure is for testing with real values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Disabled`
4. If using sampled values set the sampled values test mode
   Select *IEC 61850-9.2LE* → ***SV Test Mode*** → `Disabled`
5. Inject real signals using a test device connected to the merging units. The device will continue to listen to 'real' GOOSE messages and ignore simulated messages received.
6. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

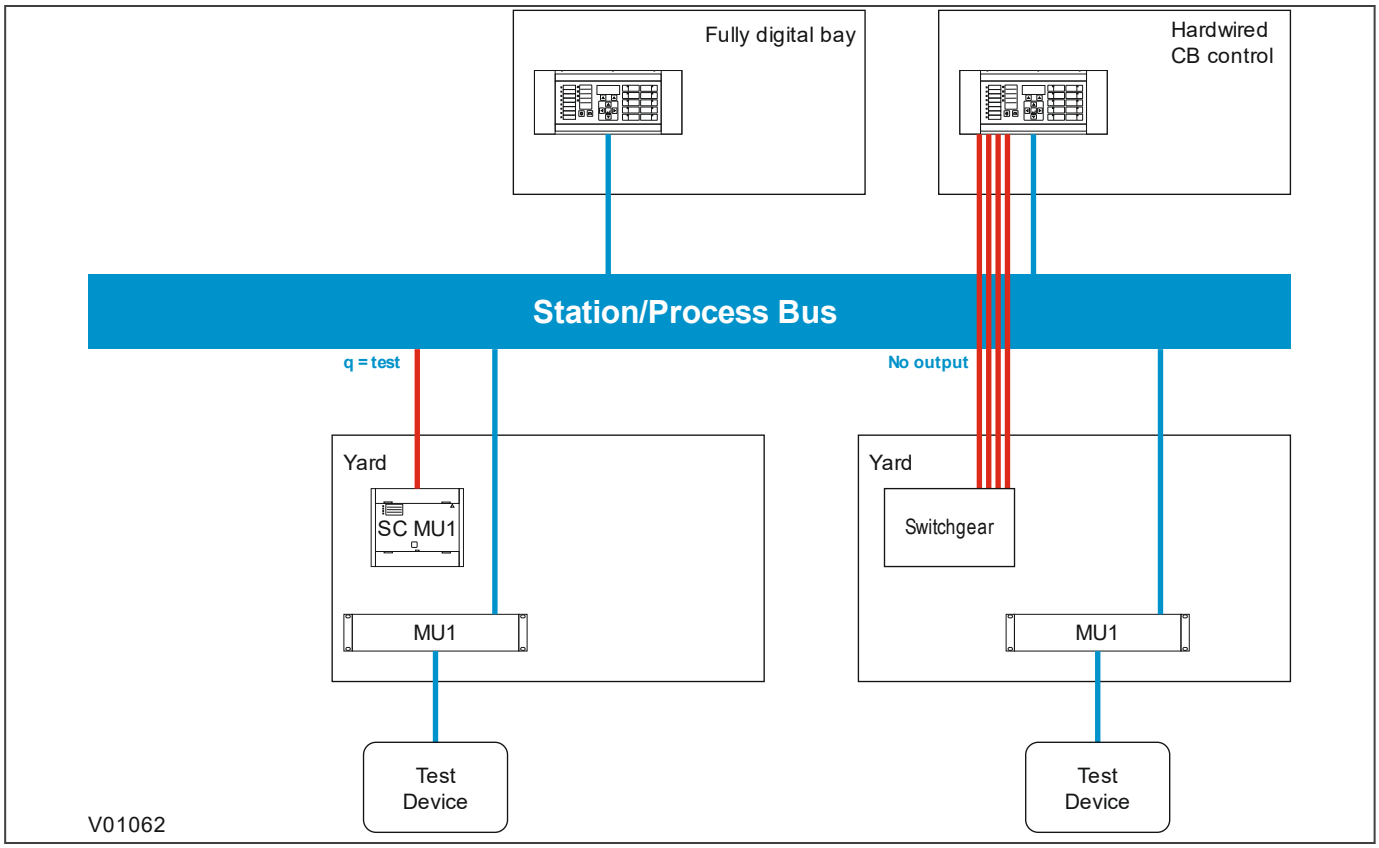


Figure 184: Test example 1

19.7.3.2 TEST PROCEDURE FOR SIMULATED VALUES - NO PLANT

This procedure is for testing with simulated values without operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Contacts Blocked`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `test-blocked`
3. Set device into Simulation Listening Mode
   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`
4. If using sampled values set the sampled values test mode
   Select *IEC 61850-9.2LE* → ***SV Test Mode*** → `Enabled`
5. Inject simulated signals using a test device connected to the Ethernet network. The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of test mode. Each message is treated separately, but sampled values are considered as a single message.
6. Verify function based on test signal outputs
   Binary outputs (e.g. CB trips) will not operate. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram

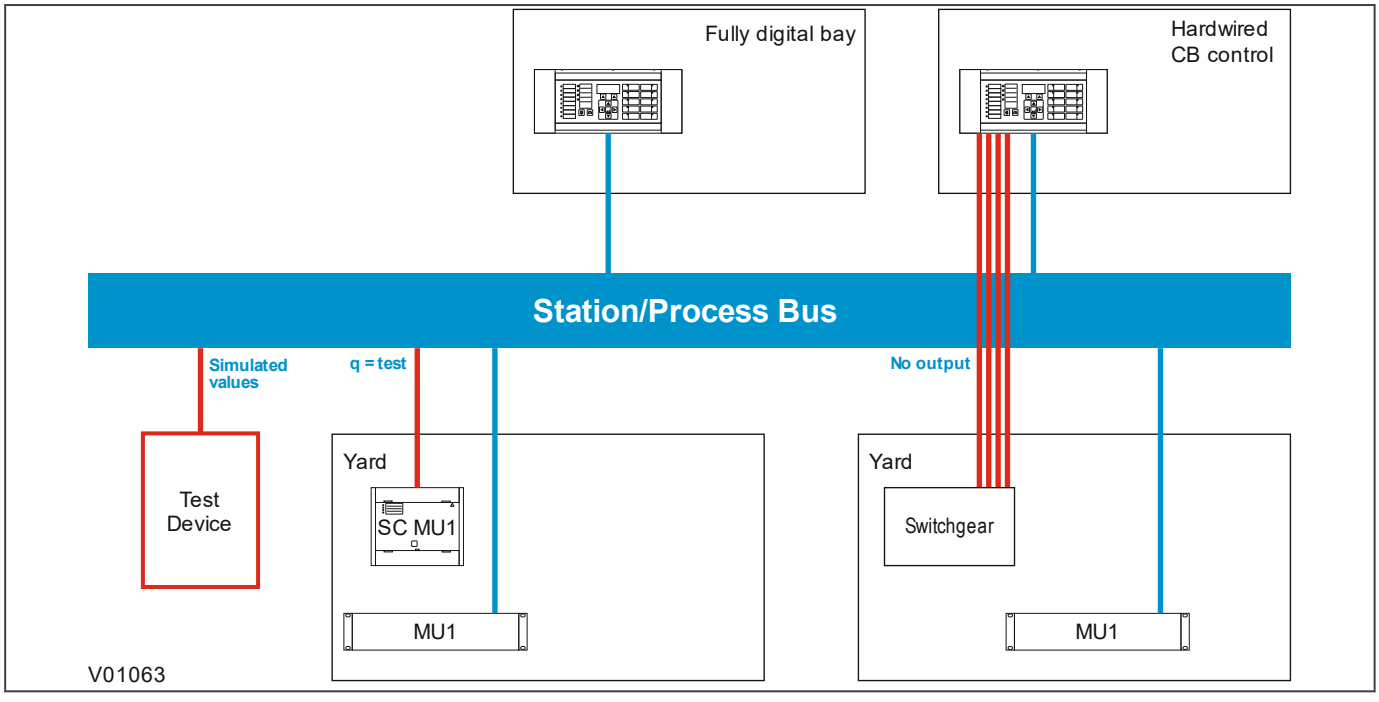


Figure 185: Test example 2

19.7.3.3 TEST PROCEDURE FOR SIMULATED VALUES - WITH PLANT

This procedure is for testing with simulated values with operating plant.

1. Set device into 'Contacts Blocked' Mode
   Select *COMMISSION TESTS* → ***IED Test Mode*** → `Test`
2. Confirm new behaviour has been enabled
   View *COMMISSION TESTS* → ***IED Mod/Beh***, and check that it shows `Test`

3. Set device into Simulation Listening Mode

   Select *COMMISSION TESTS* → ***Subscriber Sim*** = `Enabled`

4. If using sampled values set the sampled values test mode

   Select *IEC 61850-9.2LE* → ***SV Test Mode*** → `Enabled`

5. Inject simulated signals using a test device connected to the Ethernet network.

   The device will continue to listen to 'real' GOOSE messages until a simulated message is received. Once the simulated messages are received, the corresponding 'real' messages are ignored until the device is taken out of IED test mode. Each message is treated separately, but sampled values are considered as a single message.

6. Verify function based on test signal outputs.

   Binary outputs (e.g. CB trips) will operate as normal. All transmitted GOOSE and MMS data items will be tagged with the 'quality' parameter set to 'test', so that the receiver understands that they have been issued by a device under test and can respond accordingly. This is summarised in the following diagram:

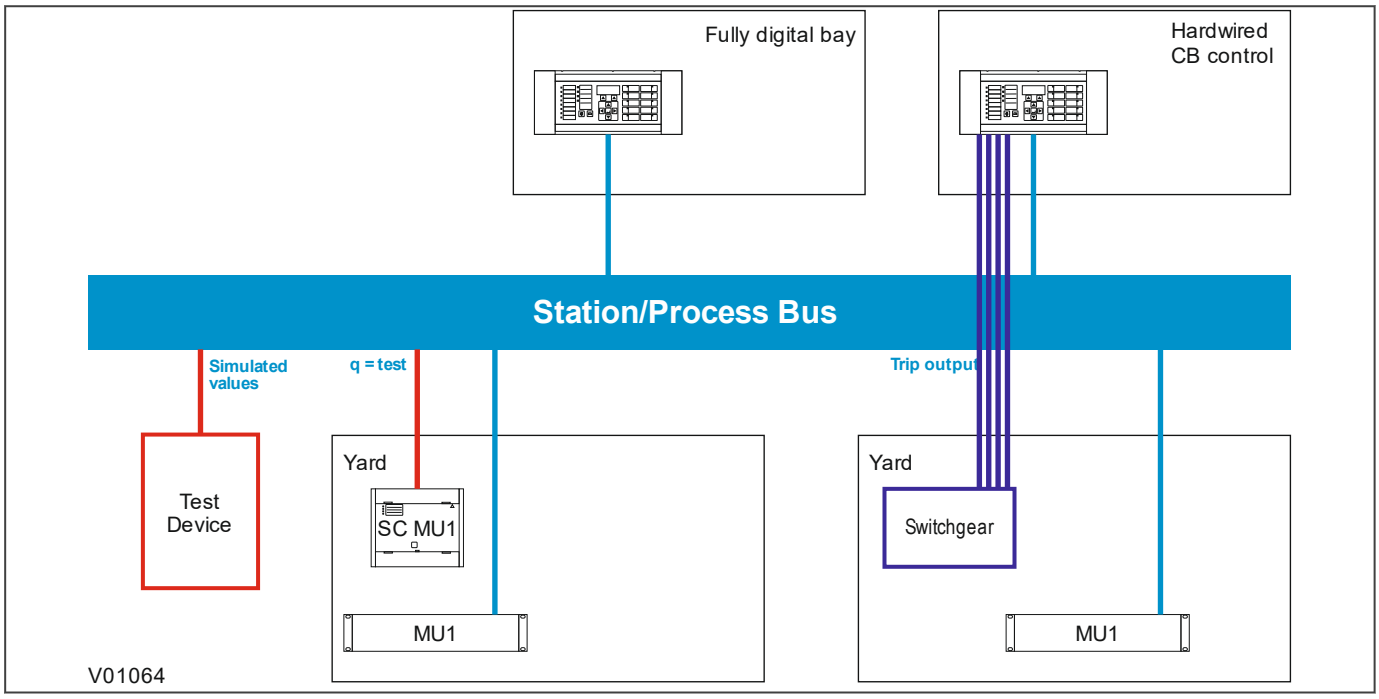


Figure 186: Test example 3

19.7.3.4 CONTACT TEST

The ***Apply Test*** command in this cell is used to change the state of the contacts set for operation.

If the device has been put into 'Contact Blocked' mode using an input signal (via the ***Block Contacts*** DDB signal) then the ***Apply Test*** command will not execute. This is to prevent a device that has been blocked by an external process having its contacts operated by a local operator using the HMI.

If the ***Block Contacts*** DDB is not set and the ***Apply Test*** command in this cell is issued, contacts change state and the command text on the LCD changes to `No Operation`. The contacts remain in the Test state until reset by issuing the ***Remove Test*** command. The command text on the LCD shows `No Operation` after the ***Remove Test*** command has been issued.

Note:
*When the **IED Test Mode** cell is set to Contacts Blocked, the **Relay O/P Status** cell does not show the current status of the output relays so cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.*

19.8 CHECKING THE DIFFERENTIAL ELEMENT

Testing of the differential element during commissioning is not necessary unless explicitly requested.

To avoid spurious operation of any other protection elements, all protection elements except the transformer differential protection should be disabled for the duration of the differential element tests. This is done in the product's *CONFIGURATION* column. Make a note of which elements need to be re-enabled after testing.

The following tests demonstrate correct operation of the differential protection. Testing should be performed on individual current inputs of each phase and on each winding, but note that the timing test should only be performed on the high voltage winding. Testing the low-set element is sufficient to test the correct operation of the differential protection.

Using a suitable current injection method, slowly increase the current from 0 Amps and note the pick-up value at which the element operates. Reduce the current slowly and note the drop-off value at which it resets. Check that the pick-up and drop-off are within the range shown in the table below.

	Current level
Pick-up	0.90 x In to 1.1 x In
Drop-off	0.90 x pick-up to 1 x pick-up

where In = Is1/(amplitude matching factor)

and Is1 is the low set setting which can be found in the ***Is1*** cell in the *DIFF PROTECTION* column.

The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. There is one amplitude matching factor for the high-voltage side, one for the low-voltage side and one for the tertiary-voltage side. You will find these in the *SYSTEM CONFIG* column. Use the appropriate amplitude matching factor to calculate the required injection current. This depends on whether it is being injected into the HV, LV, or TV current transformer inputs.

1. Whilst connected to the HV windings, connect the output contacts for the low set differential protection function to trip the test set and also to stop a timer.
2. Configure the test set so that when the current is applied, the timer starts.
3. Inject 5x In into the HV CT input.
4. Check that the element operates within the range of 30 ms to 35 ms and record the time.

Note:
If this test has been successfully performed there is no need to carry out the tests described in the protection timing checks section.

19.8.1 USING THE OMICRON ADVANCED MODULE

In software versions 05 and onwards, transient bias can be disabled or enabled. In software version 06 onwards, the CT Saturation function was separated from the No gap function.

Testing Differential Operating Characteristics

When testing the differential operating characteristic, it is important to first disable transient bias. The CT saturation and No Gap settings may be either disabled or enabled. An example is shown below:

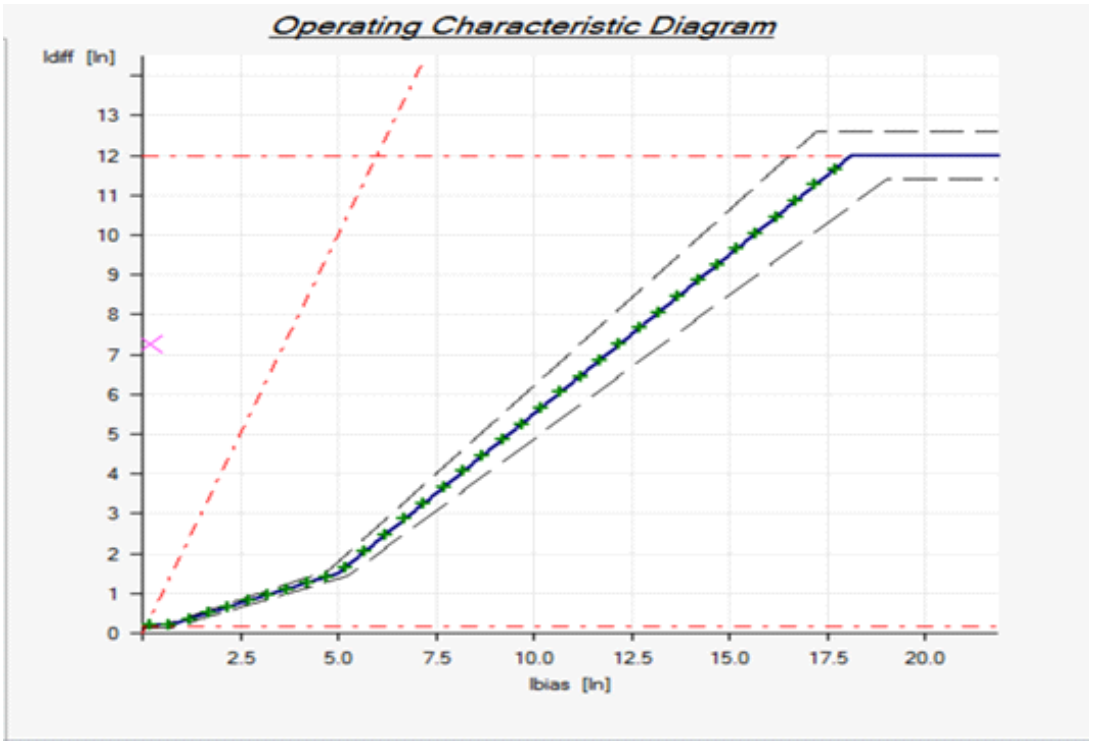


Figure 187: Operating Characteristic Diagram

Testing Differential Tripping Time Characteristics

When testing the differential tripping time characteristic, transient bias, CT saturation and No Gap settings may be either disabled or enabled. An example is shown below:

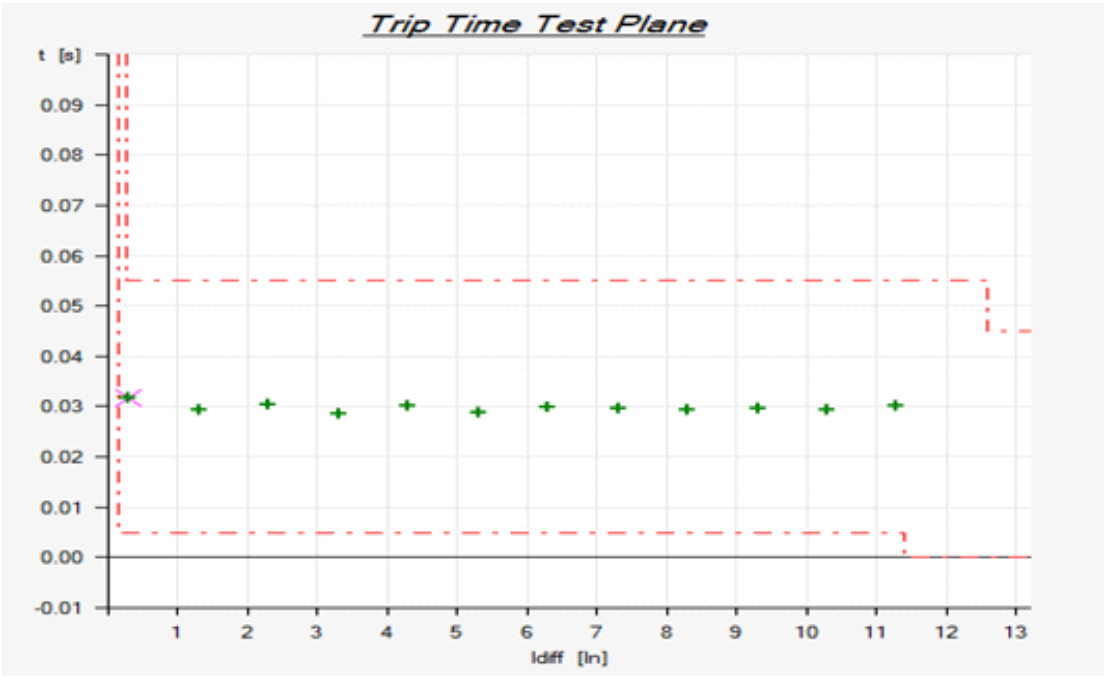


Figure 188: Trip Time Test Plane

Testing Harmonic Restraint

When testing 2nd or 5th harmonic restraint, transient bias may be either enabled or disabled, but the CT Saturation and No Gap settings must be disabled. This is because harmonic blocking is used to unblock the protection during normal energization of the transformer, while No Gap Detection and CT Saturation Detection is used to unblock the protection during an internal fault. An example is shown below:

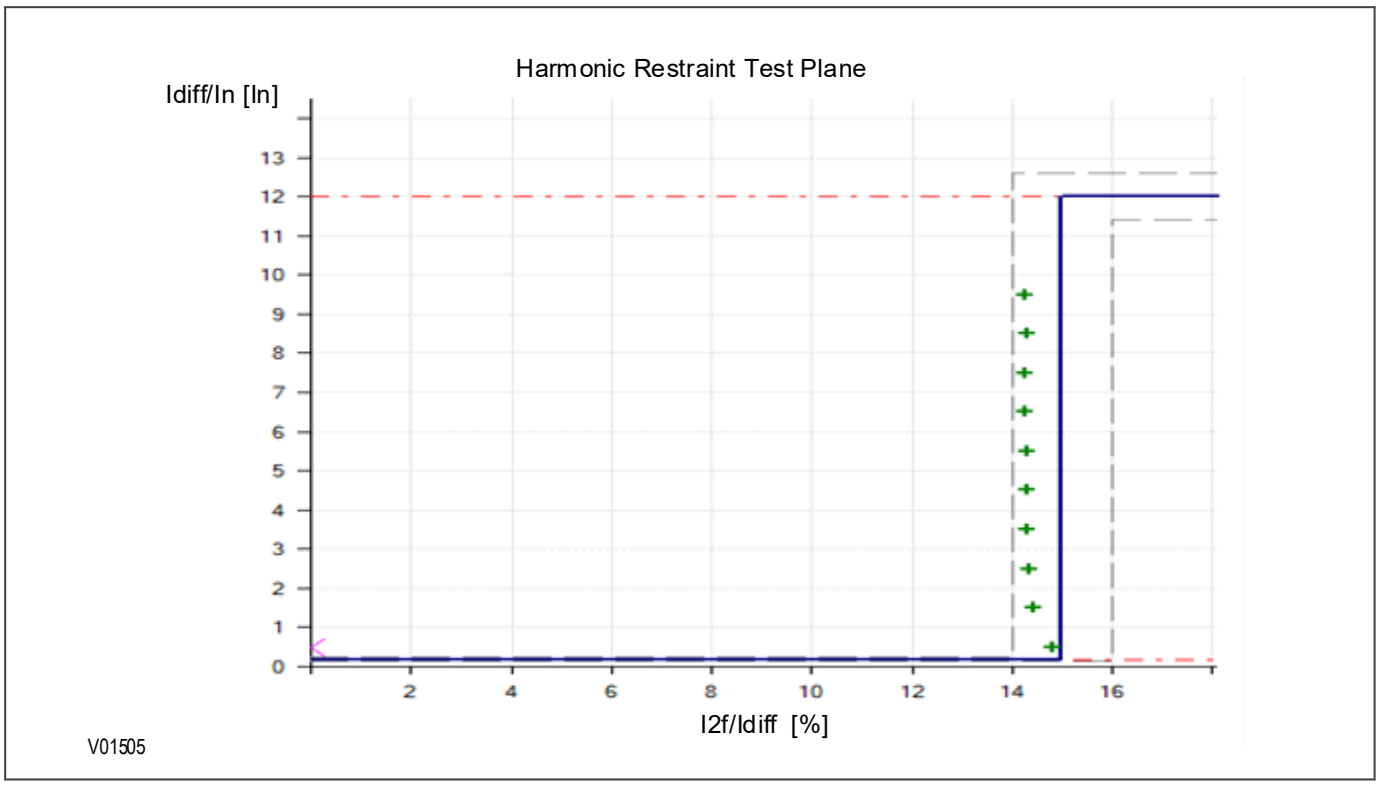


Figure 189: Harmonic Restraint Test Plane

19.9 PROTECTION TIMING CHECKS

There is no need to check every protection function. Only one protection function needs to be checked as the purpose is to verify the timing on the processor is functioning correctly.

19.9.1 BYPASSING THE ALL POLE DEAD BLOCKING CONDITION

Some protection functions and control functions are blocked when all poles are dead. When these conditions are met, an ***All Poles Dead*** signal is asserted, blocking the said conditions. If you wish to test these these elements during commissioning, you must bypass this blocking condition. You can do this by modifying the default PSL, placing a NOT gate between the ***CB1 Closed*** signal and opto-input 7, so that when this input is not energised, CB1 is assumed to be closed.

19.9.2 OVERCURRENT CHECK

If the overcurrent protection function is being used, test the overcurrent protection for stage 1.

1. Check for any possible dependency conditions and simulate as appropriate.
2. In the *CONFIGURATION* column, disable all protection elements other than the one being tested.
3. Make a note of which elements need to be re-enabled after testing.
4. Connect the test circuit.
5. Perform the test.
6. Check the operating time.

19.9.3 CONNECTING THE TEST CIRCUIT

1. Use the PSL to determine which output relay will operate when an overcurrent trip occurs.
2. Use the output relay assigned to ***Trip Output A***.
3. Use the PSL to map the protection stage under test directly to an output relay.

> *Note:*
> *If using the default PSL, use output relay 3 as this is already mapped to the DDB signal **Trip Command Out**.*

4. Connect the output relay so that its operation will trip the test set and stop the timer.
5. Connect the current output of the test set to the A-phase current transformer input.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column is set to `Directional Fwd`, the current should flow out of terminal 2. If set to `Directional Rev`, it should flow into terminal 2.

   If the ***I>1 Directional*** cell in the *OVERCURRENT* column has been set to `Directional Fwd` or `Directional Rev`, the rated voltage should be applied to terminals 20 and 21.
6. Ensure that the timer starts when the current is applied.

> *Note:*
> *If the timer does not stop when the current is applied and stage 1 has been set for directional operation, the connections may be incorrect for the direction of operation set. Try again with the current connections reversed.*

19.9.4 PERFORMING THE TEST

1. Ensure that the timer is reset.
2. Apply a current of twice the setting shown in the ***I>1 Current Set*** cell in the *OVERCURRENT* column.
3. Note the time displayed when the timer stops.
4. Check that the red trip LED has illuminated.

19.9.5 CHECK THE OPERATING TIME

Check that the operating time recorded by the timer is within the range shown below.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	Operating Time at Twice Current Setting and Time Multiplier/Time Dial Setting of 1.0	
	Nominal (seconds)	Range (seconds)
DT	I>1 Time Delay setting	Setting ±2%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	24.67 - 28.67
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 4.0
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.50	9.02 - 9.97
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Note:
With the exception of the definite time characteristic, the operating times given are for a Time Multiplier Setting (TMS) or Time Dial Setting (TDS) of 1. For other values of TMS or TDS, the values need to be modified accordingly.
For definite time and inverse characteristics there is an additional delay of up to 0.02 second and 0.08 second respectively. You may need to add this the IED's acceptable range of operating times.

Caution:
On completion of the tests, you must restore all settings to customer specifications.

19.10 ONLOAD CHECKS

Warning:
Onload checks are potentially very dangerous and may only be carried out by qualified and authorised personnel.

Onload checks can only be carried out if there are no restrictions preventing the energisation of the plant, and the other devices in the group have already been commissioned.

Remove all test leads and temporary shorting links, then replace any external wiring that has been removed to allow testing.

Warning:
If any external wiring has been disconnected for the commissioning process, replace it in accordance with the relevant external connection or scheme diagram.

19.10.1 CONFIRM CURRENT CONNECTIONS

1. Measure the current transformer secondary values for each input either by:
   a. reading from the device's HMI panel (providing it has first been verified by a secondary injection test)
   b. using a current clamp meter
2. Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control centre.
3. Ensure the current flowing in the neutral circuit of the current transformers is negligible.

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

19.10.2 CONFIRM VOLTAGE CONNECTIONS

1. Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated.
2. Check that the system phase rotation is correct using a phase rotation meter.
3. Compare the values of the secondary phase voltages with the measured voltage magnitude values, which can be found in the *MEASUREMENTS 1* menu column.

Cell in MEASUREMENTS 1 Column	Corresponding VT Ratio in CT/VT RATIOS Column
VAB MAGNITUDE *VBC MAGNITUDE* *VCA MAGNITUDE* *VAN MAGNITUDE* *VBN MAGNITUDE* *VCN MAGNITUDE*	Main VT Primary / Main VT Sec'y

If the ***Local Values*** cell is set to `Secondary`, the values displayed should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If the ***Local Values*** cell is set to `Primary`, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the *CT & VT RATIOS* column. The values should be within 1% of the expected values, plus an additional allowance for the accuracy of the test equipment being used.

19.10.3 ON-LOAD DIRECTIONAL TEST

This test ensures that directional overcurrent and fault locator functions have the correct forward/reverse response to fault and load conditions. For this test you must first know the actual direction of power flow on the system. If you do not already know this you must determine it using adjacent instrumentation or protection already in-service.

- For load current flowing in the Forward direction (power export to the remote line end), the cells ***A Phase Watts HV, A Phase Watts LV*** , and ***A Phase Watts TV*** in the *MEASUREMENTS 2* column should show positive power signing.
- For load current flowing in the Reverse direction (power import from the remote line end), the cells ***A Phase Watts LV*** in the *MEASUREMENTS 2* column should show negative power signing.

Note:
*This check applies only for Measurement Modes 0 (default), and 2. This should be checked in the MEASURE'T. SETUP column (**Measurement Mode** = 0 or 2). If measurement modes 1 or 3 are used, the expected power flow signing would be opposite to that shown above.*

In the event of any uncertainty, check the phase angle of the phase currents with respect to their phase voltage.

19.11 FINAL CHECKS

1. Remove all test leads and temporary shorting leads.
2. If you have had to disconnect any of the external wiring in order to perform the wiring verification tests, replace all wiring, fuses and links in accordance with the relevant external connection or scheme diagram.
3. The settings applied should be carefully checked against the required application-specific settings to ensure that they are correct, and have not been mistakenly altered during testing.
4. Ensure that all protection elements required have been set to `Enabled` in the *CONFIGURATION* column.
5. Ensure that the IED has been restored to service by checking that the ***Test Mode*** cell in the *COMMISSION TESTS* column is set to `Disabled`.
6. If the IED is in a new installation or the circuit breaker has just been maintained, the circuit breaker maintenance and current counters should be zero. These counters can be reset using the ***Reset All Values*** cell. If the required access level is not active, the device will prompt for a password to be entered so that the setting change can be made.
7. If the menu language has been changed to allow accurate testing it should be restored to the customer's preferred language.
8. If a P991/MMLG test block is installed, remove the P992/MMLB test plug and replace the cover so that the protection is put into service.
9. Ensure that all event records, fault records, disturbance records, alarms and LEDs and communications statistics have been reset.

> *Note:*
> *Remember to restore the language setting to the customer's preferred language on completion.*

CHAPTER 20

MAINTENANCE AND TROUBLESHOOTING

20.1 CHAPTER OVERVIEW

The Maintenance and Troubleshooting chapter provides details of how to maintain and troubleshoot products based on the Px4x and P40Agile platforms. Always follow the warning signs in this chapter. Failure to do so may result injury or defective equipment.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

The troubleshooting part of the chapter allows an error condition on the IED to be identified so that appropriate corrective action can be taken.

If the device develops a fault, it is usually possible to identify which module needs replacing. It is not possible to perform an on-site repair to a faulty module.

If you return a faulty unit or module to the manufacturer or one of their approved service centres, you should include a completed copy of the Repair or Modification Return Authorization (RMA) form.

This chapter contains the following sections:

Chapter Overview 480

Maintenance 481

Troubleshooting 489

20.2 MAINTENANCE

20.2.1 MAINTENANCE CHECKS

In view of the critical nature of the application, GE Vernova products should be checked at regular intervals to confirm they are operating correctly. GE Vernova products are designed for a life in excess of 20 years.

The devices are self-supervising and so require less maintenance than earlier designs of protection devices. Most problems will result in an alarm, indicating that remedial action should be taken. However, some periodic tests should be carried out to ensure that they are functioning correctly and that the external wiring is intact. It is the responsibility of the customer to define the interval between maintenance periods. If your organisation has a Preventative Maintenance Policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

Although some functionality checks can be performed from a remote location, these are predominantly restricted to checking that the unit is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. For this reason, maintenance checks should also be performed locally at the substation.

Caution:
Before carrying out any work on the equipment you should be familiar with the contents of the Safety Section or the Safety Guide SFTY/4LM and the ratings on the equipment's rating label.

20.2.1.1 ALARMS

First check the alarm status LED to see if any alarm conditions exist. If so, press the Read key repeatedly to step through the alarms.

After dealing with any problems, clear the alarms. This will clear the relevant LEDs.

20.2.1.2 OPTO-ISOLATORS

Check the opto-inputs by repeating the commissioning test detailed in the Commissioning chapter.

20.2.1.3 OUTPUT RELAYS

Check the output relays by repeating the commissioning test detailed in the Commissioning chapter.

20.2.1.4 MEASUREMENT ACCURACY

If the power system is energised, the measured values can be compared with known system values to check that they are in the expected range. If they are within a set range, this indicates that the A/D conversion and the calculations are being performed correctly. Suitable test methods can be found in Commissioning chapter.

Alternatively, the measured values can be checked against known values injected into the device using the test block, (if fitted) or injected directly into the device's terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

20.2.2 REPLACING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, you can replace either the complete device or just the faulty PCB, identified by the in-built diagnostic software.

If possible you should replace the complete device, as this reduces the chance of damage due to electrostatic discharge and also eliminates the risk of fitting an incompatible replacement PCB. However, we understand it may be difficult to remove an installed product and you may be forced to replace the faulty PCB on-site. The case and rear terminal blocks are designed to allow removal of the complete device, without disconnecting the scheme wiring.

Caution:
Replacing PCBs requires the correct on-site environment (clean and dry) as well as suitably trained personnel.

Caution:
If the repair is not performed by an approved service centre, the warranty will be invalidated.

Caution:
Before carrying out any work on the equipment, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label. This should ensure that no damage is caused by incorrect handling of the electronic components.

Warning:
Before working at the rear of the device, isolate all voltage and current supplying it.

Note:
The current transformer inputs are equipped with integral shorting switches which will close for safety reasons, when the terminal block is removed.

To replace the complete device:

1. Carefully disconnect the cables not connected to the terminal blocks (e.g. IRIG-B, fibre optic cables, earth), as appropriate, from the rear of the device.
2. Remove the terminal block screws using a magnetic screwdriver to minimise the risk of losing the screws or leaving them in the terminal block.
3. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
4. Remove the terminal block screws that fasten the device to the panel and rack. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.
5. Withdraw the device from the panel and rack. Take care, as the device will be heavy due to the internal transformers.
6. To reinstall the device, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the chassis ground, IRIG-B and fibre optic connections are replaced. The terminal blocks are labelled alphabetically with 'A' on the left hand side when viewed from the rear.

Once the device has been reinstalled, it should be re-commissioned as set out in the Commissioning chapter.

Caution:
If the top and bottom access covers have been removed, some more screws with smaller diameter heads are made accessible. Do NOT remove these screws, as they secure the front panel to the device.

Note:
There are four possible types of terminal block: RTD/CLIO input, heavy duty, medium duty, and MiDOS. The terminal blocks are fastened to the rear panel with slotted or cross-head screws depending on the type of terminal block. Not all terminal block types are present on all products.

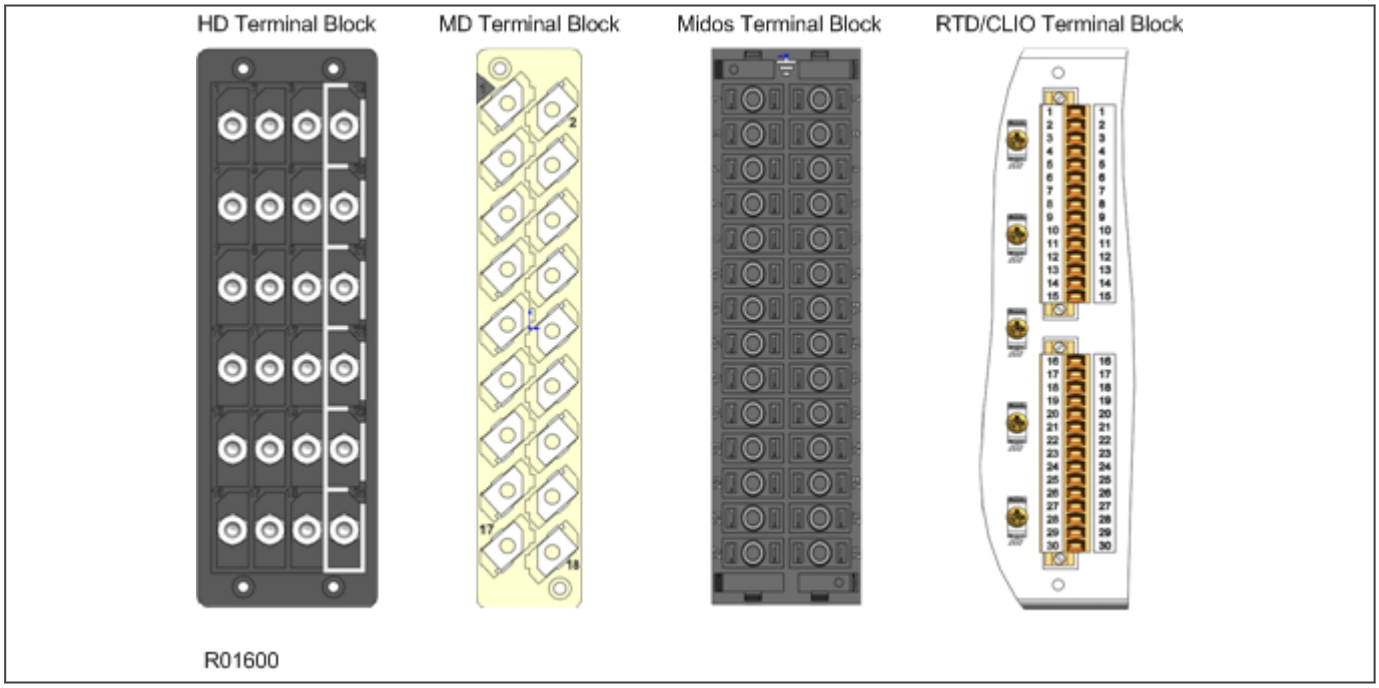


Figure 190: Possible terminal block types

20.2.3 REPAIRING THE DEVICE

If your product should develop a fault while in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. In the case of a fault, either the complete unit or just the faulty PCB, identified by the in-built diagnostic software, should be replaced.

Replacement of printed circuit boards and other internal components must be undertaken by approved Service Centres. Failure to obtain the authorization of after-sales engineers prior to commencing work may invalidate the product warranty.

We recommend that you entrust any repairs to Automation Support teams, which are available world-wide.

20.2.4 REMOVING THE FRONT PANEL

Warning:
Before removing the front panel to replace a PCB, you must first remove the auxiliary power supply and wait 5 seconds for the internal capacitors to discharge. You should also isolate voltage and current transformer connections and trip circuit.

Caution:
Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

To remove the front panel:

1. Open the top and bottom access covers. You must open the hinged access covers by more than 90° before they can be removed.
2. If fitted, remove the transparent secondary front cover.
3. Apply outward pressure to the middle of the access covers to bow them and disengage the hinge lug, so the access cover can be removed. The screws that fasten the front panel to the case are now accessible.
4. Undo and remove the screws. The 40TE case has four cross-head screws fastening the front panel to the case, one in each corner, in recessed holes. The 60TE/80TE cases have an additional two screws, one midway along each of the top and bottom edges of the front plate.
5. When the screws have been removed, pull the complete front panel forward to separate it from the metal case. The front panel is connected to the rest of the circuitry by a 64-way ribbon cable.
6. The ribbon cable is fastened to the front panel using an IDC connector; a socket on the cable and a plug with locking latches on the front panel. Gently push the two locking latches outwards which eject the connector socket slightly. Remove the socket from the plug to disconnect the front panel.

Caution:
Do not remove the screws with the larger diameter heads which are accessible when the access covers are fitted and open. These screws hold the relay in its mounting (panel or cubicle).

Caution:
The internal circuitry is now exposed and is not protected against electrostatic discharge and dust ingress. Therefore ESD precautions and clean working conditions must be maintained at all times.

20.2.5 REPLACING PCBS

1. To replace any of the PCBs, first remove the front panel.
2. Once the front panel has been removed, the PCBs are accessible. The numbers above the case outline identify the guide slot reference for each printed circuit board. Each printed circuit board has a label stating the corresponding guide slot number to ensure correct relocation after removal. To serve as a reminder of the slot numbering there is a label on the rear of the front panel metallic screen.
3. Remove the 64-way ribbon cable from the PCB that needs replacing
4. Remove the PCB in accordance with the board-specific instructions detailed later in this section.

Note:
To ensure compatibility, always replace a faulty PCB with one of an identical part number.

20.2.5.1 REPLACING THE MAIN PROCESSOR BOARD

The main processor board is situated in the front panel. This board contains application-specific settings in its non-volatile memory. You may wish to take a backup copy of these settings. This could save time in the re-commissioning process.

To replace the main processor board:

1. Remove front panel.
2. Place the front panel with the user interface face down and remove the six screws from the metallic screen, as shown in the figure below. Remove the metal plate.
3. Remove the screws that hold the main processor board in position.
4. Carefully disconnect the ribbon cable. Take care as this could easily be damaged by excessive twisting.
5. Replace the main processor board
6. Reassemble the front panel using the reverse procedure. Make sure the ribbon cable is reconnected to the main processor board and that all eight screws are refitted.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, carry out the standard commissioning procedure as defined in the Commissioning chapter.

Note:
After replacing the main processor board, all the settings required for the application need to be re-entered. This may be done either manually or by downloading a settings file.

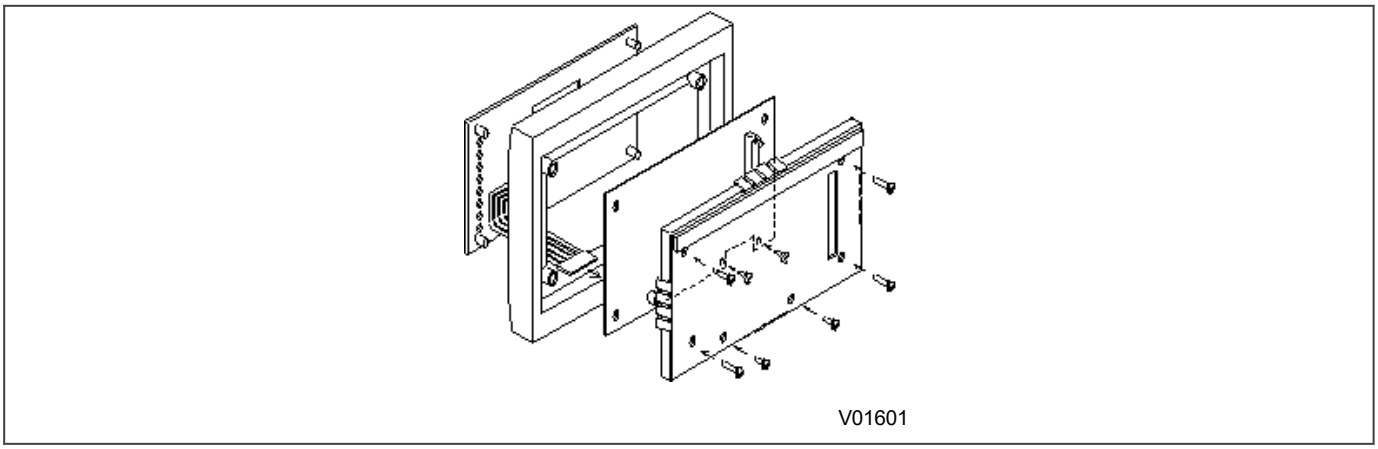


Figure 191: Front panel assembly

20.2.5.2 REPLACEMENT OF COMMUNICATIONS BOARDS

Most products will have at least one communications board of some sort fitted. There are several different boards available offering various functionality, depending on the application. Some products may even be fitted with two boards of different types.

To replace a faulty communications board:

1. Remove front panel.
2. Disconnect all connections at the rear.
3. The board is secured in the relay case by two screws, one at the top and another at the bottom. Remove these screws carefully as they are not captive in the rear panel.
4. Gently pull the communications board forward and out of the case.
5. Before fitting the replacement PCB check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.

6. Fit the replacement PCB carefully into the correct slot. Make sure it is pushed fully back and that the securing screws are refitted.
7. Reconnect all connections at the rear.
8. Refit the front panel.
9. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
10. Once the unit has been reassembled, commission it according to the Commissioning chapter.

20.2.5.3 REPLACEMENT OF THE INPUT MODULE

Depending on the product, the input module consists of two or three boards fastened together and is contained within a metal housing. One board contains the transformers and one contains the analogue to digital conversion and processing electronics. Some devices have an additional auxiliary transformer contained on a third board.

To replace an input module:

1. Remove front panel.
2. The module is secured in the case by two screws on its right-hand side, accessible from the front, as shown below. Move these screws carefully as they are not captive in the front plate of the module.
3. On the right-hand side of the module there is a small metal tab which brings out a handle (on some modules there is also a tab on the left). Grasp the handle(s) and pull the module firmly forward, away from the rear terminal blocks. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
4. Remove the module from the case. The module may be heavy, because it contains the input voltage and current transformers.
5. Slot in the replacement module and push it fully back onto the rear terminal blocks. To check that the module is fully inserted, make sure the v-shaped cut-out in the bottom plate of the case is fully visible.
6. Refit the securing screws.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

Caution:
With non-mounted IEDs, the case needs to be held firmly while the module is withdrawn. Withdraw the input module with care as it suddenly comes loose once the friction of the terminal blocks is overcome.

Note:
If individual boards within the input module are replaced, recalibration will be necessary. We therefore recommend replacement of the complete module to avoid on-site recalibration.

20.2.5.4 REPLACEMENT OF THE POWER SUPPLY BOARD

Caution:
Before removing the front panel, you should be familiar with the contents of the Safety Information section of this guide or the Safety Guide SFTY/4LM, as well as the ratings on the equipment's rating label.

The power supply board is fastened to an output relay board with push fit nylon pillars. This doubled-up board is secured on the extreme left hand side, looking from the front of the unit.

1. Remove front panel.
2. Pull the power supply module forward, away from the rear terminal blocks and out of the case. A reasonable amount of force is needed due to the friction between the contacts of the terminal blocks.
3. Separate the boards by pulling them apart carefully. The power supply board is the one with two large electrolytic capacitors.
4. Before reassembling the module, check that the number on the round label next to the front edge of the PCB matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label
5. Reassemble the module with a replacement PCB. Push the inter-board connectors firmly together. Fit the four push fit nylon pillars securely in their respective holes in each PCB.
6. Slot the power supply module back into the housing. Push it fully back onto the rear terminal blocks.
7. Refit the front panel.
8. Refit and close the access covers then press the hinge assistance T-pieces so they click back into the front panel moulding.
9. Once the unit has been reassembled, commission it according to the Commissioning chapter.

20.2.5.5 REPLACEMENT OF THE I/O BOARDS

There are several different types of I/O boards, which can be used, depending on the product and application. Some boards have opto-inputs, some have relay outputs and others have a mixture of both.

1. Remove front panel.
2. Gently pull the board forward and out of the case
3. If replacing the I/O board, make sure the setting of the link above IDC connector on the replacement board is the same as the one being replaced.
4. Before fitting the replacement board check the number on the round label next to the front edge of the board matches the slot number into which it will be fitted. If the slot number is missing or incorrect, write the correct slot number on the label.
5. Carefully slide the replacement board into the appropriate slot, ensuring that it is pushed fully back onto the rear terminal blocks.
6. Refit the front panel.
7. Refit and close the access covers then press at the hinge assistance T-pieces so they click back into the front panel moulding.
8. Once the unit has been reassembled, commission it according to the Commissioning chapter.

20.2.6 RECALIBRATION

Recalibration is not needed when a PCB is replaced, unless it is one of the boards in the input module. If any of the boards in the input module is replaced, the unit must be recalibrated.

Although recalibration is needed when a board inside the input module is replaced, it is not needed if the input module is replaced in its entirety.

Although it is possible to carry out recalibration on site, this requires special test equipment and software. We therefore recommend that the work be carried out by the manufacturer, or entrusted to an approved service centre.

20.2.7 SUPERCAPACITOR DISCHARGED

The supercapacitor maintains charge for two weeks with the IED de-energised. When first energising the IED after this time there may be a ***SuperCap Alarm*** due to the supercapacitor voltage dropping below a pre-defined

threshold. The ***SuperCap Alarm*** will clear after approximately 30 minutes of IED being energised, and once cleared there will be enough charge in the supercapacitor to maintain the RTC.

Note:
The Real Time Clock will be reset if the supercapacitor is fully discharged.

20.2.8 CLEANING

Warning:
Before cleaning the device, ensure that all AC and DC supplies and transformer connections are isolated, to prevent any chance of an electric shock while cleaning.

Only clean the equipment with a lint-free cloth dampened with clean water. Do not use detergents, solvents or abrasive cleaners as they may damage the product's surfaces and leave a conductive residue.

20.3 TROUBLESHOOTING

20.3.1 SELF-DIAGNOSTIC SOFTWARE

The device includes several self-monitoring functions to check the operation of its hardware and software while in service. If there is a problem with the hardware or software, it should be able to detect and report the problem, and attempt to resolve the problem by performing a reboot. In this case, the device would be out of service for a short time, during which the 'Healthy' LED on the front of the device is switched OFF and the watchdog contact at the rear is ON. If the restart fails to resolve the problem, the unit takes itself permanently out of service; the 'Healthy' LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the device attempts to store a maintenance record to allow the nature of the problem to be communicated to the user.

The self-monitoring is implemented in two stages: firstly a thorough diagnostic check which is performed on boot-up, and secondly a continuous self-checking operation, which checks the operation of the critical functions whilst it is in service.

20.3.2 POWER-UP ERRORS

If the IED does not appear to power up, use the following to determine whether the fault is in the external wiring, auxiliary fuse, IED power supply module or IED front panel.

Test	Check	Action
1	Measure the auxiliary voltage on terminals 1 and 2. Verify the voltage level and polarity against the rating label on the front. Terminal 1 is –dc, 2 is +dc	If the auxiliary voltage is correct, go to test 2. Otherwise check the wiring and fuses in the auxiliary supply.
2	Check the LEDs and LCD backlight switch on at power-up. Also check the N/O (normally open) watchdog contact for closing.	If the LEDs and LCD backlight switch on, or the contact closes and no error code is displayed, the error is probably on the main processor board in the front panel. If the LEDs and LCD backlight do not switch on and the contact does not close, go to test 3.
3	Check the output (nominally 48 V DC).	If there is no field voltage, the fault is probably in the IED power supply module.

20.3.3 ERROR MESSAGE OR CODE ON POWER-UP

The IED performs a self-test during power-up. If it detects an error, a message appears on the LCD and the power-up sequence stops. If the error occurs when the IED application software is running, a maintenance record is created and the device reboots.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If the IED locks up and displays an error code permanently, go to test 2. If the IED prompts for user input, go to test 4. If the IED reboots automatically, go to test 5.
2	Record displayed error, and then remove and re-apply IED auxiliary supply.	Record whether the same error code is displayed when the IED is rebooted. If no error code is displayed, contact the local service centre stating the error code and IED information. If the same code is displayed, go to test 3.

Test	Check	Action
3	Error Code Identification The following text messages (in English) are displayed if a fundamental problem is detected, preventing the system from booting: Bus Fail – address lines SRAM Fail – data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail The following hex error codes relate to errors detected in specific IED modules:	These messages indicate that a problem has been detected on the IED's main processor board in the front panel.
3.1	0c140005/0c0d0000	Input Module (including opto-isolated inputs)
3.2	0c140006/0c0e0000	Output IED boards
3.3	The last four digits provide details on the actual error.	Other error codes relate to hardware or software problems on the main processor board. Contact General Electric with details of the problem for a full analysis.
4	The IED displays a message for corrupt settings and prompts for the default values to be restored for the affected settings.	The power-up tests have detected corrupted IED settings. Restore the default settings to allow the power-up to complete, and then reapply the application-specific settings.
5	The IED resets when the power-up is complete. A record error code is displayed	Error 0x0E080000, programmable scheme logic error due to excessive execution time. If the IED powers up successfully, check the programmable logic for feedback paths. Other error codes relate to software errors on the main processor board.

20.3.4 OUT OF SERVICE LED ON AT POWER-UP

Test	Check	Action	
1	Using the IED menu, confirm the Commission Test or Test Mode setting is Enabled. If it is not Enabled, go to test 2.	If the setting is Enabled, disable the test mode and make sure the Out of Service LED is OFF.	
2	Select the *VIEW RECORDS* column then view the last maintenance record from the menu.	Check for the H/W Verify Fail maintenance record. This indicates a discrepancy between the IED model number and the hardware. Examine the ***Maint Data***; cell. This indicates the causes of the failure using bit fields: Bit Meaning	
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID

Test	Check	Action	
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110 V VTs fitted)
		7	The VT type field in the model number is incorrect (440 V VTs fitted)
		8	The VT type field in the model number is incorrect (no VTs fitted)

20.3.5 ERROR CODE DURING OPERATION

The IED performs continuous self-checking. If the IED detects an error it displays an error message, logs a maintenance record and after a short delay resets itself. A permanent problem (for example due to a hardware fault) is usually detected in the power-up sequence. In this case the IED displays an error code and halts. If the problem was transient, the IED reboots correctly and continues operation. By examining the maintenance record logged, the nature of the detected fault can be determined.

20.3.6 MAL-OPERATION DURING TESTING

20.3.6.1 FAILURE OF OUTPUT CONTACTS

An apparent failure of the relay output contacts can be caused by the configuration. Perform the following tests to identify the real cause of the failure. The self-tests verify that the coils of the output relay contacts have been energized. An error is displayed if there is a fault in the output relay board.

Test	Check	Action
1	Is the Out of Service LED ON?	If this LED is ON, the relay may be in test mode or the protection has been disabled due to a hardware verify error.
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, go to test 4; if not, go to test 3.
3	Examine the fault record or use the test port to check the protection element is operating correctly.	If the protection element does not operate, check the test is correctly applied. If the protection element operates, check the programmable logic to make sure the protection element is correctly mapped to the contacts.
4	Using the Commissioning or Test mode function, apply a test pattern to the relevant relay output contacts. Consult the correct external connection diagram and use a continuity tester at the rear of the relay to check the relay output contacts operate.	If the output relay operates, the problem must be in the external wiring to the relay. If the output relay does not operate the output relay contacts may have failed (the self-tests verify that the relay coil is being energized). Ensure the closed resistance is not too high for the continuity tester to detect.

20.3.6.2 FAILURE OF OPTO-INPUTS

The opto-isolated inputs are mapped onto the IED's internal DDB signals using the programmable scheme logic. If an input is not recognised by the scheme logic, use the ***Opto I/P Status*** cell in the *COMMISSION TESTS* column to check whether the problem is in the opto-input itself, or the mapping of its signal to the scheme logic functions.

If the device does not correctly read the opto-input state, test the applied signal. Verify the connections to the opto-input using the wiring diagram and the nominal voltage settings in the *OPTO CONFIG* column. To do this:

1. Select the nominal voltage for all opto-inputs by selecting one of the five standard ratings in the ***Global Nominal V*** cell.
2. Select `Custom` to set each opto-input individually to a nominal voltage.
3. Using a voltmeter, check that the voltage on its input terminals is greater than the minimum pick-up level (See the Technical Specifications chapter for opto pick-up levels).

If the signal is correctly applied, this indicates failure of an opto-input, which may be situated on standalone opto-input board, or on an opto-input board that is part of the input module. Separate opto-input boards can simply be replaced. If, however, the faulty opto-input board is part of the input module, the complete input module should be replaced. This is because the analogue input module cannot be individually replaced without dismantling the module and recalibration of the IED.

20.3.6.3 INCORRECT ANALOGUE SIGNALS

If the measured analogue quantities do not seem correct, use the measurement function to determine the type of problem. The measurements can be configured in primary or secondary terms.

1. Compare the displayed measured values with the actual magnitudes at the terminals.
2. Check the correct terminals are used.
3. Check the CT and VT ratios set are correct.
4. Check the phase displacement to confirm the inputs are correctly connected.

20.3.7 PSL EDITOR TROUBLESHOOTING

A failure to open a connection could be due to one or more of the following:

- The IED address is not valid (this address is always 1 for the front port)
- Password in not valid
- Communication set-up (COM port, Baud rate, or Framing) is not correct
- Transaction values are not suitable for the IED or the type of connection
- The connection cable is not wired correctly or broken
- The option switches on any protocol converter used may be incorrectly set

20.3.7.1 DIAGRAM RECONSTRUCTION

Although a scheme can be extracted from an IED, a facility is provided to recover a scheme if the original file is unobtainable.

A recovered scheme is logically correct but much of the original graphical information is lost. Many signals are drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B. Any annotation added to the original diagram such as titles and notes are lost.

Sometimes a gate type does not appear as expected. For example, a single-input AND gate in the original scheme appears as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 also appear as OR gates

20.3.7.2 PSL VERSION CHECK

The PSL is saved with a version reference, time stamp and CRC check (Cyclic Redundancy Check). This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

20.3.8 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Return Authorization (RMA) form
   An electronic version of the RMA form is available from the following:
   contact.centre@ge.com
2. Fill in the RMA form
   Fill in only the white part of the form.
   Please ensure that all fields marked **(M)** are completed such as:
   - Equipment model
   - Model No. and Serial No.
   - Description of failure or modification required (please be specific)
   - Value for customs (in case the product requires export)
   - Delivery and invoice addresses
   - Contact details
3. Send the RMA form to your local contact
   For a list of local service contacts worldwide, email us at:
   contact.centre@ge.com
4. The local service contact provides the shipping information
   Your local service contact provides you with all the information needed to ship the product:
   - Pricing details
   - RMA number
   - Repair centre address

   If required, an acceptance of the quote must be delivered before going to the next stage.
5. Send the product to the repair centre
   - Address the shipment to the repair centre specified by your local contact
   - Make sure all items are packaged in an anti-static bag and foam protection
   - Make sure a copy of the import invoice is attached with the returned unit
   - Make sure a copy of the RMA form is attached with the returned unit
   - E-mail or fax a copy of the import invoice and airway bill document to your local contact.

CHAPTER 21

TECHNICAL SPECIFICATIONS

21.1 CHAPTER OVERVIEW

This chapter describes the technical specifications of the product.

This chapter contains the following sections:

Chapter Overview 496
Interfaces 497
Performance of Transformer Differential Protection and Monitoring Functions 501
Performance of Current Protection Functions 504
Performance of Voltage Protection Functions 507
Performance of Frequency Protection Functions 509
Performance of Monitoring and Control Functions 510
Measurements and Recording 512
Ratings 514
Input/Output Connections 517
Mechanical Specifications 519
Type Tests 520
Environmental Conditions 521
Electromagnetic Compatibility 522

21.2 INTERFACES

21.2.1 GRAPHICAL HMI

Graphical HMI	
Screen size	4.0" diagonal
Display format	480 x 480 Dots
Number of colour	16.7M
Dimensions	77 mm (H) x 80 mm (V) x 2.3 mm (D)
Active area	71.86 mm (H) x 70.18 mm (V)
Display mode	Transmissive/normally black
Viewing direction	All round
Backlight type	LED, white
Operating temperature	-30°C ~ + 85°C
Storage temperature	-40°C ~ + 90°C

21.2.2 FRONT USB PORT

Front USB port	
Use	For local connection to laptop for configuration purposes and firmware downloads
Connector	USB type B
Isolation	Isolation to ELV level
Constraints	Maximum cable length 5 m

21.2.3 REAR SERIAL PORT 1

Rear serial port 1 (RP1)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus
Connector	General purpose block, M4 screws (2 wire)
Cable	Screened twisted pair (STP)
Supported Protocols *	Courier, IEC-60870-5-103, DNP3.0
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m

21.2.4 FIBRE REAR SERIAL PORT 1

Optional fibre rear serial port (RP1)	
Main Use	Serial SCADA communications over fibre
Connector	IEC 874-10 BFOC 2.5 –(ST®) (1 each for Tx and Rx)
Fibre type	Multimode 50/125 µm or 62.5/125 µm
Supported Protocols	Courier, IEC870-5-103, DNP 3.0
Wavelength	850 nm

21.2.5 REAR SERIAL PORT 2

Optional rear serial port (RP2)	
Use	For SCADA communications (multi-drop)
Standard	EIA(RS)485, K-bus, EIA(RS)232
Designation	SK4
Connector	9 pin D-type female connector
Cable	Screened twisted pair (STP)
Supported Protocols	Courier
Isolation	Isolation to SELV level
Constraints	Maximum cable length 1000 m for RS485 and K-bus, 15 m for RS232

21.2.6 OPTIONAL REAR SERIAL PORT (SK5)

Optional rear serial port for teleprotection	
Use	For teleprotection in distance products
Standard	EIA(RS)232
Designation	SK5
Connector	9 pin D-type female connector
Cable	Screened twisted pair (STP)
Supported Protocols	InterMiCOM (IM)
Isolation	Isolation to SELV level
Constraints	Maximum cable length 15 m

21.2.7 IRIG-B (DEMODULATED)

IRIG-B Interface (Demodulated)	
Use	External clock synchronisation signal
Standard	IRIG 200-98 format B00X
Connector	BNC
Cable type	50 ohm coaxial
Isolation	Isolation to SELV level
Input signal	TTL level
Input impedance	10 k ohm at dc
Accuracy	+/- 1 ms

21.2.8 IRIG-B (MODULATED)

IRIG-B Interface (Modulated)	
Use	External clock synchronisation signal
Standard	IRIG 200-98 format B12X
Connector	BNC
Cable type	50 ohm coaxial
Isolation	Isolation to SELV level

IRIG-B Interface (Modulated)	
Input signal	peak to peak, 200 mV to 20 mV
Input impedance	6 k ohm at 1000 Hz
Accuracy	+/- 1 ms

21.2.9 REAR ETHERNET PORT COPPER

Rear Ethernet Port Using CAT 5/6/7 Wiring	
Main Use	Substation Ethernet communications
Standard	IEEE 802.3 10BaseT/100BaseTX
Connector	RJ45
Cable type	Screened twisted pair (STP)
Isolation	1.5 kV
Supported Protocols	Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog
Redundancy Protocols Supported	PRP (Parallel Redundancy Protocol) HSR (High-availability Seamless Redundancy) RSTP (Rapid Spanning Tree Protocol) Failover
Constraints	Maximum cable length 100 m

21.2.10 REAR ETHERNET PORT FIBRE

Rear Ethernet Port Using Fibre-optic Cabling	
Main Use	Substation Ethernet communications
Connector	IEC 874-10 BFOC 2.5 - (LC®) (1 each for Tx and Rx)
Standard	IEEE 802.3 100 BaseFX
Fibre type	Multimode 50/125 µm (OM2 or OM3) or 62.5/125 µm (OM1)
Supported Protocols	Courier (tunnelled), IEC 61850, PTP, SNTP, SNMP, RADIUS, syslog
Redundancy Protocols Supported	PRP (Parallel Redundancy Protocol) HSR (High-availability Seamless Redundancy) RSTP (Rapid Spanning Tree Protocol) Failover
Wavelength	1310 nm

21.2.10.1 100 BASE FX RECEIVER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)	-31.0		-12.0	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Conditions: TA = 0°C to 70°C

21.2.10.2 100 BASE FX TRANSMITTER CHARACTERISTICS

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power BOL 62.5/125 µm NA = 0.275 Fibre EOL	PO	-20	-17.0	-14.0	dBm avg.
Output Optical Power BOL 50/125 µm NA = 0.20 Fibre EOL	PO	-24.0	-21.0	-17.0	dBm avg.
Optical Extinction Ratio	ER	10			dB
Output Optical Power at Logic "0" State	$P_{O(off)}$			-45	dBm avg.

Conditions: TA = 0°C to 70°C

21.3 PERFORMANCE OF TRANSFORMER DIFFERENTIAL PROTECTION AND MONITORING FUNCTIONS

21.3.1 TRANSFORMER DIFFERENTIAL PROTECTION

Accuracy	
Pick-up	Formula +/-5% or 20 mA, whichever is greater
Drop-off	0.95 x formula +/- 5% or 20 mA, whichever is greater
Pick-up and drop-off repeatability	< 1%
Low set differential element operate time (High Break contact)	< 33 ms (currents applied at 1.2x pickup level or higher)
Low set differential element operate time (Standard Contact)	< 36 ms (currents applied at 1.2x pickup level or higher)
High set 1 differential element operate time (Transient Bias disabled)	< 15 ms (currents applied at 2x pickup level or higher)
High set 2 differential element operate time (High Break contact)	< 25 ms (currents applied at 2x pickup level or higher)
DT operate time (High Break contact)	< 33 ms, whichever is greater (currents applied at 1.2x pickup level or higher
DT operate time (Standard contact)	< 36 ms, whichever is greater (currents applied at 1.2x pickup level or higher
Operate time repeatability	< 2 ms
Disengagement time	< 15 ms
2nd harmonic blocking pick-up	Setting +/-5% of setting or 20 mA, whichever is greater
2nd harmonic blocking drop-off	0.95 x setting +/-5% or 20 mA, whichever is greater
5th harmonic blocking pick-up	Setting +/-5% of setting or 20 mA, whichever is greater
5th harmonic blocking drop-off	0.95 x setting +/-5% or 20 mA, whichever is greater

Note:
Transformer differential protection operating times are with the ***Diff Protection - Phase Comparison*** *setting* ***Disabled****.*

21.3.2 MATCHING FACTORS

CT Type	Max. sensitivity	Permitted Matching Factor range	Matching factor for typical setting Is1 = 0.2 pu
Standard	43 mA	0.05 - 15	4.65
Sensitive	13 mA	0.05 - 20	15.38

21.3.3 CIRCUITRY FAULT ALARM

Pick-up	Formula +/- 5% (for Is-cctfail > 0.05 pu)
Drop-off	0.95 x formula +/- 5% or 20 mA, whichever is greater

Pick-up and drop-off repeatability	< 4%
DT operate	< 26 ms (currents applied at 2.5x pickup level or higher)
Operate time repeatability	< 8 ms
Disengagement time	< 26 ms
Timer	+/- 2% or 50 ms, whichever is greater

21.3.4 THROUGH FAULT MONITORING

Overcurrent pick-up	Setting +/-5% or 50 mA, whichever greater
Overcurrent drop-off	0.95 x setting +/- 5% or 50 mA, whichever is greater
Heating pickup (I2t)	Setting +/-2% or 5 A^2s, whichever greater

21.3.5 THERMAL OVERLOAD

Accuracy	
Hot Spot pick-up	Expected pick-up time +/-5% or 50 ms, whichever greater. (Expected pick-up time is the time required to reach the temperature setting)
Hot Spot operate	DT +/-5% or <= 50 ms, whichever greater
Top Oil pick-up	Expected pick-up time +/-5% or 50 ms, whichever greater
Top Oil operate	DT +/-5% or <= 50 ms, whichever greater
Repeatability	< 2.5%

21.3.6 TRANSFORMER AND LOSS OF LIFE

Loss of Life	
FAA > pick-up	Formula: +/-5%
Loss of life > pick-up	Expected pick-up current +/-5%
Repeatability	< 2.5%
FAA > DT	±5% or 200 ms, whichever is greater

21.3.7 LOW IMPEDANCE RESTRICTED EARTH FAULT

Pick-up	Formula +/-5% or 20 mA, whichever is greater
Drop-off	0.9 x formula +/- 5% or 20 mA, whichever is greater
Pick-up and drop-off repeatability	< 5%
Operate time	< 30 ms (currents applied at 3x pickup level or higher)
Operate time repeatability	< 5 ms
Disengagement time	< 30 ms

21.3.8 HIGH IMPEDANCE RESTRICTED EARTH FAULT

Pick-up	Formula +/-5% or 20 mA, whichever is greater
Drop-off	0.9 x formula +/- 5% or 20 mA, whichever is greater
Pick-up and drop-off repeatability	< 5%
Operate time	< 30 ms
Operate time repeatability	< 5 ms
Disengagement time	< 30 ms

21.4 PERFORMANCE OF CURRENT PROTECTION FUNCTIONS

21.4.1 TRANSIENT OVERREACH AND OVERSHOOT

Accuracy	
Additional tolerance due to increasing X/R ratios	+/-5% over the X/R ratio of 1 to 120
Overshoot of overcurrent elements	< 40 ms
Disengagement time	< 30 ms

21.4.2 THREE-PHASE OVERCURRENT PROTECTION

Accuracy	
IDMT pick-up	1.05 x Setting +/-5% or 20 mA, whichever is greater
DT pick-up	Setting +/-5% or 20 mA, whichever is greater
Drop-off (IDMT and DT)	0.95 x setting +/-5% or 20 mA, whichever is greater
IDMT operate	+/-5% of expected operating time or 40 ms, whichever is greater
IEEE reset	+/-5% or 50 ms, whichever is greater
DT operate	+/-2% of setting or 50 ms, whichever is greater
DT reset	Setting +/-5%
Characteristic UK	IEC 60255-3 1998
Characteristic US	IEEE C37.112 1996

21.4.2.1 THREE-PHASE OVERCURRENT DIRECTIONAL PARAMETERS

Accuracy	
Directional boundary pickup (RCA +/-90%)	+/-2°
Directional boundary hysteresis	< 3°
Directional boundary repeatability	<1%
Directional voltage pick-up	+/-5% or 50 mV, whichever is greater
Directional voltage drop-off	0.95 x setting +/-5% or 50 mV, whichever is greater
Directional voltage repeatability	<3%

21.4.3 VOLTAGE DEPENDENT OVERCURRENT PROTECTION

Accuracy	
Voltage threshold pick-up	Setting +/- 5%
Voltage threshold drop-off	1.05 x setting +/- 5%
Current threshold pick-up	Formula +/- 5% or 50 mA, whichever is greater
Current threshold drop-off	0.95 x formula +/- 5% or 50 mA, whichever is greater

Note:
Reference conditions: IDMT accuracy = +/- 5% or 50 ms for M value above 1.1

21.4.4 EARTH FAULT PROTECTION

Accuracy	
IDMT pick-up	1.05 x Setting +/-5% or 20 mA, whichever is greater
DT pick-up	Setting +/-5%, or 20 mA, whichever is greater
Measured drop-off (IDMT and DT)	0.95 x setting +/-5% or 20 mA, whichever is greater
Derived drop-off (IDMT and DT)	0.9 x setting +/-5% or 20 mA, whichever is greater
IDMT Operate	+/-5% or 40 ms, whichever is greater*
IEEE reset	+/-5% or 40 ms, whichever is greater
Pick-up and drop-off repeatability	< 2%
DT operate time	+/-2% or 50 ms, whichever is greater
DT reset time	+/- 5%

Note:
Reference conditions: TMS = 1, TD = 1, IN> = 1A, operating range = 2-16In

21.4.4.1 EARTH FAULT DIRECTIONAL PARAMETERS

Measured and Derived	
Vpol pick-up	Vpol +/-5% or 50 mV, whichever is greater
Vpol drop-off	0.95 x Vpol +/-5% or 50 mV, whichever is greater
Directional boundary pickup (RCA +/-90%)	+/- 2°
Directional boundary hysteresis	< 1°
Directional boundary repeatability	< 1%

21.4.5 NEGATIVE SEQUENCE OVERCURRENT PROTECTION

Pick-up (IDMT and DT)	Setting +/-5% or 20 mA, whichever is greater
Drop-off (IDMT and DT)	0.95 x Setting +/-5% or 20 mA, whichever is greater
Pick-up and drop-off repeatability	< 1%
Disengagement time	< 35 ms
DT operate	+/- 2% or 60 ms, whichever is greater
Operate time repeatability	< 6 ms

21.4.5.1 NPSOC DIRECTIONAL PARAMETERS

Directional boundary pick-up (RCA +/-90%)	+/-2°
Directional boundary hysteresis	< 2°
Directional boundary repeatability	< 2%
Vpol pickup	Setting +/-5% or 50 mV, whichever is greater
Vpol drop-off	0,95 x setting +/-5% or 50 mV, whichever is greater

21.4.6 CIRCUIT BREAKER FAIL PROTECTION

I< Pick-up	1.1 X setting +/- 5% or 20 mA, whichever is greater
I< Drop-off	Setting +/- 5% or 20 mA, whichever is greater
Timers	+/- 2% or 50 ms, whichever is greater
Reset time	< 15 ms (fully offset current waveform considered)

21.5 PERFORMANCE OF VOLTAGE PROTECTION FUNCTIONS

21.5.1 UNDERVOLTAGE PROTECTION (P643/5)

Pick-up (IDMT and DT)	Setting +/- 5%
Drop-off (IDMT and DT)	1.02 x Setting +/-5%
Operate (IDMT and DT)	+/- 2% or 50 ms, whichever is greater
Reset	< 50 ms
Repeatability	< 1%

21.5.2 OVERVOLTAGE PROTECTION

Pick-up (IDMT and DT)	Setting +/- 5%
Drop-off (IDMT and DT)	0.98 x Setting +/-5%
Operate (IDMT and DT)	+/- 2% or 50 ms, whichever is greater
Reset	< 50 ms
Repeatability	< 1%

21.5.3 RESIDUAL OVERVOLTAGE PROTECTION (P643/5)

Pick-up (IDMT and DT)	Setting +/- 5% or 50 mV, whichever is greater
Drop-off (IDMT and DT)	0.95 x Setting +/-5%
IDMT operate	+/- 2% or 55 ms, whichever is greater
DT operate	+/- 2% or 70 ms or whichever is greater
Reset time	< 50 ms
Disengagement time	< 35 ms
Pick-up and drop-off repeatability	<1%
Timer repeatability	< 10 ms

21.5.4 NEGATIVE SEQUENCE VOLTAGE PROTECTION

DT Pick-up	Setting +/- 5%
DT Drop-off	0.95 x Setting +/-5%
DT operate	+/- 2% or 50 ms, whichever is greater (accelerated mode) +/- 2% or 60 ms, whichever is greater (normal mode)
Disengagement time	<35 ms
Operating time Repeatability	< 5 ms
Operating threshold repeatability	< 1%

Note:
Reference conditions: IDMT accuracy = +/- 5% or 50 ms for M value above 1.1

21.6 PERFORMANCE OF FREQUENCY PROTECTION FUNCTIONS

21.6.1 OVERFREQUENCY PROTECTION

Pick-up	Setting +/- 10 mHz
Drop-off	Setting -25 mHz +/- 10 mHz
DT operate	+/- 2% or 70 ms, whichever is greater (excluding frequency tracking time delay)
Repeatability	< 1%

21.6.2 UNDERFREQUENCY PROTECTION

Pick-up	Setting +/- 10 mHz
Drop-off	Setting +25 mHz +/- 10 mHz
DT Operate	+/- 2% or 70 ms, whichever is greater (excluding frequency tracking time delay)
Repeatability	< 1%

21.6.3 OVERFLUXING PROTECTION

Pick-up	Setting +/- 5%
Drop-off	Setting -2% +/- 5%
Repeatability (operating threshold)	< 1%
IDMT operate	+/- 5% or 50 ms, whichever is greater
DT operate	+/- 2% or 50 ms, whichever is greater
Instantaneous operation	< 50 ms
Disengagement time	< 50 ms
Repeatability (operating times)	< 10 ms
V / Hz measurement	+/- 1%
Reset time	+/- 2% or 50 ms, whichever is greater

Note:
Reference conditions: IDMT accuracy = +/- 5% or 50 ms for M value above 1.1

21.7 PERFORMANCE OF MONITORING AND CONTROL FUNCTIONS

21.7.1 VOLTAGE TRANSFORMER SUPERVISION

VTS I> pick-up	Setting +/- 5% or 50 mA, whichever is greater
VTS I> drop-off	0.9 x Setting +/- 5% or 50 mA, whichever is greater
VTS I2> pick-up	Setting +/- 5% or 50 mA, whichever is greater
VTS I> drop-off	0.95 x Setting +/- 5% or 50 mA, whichever is greater
VTS V< pick-up (P642)	70V +/- 5%
VTS V< pick-up (P643/5)	10V +/- 5%
VTS V< drop-off (P642)	95V +/- 5%
VTS V< drop-off (P643/5)	30V +/- 5%
VTS V2> pick-up (P642/3/5)	10V +/- 5%
VTS V2> drop-off (P642/3/5)	9.5V +/- 5%
Fast block operation	< 25 ms
Fast block reset	< 30 ms
Time delay	Setting +/- 2% or 50 ms, whichever is greater
Pick-up and drop-off repeatability	< 1%

21.7.2 CURRENT TRANSFORMER SUPERVISION

CTS I1 pick-up ratio	Setting +/- 5% or 20 mA, whichever is greater
CTS I2/I1>1 pick-up ratio	0.95 x Setting +/- 5% or 20 mA, whichever is greater
CTS I2/I1>2 pick-up ratio	1.05 x setting +/- 5% or 20 mA, whichever is greater
CTS I1 drop-off ratio	0.95 x setting +/-5% or 20 mA, whichever is greater
CTS I2/I1>1 drop-off ratio	Setting +/-5% or 20 mA, whichever is greater
CTS I2/I1>2 drop-off ratio	Setting +/-5% or 20 mA, whichever is greater
Pick-up and drop-off repeatability	< 3%
Time delay operation	Setting +/-2% or 50 ms, whichever is greater
CTS terminal block operation	< 25 ms
CTS differential block operation	< 30 ms
CTS reset time	< 25 ms
CTS disengagement time	< 30 ms

21.7.3 POLE DEAD PROTECTION

Current pick-up	50 mA +/- 20 mA
Current drop-off	55 mA +/- 20 mA
Voltage pick-up	10V +/- 5%

Voltage drop-off	30V +/- 5%
DT operate	< 50 ms

21.7.4 PSL TIMERS

Output conditioner timer	Setting ±2% or 50 ms, whichever is greater
Dwell conditioner timer	Setting ±2% or 50 ms, whichever is greater
Pulse conditioner timer	Setting ±2% or 50 ms, whichever is greater

21.8 MEASUREMENTS AND RECORDING

21.8.1 GENERAL

General Measurement Accuracy	
General measurement accuracy	Typically +/- 1%, but +/- 0.5% between 0.2 - 2 In/Vn
Phase	0° to 360° +/- 0.5%
Current (0.05 to 3 In)	+/- 1.0% of reading, or 4mA (1A input), or 20mA (5A input)
Voltage (0.05 to 2 Vn)	+/- 1.0% of reading
Frequency (45 to 65 Hz)	+/- 0.025 Hz
Power (W) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading at unity power factor
Reactive power (Vars) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading at zero power factor
Apparent power (VA) (0.2 to 2 Vn and 0.05 to 3 In)	+/- 5.0% of reading
Energy (Wh) (0.2 to 2 Vn and 0.2 to 3 In)	+/- 5.0% of reading at unity power factor
Energy (Varh) (0.2 to 2 Vn and 0.2 to 3In)	+/- 5.0% of reading at zero power factor

21.8.2 DISTURBANCE RECORDS

Disturbance Records Measurement Accuracy	
Minimum record duration	0.1 s
Maximum record duration	10.5 s
Minimum number of records at 10.5 seconds	100
Magnitude and relative phases accuracy	+/- 5% of applied quantities
Duration accuracy	+/- 2%
Trigger position accuracy	+/- 2% (minimum Trigger 100 ms)

21.8.3 EVENT, FAULT AND MAINTENANCE RECORDS

Event, Fault & Maintenance Records	
Record location	Flash memory
Viewing method	Front panel display or Settings Application Software
Extraction method	Extracted via USB, RP1, RP2, NIC (Ethernet) port
Number of event records	Up to 5000 time tagged event records (newest overwrites oldest)
Number of fault records	Up to 100
Number of maintenance records	Up to 10
Event time stamp resolution	1 ms

21.8.4 RESISTIVE TEMPERATURE DETECTORS

Accuracy	
Pick-up:	Setting ±1°C

Accuracy	
Drop-off:	(Setting -1°C)
Operating time:	±2% or <3 s

21.9 RATINGS

21.9.1 AC MEASURING INPUTS

AC Measuring Inputs	
Nominal frequency	50 Hz or 60 Hz (settable)
Operating range	45 to 65 Hz
Phase rotation	ABC or CBA

21.9.2 CURRENT TRANSFORMER INPUTS

AC Current Inputs	
Nominal current (In)	1A or 5A
Nominal burden per phase	< 0.2 VA at In
AC current thermal withstand (5A input)	20 A (continuous operation) 150 A (for 10 s) 500 A (for 1 s)
AC current thermal withstand (1A input)	4 A (continuous operation) 30 A (for 10 s) 100 A (for 1 s)
Linearity	Standard: Linear up to 64 × In (non-offset AC current) Sensitive: Linear up to 2 × In (non-offset AC current)

21.9.3 VOLTAGE TRANSFORMER INPUTS

AC Voltage Inputs		
Version	100 V to 120 V (ph-ph)	380 V to 480 V (ph-ph)
Nominal burden per VT input *1	< 0.003 VA @ Vn (ph-n); Vn < 120/Ö3 V (ph-n) < 0.01 VA @ Vn (ph-n); Vn < 240/Ö3 V (ph-n)	< 0.02 VA @ Vn (ph-n); Vn < 440/3Ö V (ph-n) < 0.07 VA @ Vn (ph-n); Vn < 880/3Ö V (ph-n)
Linearity for each VT input	Linear up to 200 Vac rms	Linear up to 800 Vac rms
Continuous rating for each VT input	240 Vac rms	880 Vac rms
10 seconds rating for each VT input	312 Vac rms	1144 Vac rms

Note:
*Reference Conditions: *1 = Overfrequency operating range 50/60 Hz and over temperature range 20° +/- 5° C.*

21.9.4 AUXILIARY SUPPLY VOLTAGE

Nominal operating range	CORTEC option (DC only) 24 to 48 V DC CORTEC option (rated for AC or DC operation) 48 to 110 V DC 40 to 100 V AC rms CORTEC option (rated for AC or DC operation) 110 to 250 V DC 100 to 240 V AC rms
Maximum operating range	CORTEC option (DC only) 19 to 65 V DC CORTEC option (rated for AC or DC operation) 37 to 150 V DC 32 to 110 V AC rms CORTEC option (rated for AC or DC operation) 87 to 300 V DC 80 to 265 V AC rms
Frequency range for AC supply	45 to 65 Hz
Ripple	<15% for a DC supply (compliant with IEC 60255-26:2013)
Power up time	< 11 seconds

21.9.5 NOMINAL BURDEN

Quiescent burden	11.2 W or 22 VA
2nd rear communications port	1.25 W or 2.5 VA
Each relay output burden	0.13 W or 0.25 VA per output relay
Each opto-input burden (24 – 27 V)	0.065 W or 0.13 VA max
Each opto-input burden (30 – 34 V)	0.065 W or 0.13 VA max
Each opto-input burden (48 – 54 V)	0.125 W or 0.25 VA max
Each opto-input burden (110 – 125 V)	0.36 W or 0.72 VA max
Each opto-input burden (220 – 250 V)	0.9 W or 1.8 VA max

21.9.6 POWER SUPPLY INTERRUPTION

Standard	IEC 60255-26:2013 (DC and AC)
24-48V DC SUPPLY 100% interruption without de-energising	20 ms at 24 V (half and full load) 50 ms at 36 V (half and full load) 100 ms at 48 V (half and full load)
48-110V DC SUPPLY 100% interruption without de-energising	20 ms at 37V (half and full load) 50 ms at 60 V (half and full load) 100 ms at 72 V (half load) 100 ms at 85 V (full load) 200 ms at 110 V (half and full load)

110-250V DC SUPPLY 100% interruption without de-energising	20 ms at 87 V (half load) 50 ms at 110 V (half load) 50 ms at 98 V (full load) 100 ms at 160 V (half load) 100 ms at 135 V (full load) 200 ms at 210 V (half load) 200 ms at 174 V (full load)
40-100V AC SUPPLY 100% voltage dip without de-energising	50 ms at 32 V (half load) 10 ms at 32 V (full load)
100-240V AC SUPPLY 100% voltage dip without de-energising	50 ms at 80 V (full and half load)

Note:
Maximum loading = all inputs/outputs energised.

Note:
Quiescent or 1/2 loading = 1/2 of all inputs/outputs energised.

21.9.7 SUPERCAPACITOR

Discharge time	>14 days

21.10 INPUT/OUTPUT CONNECTIONS

21.10.1 ISOLATED DIGITAL INPUTS

Opto-isolated digital inputs (opto-inputs)	
Compliance	ESI 48-4
Rated nominal voltage	24 to 250 V dc
Operating range	19 to 265 V dc
Withstand	300 V dc
Recognition time with half-cycle ac immunity filter removed	< 2 ms
Recognition time with filter on	< 12 ms

21.10.1.1 NOMINAL PICKUP AND RESET THRESHOLDS

Nominal battery voltage	Logic levels: 60-80% DO/PU	Logic Levels: 50-70% DO/PU
24/27 V	Logic 0 < 16.2V, Logic 1 > 19.2V	Logic 0 <12V, Logic 1 > 16.8V
30/34	Logic 0 < 20.4V, Logic 1 > 24V	Logic 0 < 15V, Logic 1 > 21V
48/54	Logic 0 < 32.4V, Logic 1 > 38.4V	Logic 0 < 24V, Logic 1 > 33.6V
110/125	Logic 0 < 75V, Logic 1 > 88V	Logic 0 < 55.V, Logic 1 > 77V
220/250	Logic 0 < 150V, Logic 1 > 176V	Logic 0 < 110V, Logic 1 > 154V

Note:
Filter is required to make the opto-inputs immune to induced AC voltages.

In addition to the above thresholds, some models of this product provide the following threshold levels for FSK applications:

- For 220/250 voltage inputs: Logic 0 < 145V, Logic 1 > 165V

21.10.2 STANDARD OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	General purpose relay outputs for signalling, tripping and alarming
Rated voltage	300 V
Maximum continuous current	10 A
Short duration withstand carry	30 A for 3 s 250 A for 30 ms
Make and break, dc resistive	50 W
Make and break, dc inductive	62.5 W (L/R = 50 ms)
Make and break, ac resistive	2500 VA resistive (cos phi = unity)
Make and break, ac inductive	2500 VA inductive (cos phi = 0.7)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to a maximum load of 7500W))

Make, carry and break, dc resistive	4 A for 1.5 s, 10000 operations (subject to the above limit for make and break, dc resistive load)
Make, carry and break, dc inductive	0.5 A for 1 s, 10000 operations (subject to the above limit for make and break, dc inductive load)
Make, carry and break ac resistive	30 A for 200 ms, 2000 operations (subject to the above limits)
Make, carry and break ac inductive	10 A for 1.5 s, 10000 operations (subject to the above limits)
Loaded contact	10000 operations min.
Unloaded contact	100000 operations min.
Operate time	< 5 ms
Reset time	< 10 ms

21.10.3 HIGH BREAK OUTPUT CONTACTS

Compliance	In accordance with IEC 60255-1:2009
Use	For applications requiring high rupture capacity
Rated voltage	300 V
Maximum continuous current	10 A DC
Short duration withstand carry	30 A DC for 3 s 250 A for 30 ms
Make and break, dc resistive	7500 W
Make and break, dc inductive	2500 W (L/R = 50 ms)
Make and carry, dc resistive	30 A for 3 s, 10000 operations (subject to the above limits)
Make, carry and break, dc resistive	30 A for 3 s, 5000 operations (subject to the above limit for make and break, dc resistive load) 30 A for 200 ms, 10000 operations (subject to the above limit for make and break, dc resistive load)
Make, carry and break, dc inductive	10 A for 40 ms, 10000 operations (subject to the above limit for make and break, dc inductive load) 10 A for 20 ms (250V, 4 shots per second, subject to the above limit for make and break, dc inductive load)
Loaded contact	10,000 operations minimum.
Unloaded contact	100,000 operations minimum.
Operate time	< 0.2 ms
Reset time	< 8 ms
MOV Protection	Maximum voltage 330 V DC

21.10.4 WATCHDOG CONTACTS

Use	Non-programmable contacts for relay healthy/relay fail indication
Breaking capacity, dc resistive	30 W
Breaking capacity, dc inductive	15 W (L/R = 40 ms)
Breaking capacity, ac inductive	375 VA inductive (cos phi = 0.7)

21.11 MECHANICAL SPECIFICATIONS

21.11.1 PHYSICAL PARAMETERS

Case Types*	40TE 60TE 80TE
Weight (40TE case)	7 kg – 8 kg (depending on chosen options)
Weight (60TE case)	9 kg – 12 kg (depending on chosen options)
Weight (80TE case)	13 kg - 16 kg (depending on chosen options)
Dimensions in mm (w x h x l) (40TE case)	W: 206.0 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w x h x l) (60TE case)	W: 309.6 mm H: 177.0 mm D: 243.1 mm
Dimensions in mm (w x h x l) (80TE case)	W 413.2 mm H 177.0 mm D 243.1 mm
Mounting	Panel, rack, or retrofit

Note:
**Case size is product dependent.*

21.11.2 ENCLOSURE PROTECTION

Against dust and dripping water (front face)	IP52 as per IEC 60529:1989/A2:2013
Protection against dust (whole case)	IP50 as per IEC 60529:1989/A2:2013
Protection for sides of the case (safety)	IP30 as per IEC 60529:1989/A2:2013
Protection for rear of the case (safety)	IP10 as per IEC 60529:1989/A2:2013

21.11.3 MECHANICAL ROBUSTNESS

Vibration test per EN 60255-21-1:1998	Response: class 2, Endurance: class 2
Shock and bump immunity per EN 60255-21-2:1988	Shock response: class 2, Shock withstand: class 1, Bump withstand: class 1
Seismic test per EN 60255-21-3: 1993	Class 2

21.11.4 TRANSIT PACKAGING PERFORMANCE

Primary packaging carton protection	ISTA 1C
Vibration tests	3 orientations, 7 Hz, amplitude 5.3 mm, acceleration 1.05g
Drop tests	10 drops from 610 mm height on multiple carton faces, edges and corners

21.12 TYPE TESTS

21.12.1 INSULATION

Compliance	IEC 60255-27: 2013
Insulation resistance	> 100 M ohm at 500 V DC (Using only electronic/brushless insulation tester)

21.12.2 CREEPAGE DISTANCES AND CLEARANCES

Compliance	IEC 60255-27: 2013
Pollution degree	3
Overvoltage category	III
Impulse test voltage (not RJ45)	5 kV
Impulse test voltage (RJ45)	1 kV

21.12.3 HIGH VOLTAGE (DIELECTRIC) WITHSTAND

IEC Compliance	IEC 60255-27: 2013
Between all independent circuits	2 kV ac rms for 1 minute
Between independent circuits and protective earth conductor terminal	2 kV ac rms for 1 minute
Between all case terminals and the case earth	2 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute
Across open contacts of changeover output relays	1 kV ac rms for 1 minute
Between all RJ45 contacts and protective earth	1 kV ac rms for 1 minute
Between all screw-type EIA(RS)485 contacts and protective earth	1 kV ac rms for 1 minute
ANSI/IEEE Compliance	ANSI/IEEE C37.90-2005
Across open contacts of normally open output relays	1.5 kV ac rms for 1 minute
Across open contacts of normally open changeover output relays	1 kV ac rms for 1 minute
Across open watchdog contacts	1 kV ac rms for 1 minute

21.12.4 IMPULSE VOLTAGE WITHSTAND TEST

Compliance	IEC 60255-27: 2013
Between all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between terminals of all independent circuits	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J
Between all independent circuits and protective earth conductor terminal	Front time: 1.2 µs, Time to half-value: 50 µs, Peak value: 5 kV, 0.5 J

Note:
Exceptions are communications ports and normally-open output contacts, where applicable.

21.13 ENVIRONMENTAL CONDITIONS

21.13.1 AMBIENT TEMPERATURE RANGE

Compliance	IEC 60255-27: 2013
Test Method	IEC 60068-2-1:2007 and IEC 60068-2-2 2007
Operating temperature range	-25°C to +55°C (continuous)
Storage and transit temperature range	-25°C to +70°C (continuous)

21.13.2 TEMPERATURE ENDURANCE TEST

Temperature Endurance Test	
Test Method	IEC 60068-2-1: 2007 and 60068-2-2: 2007
Operating temperature range	-40°C (96 hours) +70°C (96 hours)
Storage and transit temperature range	-40°C (96 hours) +70°C (96 hours)

21.13.3 AMBIENT HUMIDITY RANGE

Compliance	IEC 60068-2-78: 2012 and IEC 60068-2-30: 2005
Durability	56 days at 93% relative humidity and +40°C
Damp heat cyclic	six (12 + 12) hour cycles, 93% RH, +25 to +55°C

21.13.4 CORROSIVE ENVIRONMENTS

Compliance, Industrial corrosive environment/poor environmental control	IEC 60068-2-42: 2003, IEC 60068-2-43: 2003, IEC 60068-2-52: 1996
Sulphur Dioxide, IEC 60068-2-42: 2003	21 days exposure to elevated concentrations (25ppm) of SO_2 at 75% relative humidity and +25°C
Hydrogen Sulphide, IEC 60068-2-43: 2003	21 days exposure to elevated concentrations (10ppm) of H_2S at 75% relative humidity and +25°C
Salt mist, IEC 60068-2-52: 1996	7 days, KB severity 3

21.14 ELECTROMAGNETIC COMPATIBILITY

21.14.1 1 MHZ BURST HIGH FREQUENCY DISTURBANCE TEST

Compliance	IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Differential test voltage (level 3)	1.0 kV

21.14.2 DAMPED OSCILLATORY TEST

Compliance	EN61000-4-18: 2011: Level 3, 100 kHz and 1 MHz. Level 4: 3 MHz, 10 MHz and 30 MHz, IEC 60255-26:2013
Common-mode test voltage (level 3)	2.5 kV
Common-mode test voltage (level 4)	4.0 kV
Differential mode test voltage	1.0 kV

21.14.3 IMMUNITY TO ELECTROSTATIC DISCHARGE

Compliance	IEC 60255-26:2013, IEC 61000-4-2:2009
Class 4 Condition	15 kV discharge in air to user interface, display, and exposed metalwork
Class 3 Condition	8 kV discharge in air to all communication ports

21.14.4 ELECTRICAL FAST TRANSIENT OR BURST REQUIREMENTS

Compliance	IEC 60255-26:2013, IEC 61000-4-4:2012
Applied to communication inputs	Amplitude: 2 kV, burst frequency 5 kHz and 100 KHz (level 4)
Applied to power supply and all other inputs except for communication inputs	Amplitude: 4 kV, burst frequency 5 kHz and 100 KHz (level 4)

21.14.5 SURGE WITHSTAND CAPABILITY

Compliance	IEEE/ANSI C37.90.1: 2012
Condition 1	4 kV fast transient and 2.5 kV oscillatory applied common mode and differential mode to opto inputs, output relays, CTs, VTs, power supply
Condition 2	4 kV fast transient and 2.5 kV oscillatory applied common mode to communications, IRIG-B

21.14.6 SURGE IMMUNITY TEST

Compliance	IEC 60255-26:2013, IEC 61000-4-5:2014+AMD1:2017
Pulse duration	Time to half-value: 1.2/50 µs
Between all groups and protective earth conductor terminal	Amplitude 4 kV
Between terminals of each group (excluding communications ports, where applicable)	Amplitude 2 kV

21.14.7 IMMUNITY TO RADIATED ELECTROMAGNETIC ENERGY

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency band	80 MHz to 3.0 GHz
Spot tests at	80, 160, 380, 450, 900, 1850, 2150 MHz
Test field strength	10 V/m
Test using AM	1 kHz @ 80%
Compliance	IEEE/ANSI C37.90.2: 2004
Frequency band	80 MHz to 1 GHz
Spot tests at	80, 160, 380, 450 MHz
Waveform	1 kHz @ 80% am and pulse modulated
Field strength	35 V/m

21.14.8 RADIATED IMMUNITY FROM DIGITAL COMMUNICATIONS

Compliance	IEC 61000-4-3:2006 + A2:2010
Frequency bands	800 to 960 MHz, 1.4 to 2.0 GHz
Test field strength	30 V/m
Test using AM	1 kHz / 80%

21.14.9 RADIATED IMMUNITY FROM DIGITAL RADIO TELEPHONES

Compliance	IEC 60255-26:2013, IEC 61000-4-3:2006 + A2:2010
Frequency bands	900 MHz and 1.89 GHz
Test field strength	10 V/m

21.14.10 IMMUNITY TO CONDUCTED DISTURBANCES INDUCED BY RADIO FREQUENCY FIELDS

Compliance	IEC 60255-26:2013, IEC 61000-4-6:2013 Level 3
Frequency bands	150 kHz to 80 MHz

Test disturbance voltage	10 V rms
Test using AM	1 kHz @ 80%
Spot tests	27 MHz and 68 MHz

21.14.11 MAGNETIC FIELD IMMUNITY

Compliance	IEC 61000-4-8:2009 Level 5 IEC 61000-4-9:2016 Level 5 IEC 61000-4-10:2016 Level 5
IEC 61000-4-8 test	100 A/m applied continuously, 1000 A/m applied for 3 s
IEC 61000-4-9 test	1000 A/m applied in all planes
IEC 61000-4-10 test	100 A/m applied in all planes at 100 kHz/1 MHz with a burst duration of 2 seconds

21.14.12 CONDUCTED EMISSIONS

Compliance	IEC 60255-26:2013, EN 55032: 2015+A1:2020
Power supply test 1	0.15 - 0.5 MHz, 79 dBµV (quasi peak) 66 dBµV (average)
Power supply test 2	0.5 – 30 MHz, 73 dBµV (quasi peak) 60 dBµV (average)
RJ45 test 1 (where applicable)	0.15 - 0.5 MHz, 97 dBµV (quasi peak) 84 dBµV (average)
RJ45 test 2 (where applicable)	0.5 – 30 MHz, 87 dBµV (quasi peak) 74 dBµV (average)

21.14.13 RADIATED EMISSIONS

Compliance	IEC 60255-26:2013
Test 1	30 – 230 MHz, 40 dBµV/m at 10 m measurement distance
Test 2	230 – 1 GHz, 47 dBµV/m at 10 m measurement distance
Test 3	1 – 2 GHz, 76 dBµV/m at 10 m measurement distance

21.14.14 POWER FREQUENCY

Compliance	IEC 60255-26:2013
Opto-inputs (Compliance is achieved using the opto-input filter)	300 V common-mode (Class A) 150 V differential mode (Class A)

Note:
Compliance is achieved using the opto-input filter.

APPENDIX A

ORDERING OPTIONS

CORTEC Order Code Matrix		1-3	4	5	6	7	8	9	10	11	12-13	14	15
Transformer Protection		P64									AB		
2 End: 2 Winding Transformer			2										
3 End: 3 Winding Transformer			3										
5 End: 3 Winding Transformer			5										
Nominal Auxiliary Supply Voltage													
24-54 Vdc				7									
48-125 Vdc (40-100 Vac)				8									
110-250 Vdc (100-240 Vac)				9									
CT and VT Ratings	CT/Hardware Opt. Compatibility												
HV-LV In = 1A/5A, Vn = (100/120V) (xCT/1VT) Standard CT	P642 = 8, P643 = 12, P645 = 18				1								
HV-LV In = 1A/5A, Vn = (100/120V) (xCT/4VT) Standard CT (8 CT & 2VT for P642)	P642 = 8, P643 = 12, P645 = 18				2								
HV-LV In = 1A/5A, Vn = (100/120V) (xCT/1VT) Sensitive CT (P643/5 Only)	P643 = 12, P645 = 18				3								
HV-LV In = 1A/5A, Vn = (100/120V) (xCT/4VT) Sensitive CT (P643/5 Only)	P643 = 12, P645 = 18				4								
Hardware Options													
Standard - 1 x RS485 rear serial communications port provided with all ordering options (Courier, -103, DNP3 ready)						1							
With additional IRIG-B (Modulated)						2							
With additional IRIG-B (Modulated) & Serial Fibre Optic comms						4							
Single Ethernet 1 LC Duplex port + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						U							
Redundant Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex port + IEC870-103 Serial Fibre ST ports + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						V							
Redundant Ethernet PRP/HSR/RSTP/Failover 2 RJ45 + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						W							
Redundant Ethernet PRP/HSR/RSTP/Failover 2 LC Duplex ports + Universal IRIG-B + 1588 + 1 RJ45 Maintenance Port						Y							
Input/Output Options	Case Size Compatibility												
8 inputs, 8 outputs	40TE, 60TE						B						
12 inputs, 12 outputs	60TE						E						
16 inputs, 16 outputs	60TE						H						
16 inputs, 16 outputs + 4 High-Speed High-Break	60TE, 80TE						J						
16 inputs, 21 outputs	60TE, 80TE						K						
16 inputs, 24 outputs	60TE, 80TE						L						
20 inputs, 20 outputs	60TE, 80TE						P						
24 inputs, 16 outputs	60TE, 80TE						S						
24 inputs, 16 outputs + 8 High-Speed High-Break	80TE						T						
24 inputs, 24 outputs	80TE						U						
24 inputs, 32 outputs	80TE						V						
32 inputs, 24 outputs	80TE						1						
32 inputs, 32 outputs	80TE						2						
40 inputs, 24 outputs	80TE						4						
48 inputs, 16 outputs	80TE						7						
Product Specific Options													
RTD								A					
CLIO								B					
RTD + CLIO								C					
None								X					
Case Size and Mounting	Product Compatibility												
80TE Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P642, P643, P645								S				
80TE Case - 19" Rack Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys 40TE	P642, P643, P645								T				
Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port, without Function Keys 60TE	P642								U				
Case - Flush/Panel Mounting with Harsh Env. Coating, with USB Port and 10 Function Keys	P642, P643								V				
Product Features													
Standard Version										X			
Software Version													
Enhanced cybersecurity, concurrent protocols, 5000 events, 100 fault records, 1050s oscillography											AB		
Customer-Specific Additions													
Standard version												0	
Customer-specific configuration/options												A	
Hardware Version													
5th Generation Hardware, Graphical Colour HMI with High Performance Processing													Q

APPENDIX B

SETTINGS AND SIGNALS

Tables, containing a full list of settings for each model, are provided in a separate Excel file attached as an embedded resource. To access the spreadsheet file, click on the button below.

Note:
An Open File dialogue box may open with a warning message about potential harm from programs, macros or viruses. The file supplied does not contain any harmful content, and may be safely opened.

Settings and Signals

APPENDIX C

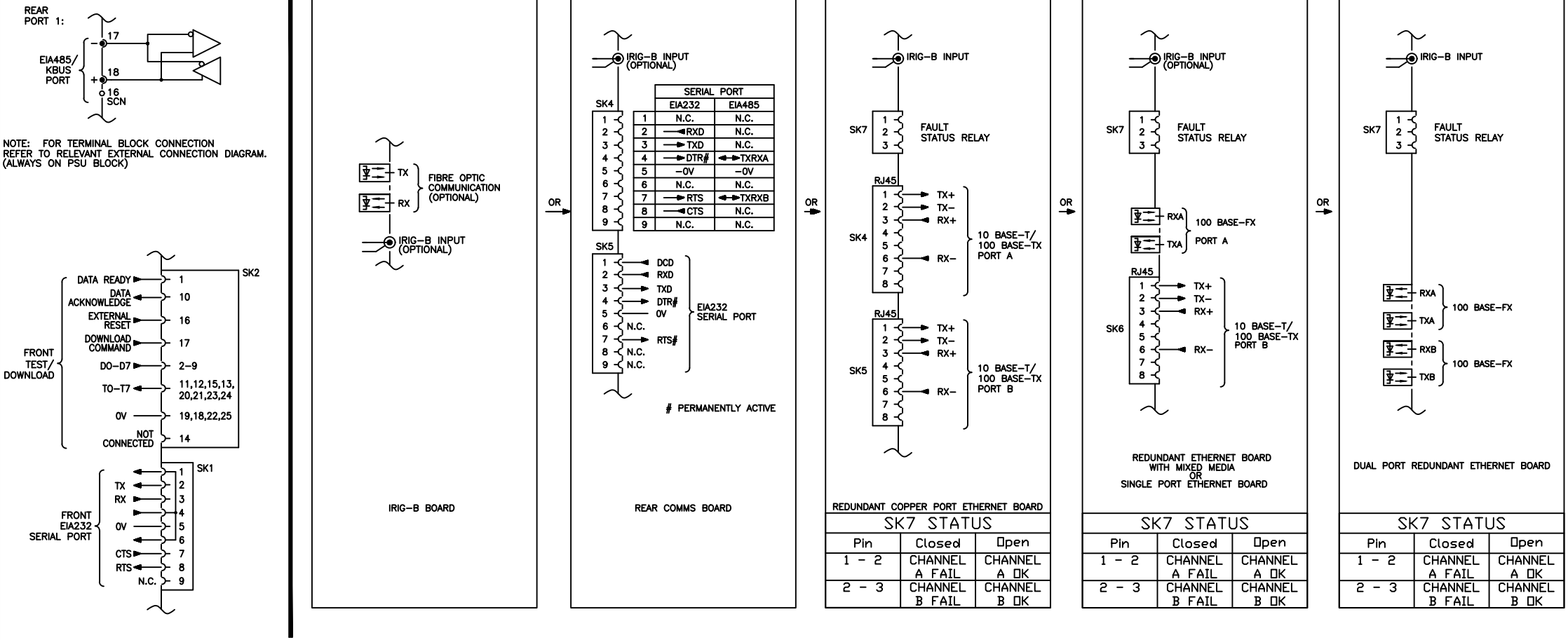
WIRING DIAGRAMS

Model	CORTEC Option*	Product Specific Option	Input/Output Options and Case Size Compatibility	Drawing-Sheet	Issue
All	-	-	Comms Options MiCOM Px40 Platform	10Px4001-1 10Px4001-2	N A
P642	I/O Option B	X	(8 I/P & 8 O/P) (40TE)	10P64201-1	L
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64201-2	H
	I/O Option B	A - RTD	(8 I/P & 8 O/P + RTD) (40TE)	10P64202-1	K
	I/O Option B	B - CLIO	(8 I/P & 8 O/P + CLIO) (40TE)	10P64203-1	K
	I/O Option B	A - RTD B - CLIO X	(8 I/P & 8 O/P) (60TE)	10P64217-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64217-2	
	I/O Option E	A - RTD B - CLIO X	(12 I/P & 12 O/P) (60TE)	10P64226-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64226-2	
	I/O Option H	X	(16 I/P & 16 O/P) (60TE)	10P64233-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64233-2	
	I/O Option J	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 16 O/P + 4 High-Speed High-Break) (80TE)	10P64237-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64237-2	
	I/O Option K	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 21 O/P) (80TE)	10P64241-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64241-2	
	I/O Option L	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 24 O/P) (80TE)	10P64245-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64245-2	
	I/O Option P	A - RTD B - CLIO C - RTD + CLIO X	(20 I/P & 20 O/P) (80TE)	10P64249-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64249-2	
	I/O Option S	A - RTD B - CLIO C - RTD + CLIO X	(24 I/P & 16 O/P) (80TE)	10P64257-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64257-2	
	I/O Option T	B - CLIO	(24 I/P & 16 O/P + 8 High-Speed High-Break) (80TE)	10P64258-1	C
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64258-2	
	I/O Option U	A - RTD B - CLIO X	(24 I/P & 24 O/P) (80TE)	10P64259-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64259-2	
	I/O Option V	X	(24 I/P & 32 O/P) (80TE)	10P64262-1	B
			High Z REF for 2 bias input transformer differential same principle applies to wire High Z REF for T2	10P64262-2	
P643	I/O Option H	X	(16 I/P & 16 O/P) (60TE)	10P64301-1 10P64301-2	G J
			High Z REF for 3 bias input transformer differential same principle applies to wire High Z REF for T2 & T3	10P64301-3	E
	I/O Option H	A - RTD	(16 I/P & 16 O/P + RTD) (60TE)	10P64302-1 10P64302-2	G J
	I/O Option H	B - CLIO	(16 I/P & 16 O/P + CLIO) (60TE)	10P64303-1 10P64303-2	H J

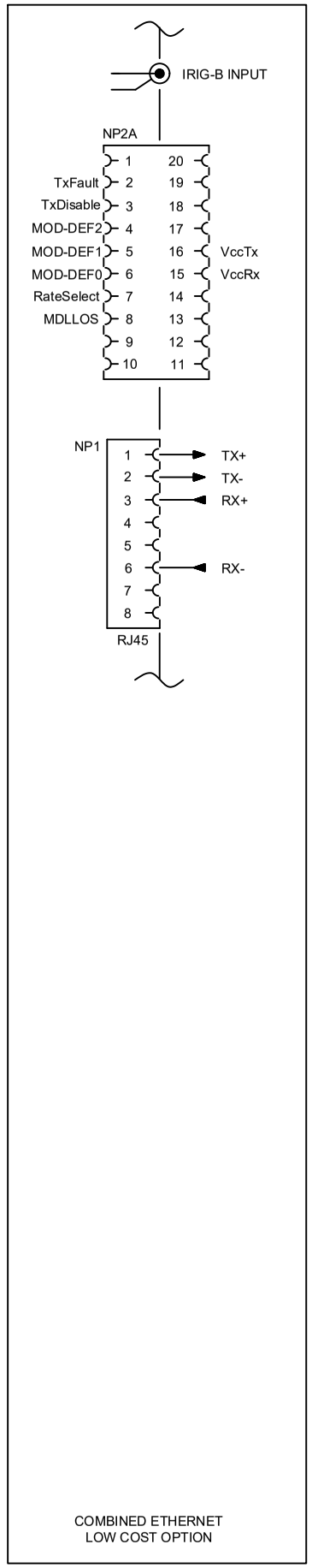
Model	CORTEC Option*	Product Specific Option	Input/Output Options and Case Size Compatibility	Drawing-Sheet	Issue
P643	I/O Option J	X	(16 I/P & 16 O/P + 4 High-Speed High-Break) (60TE)	10P64306-1 10P64306-2	G J
	I/O Option J	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 16 O/P + 4 High-Speed High-Break) (80TE)	10P64330-1 10P64330-2	A
	I/O Option K	X	(16 I/P & 21 O/P) (60TE)	10P64322-1 10P64322-2	A
	I/O Option K	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 21 O/P) (80TE)	10P64335-1 10P64335-2	A
	I/O Option L	X	(16 I/P & 24 O/P) (60TE)	10P64305-1 10P64305-2	G J
	I/O Option L	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 24 O/P) (80TE)	10P64339-1 10P64339-2	A
	I/O Option P	X	(20 I/P & 20 O/P) (60TE)	10P64345-1 10P64345-2	A
	I/O Option P	A - RTD B - CLIO C - RTD + CLIO X	(20 I/P & 20 O/P) (80TE)	10P64342-1 10P64342-2	A
	I/O Option S	X	(24 I/P & 16 O/P) (60TE)	10P64304-1 10P64304-2	H J
	I/O Option S	A - RTD B - CLIO C - RTD + CLIO X	(24 I/P & 16 O/P) (80TE)	10P64362-1 10P64362-2	A
	I/O Option T	A - RTD B - CLIO X	(24 I/P & 16 O/P + 8 High-Speed High-Break) (80TE)	10P64363-1 10P64363-2	A
	I/O Option U	A - RTD B - CLIO C - RTD + CLIO X	(24 I/P & 24 O/P) (80TE)	10P64352-1 10P64352-2	A
	I/O Option V	A - RTD B - CLIO X	(24 I/P & 32 O/P) (80TE)	10P64353-1 10P64353-2	A
	I/O Option 1	A - RTD B - CLIO X	(32 I/P & 24 O/P) (80TE)	10P64374-1 10P64374-2	A
	I/O Option 2	B - CLIO	(32 I/P & 32 O/P) (80TE)	10P64377-1 10P64377-2	A
	I/O Option 4	B - CLIO	(40 I/P & 24 O/P) (80TE)	10P64355-1 10P64355-2	A
	I/O Option 7	B - CLIO	(48 I/P & 16 O/P) (80TE)	10P64356-1 10P64356-2	A
P645	I/O Option H	X	(16 I/P & 16 O/P) (60TE)	10P64501-1 10P64501-2	F K
			High Z REF for 5 bias input transformer differential same principle applies to wire High Z REF for T2, T3, T4 & T5	10P64501-3	H
	I/O Option H	A - RTD	(16 I/P & 16 O/P + RTD) (60TE)	10P64502-1 10P64502-2	F J

Model	CORTEC Option*	Product Specific Option	Input/Output Options and Case Size Compatibility	Drawing-Sheet	Issue
P645	I/O Option H	B - CLIO	(16 I/P & 16 O/P + CLIO) (60TE)	10P64503-1 10P64503-2	F J
	I/O Option J	X	(16 I/P & 16 O/P + 4 High-Speed High-Break) (60TE)	10P64528-1 10P64528-2	A
	I/O Option J	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 16 O/P + 4 High-Speed High-Break) (80TE)	10P64538-1 10P64538-2	A
	I/O Option K	X	(16 I/P & 21 O/P) (60TE)	10P64529-1 10P64529-2	A
	I/O Option K	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 21 O/P) (80TE)	10P64542-1 10P64542-2	A
	I/O Option L	X	(16 I/P & 24 O/P) (60TE)	10P64505-1 10P64505-2	F J
	I/O Option L	A - RTD B - CLIO C - RTD + CLIO X	(16 I/P & 24 O/P) (80TE)	10P64546-1 10P64546-2	A
	I/O Option P	X	(20 I/P & 20 O/P) (60TE)	10P64530-1 10P64530-2	A
	I/O Option P	A - RTD B - CLIO C - RTD + CLIO X	(20 I/P & 20 O/P) (80TE)	10P64550-1 10P64550-2	A
	I/O Option S	X	(24 I/P & 16 O/P) (60TE)	10P64504-1 10P64504-2	F J
	I/O Option S	A - RTD B - CLIO C - RTD + CLIO X	(24 I/P & 16 O/P) (80TE)	10P64558-1 10P64558-2	A
	I/O Option T	A - RTD B - CLIO X	(24 I/P & 16 O/P + 8 High-Speed High-Break) (80TE)	10P64559-1 10P64559-2	A
	I/O Option U	A - RTD B - CLIO C - RTD + CLIO X	(24 I/P & 24 O/P) (80TE)	10P64565-1 10P64565-2	A
	I/O Option V	A - RTD B - CLIO X	(24 I/P & 32 O/P) (80TE)	10P64566-1 10P64566-2	A
	I/O Option 1	A - RTD B - CLIO X	(32 I/P & 24 O/P) (80TE)	10P64573-1 10P64573-2	A
	I/O Option 2	B - CLIO	(32 I/P & 32 O/P) (80TE)	10P64576-1 10P64576-2	A
	I/O Option 4	B - CLIO	(40 I/P & 24 O/P) (80TE)	10P64577-1 10P64577-2	A
	I/O Option 7	B - CLIO	(48 I/P & 16 O/P) (80TE)	10P64578-1 10P64578-2	A

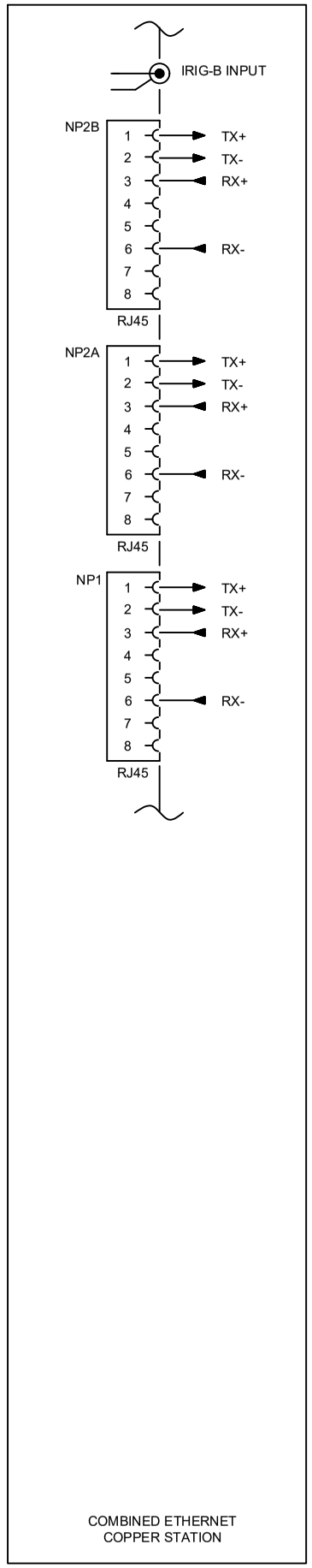
* When selecting the applicable wiring diagram(s), refer to appropriate model's CORTEC.



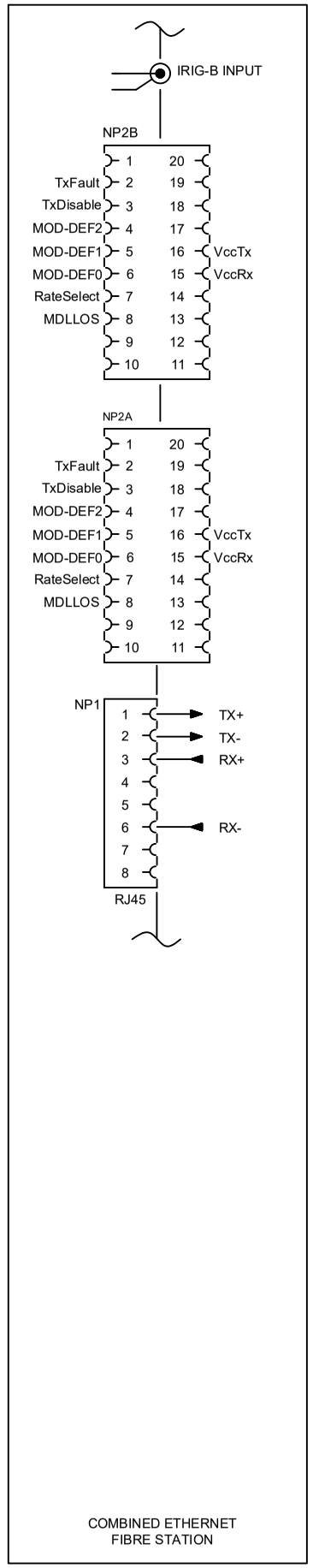
Issue: N	Revision: SHEET 2 ADDED. CID008142.		Title: EXTERNAL CONNECTION DIAGRAM: COMMS OPTIONS MICOM Px40 PLATFORM	
Date: 17/07/2024	Name: S WOOTTON	GE Vernova PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of GE Vernova and contains proprietary information of GE Vernova. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE Vernova, and that the information shall be used by the recipient only as approved expressly by GE Vernova. This document shall be returned to GE Vernova upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations. © GE Vernova, GE VERNOVA CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10PX4001	Sht: 1 Next Sht: 2
Date:	Chkd:			GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.



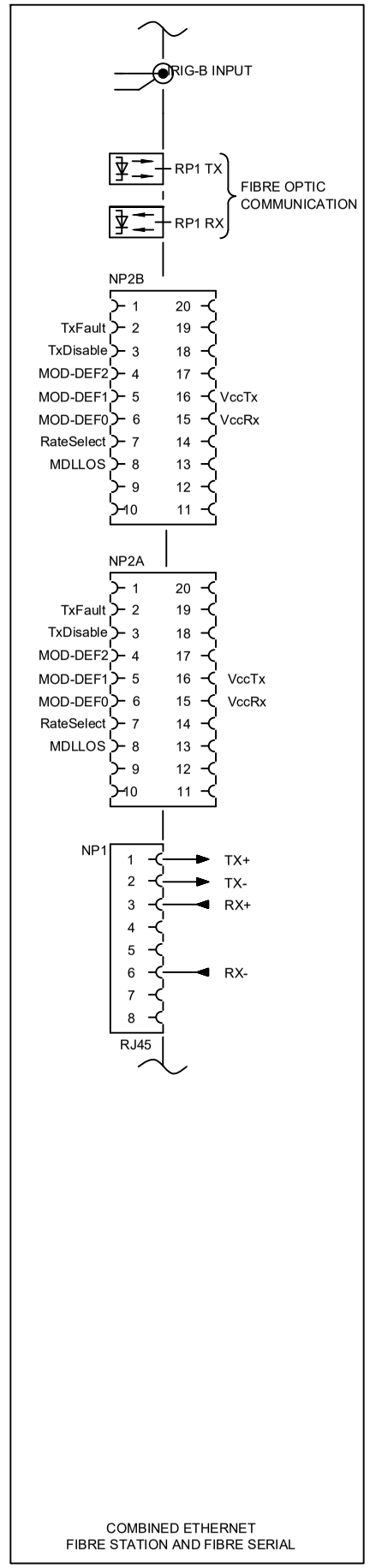
COMBINED ETHERNET
LOW COST OPTION



COMBINED ETHERNET
COPPER STATION

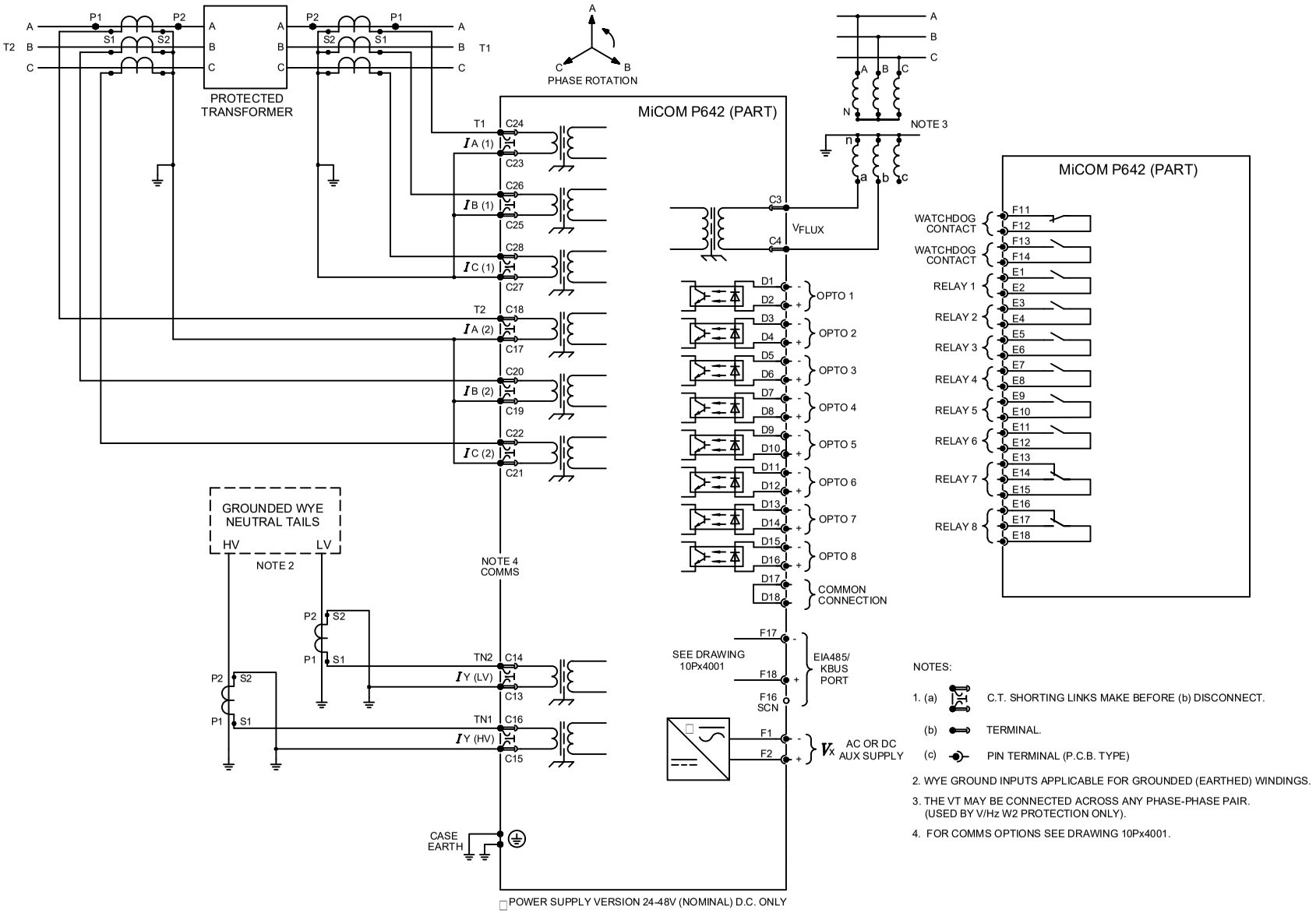


COMBINED ETHERNET
FIBRE STATION



COMBINED ETHERNET
FIBRE STATION AND FIBRE SERIAL

Issue: A	Revision: INITIAL ISSUE. CID008142		Title: EXTERNAL CONNECTION DIAGRAM COMMS OPTIONS MICOM Px40		
Date: 27/06/2024	Name: S WOOTTON		Drg No: 10PX4001	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: L	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (8 I/P & 8 O/P) WITH 1 POLE VT INPUT (40TE)	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64201	Sht: 1
Date:	Chkd:			Next Sht: 2

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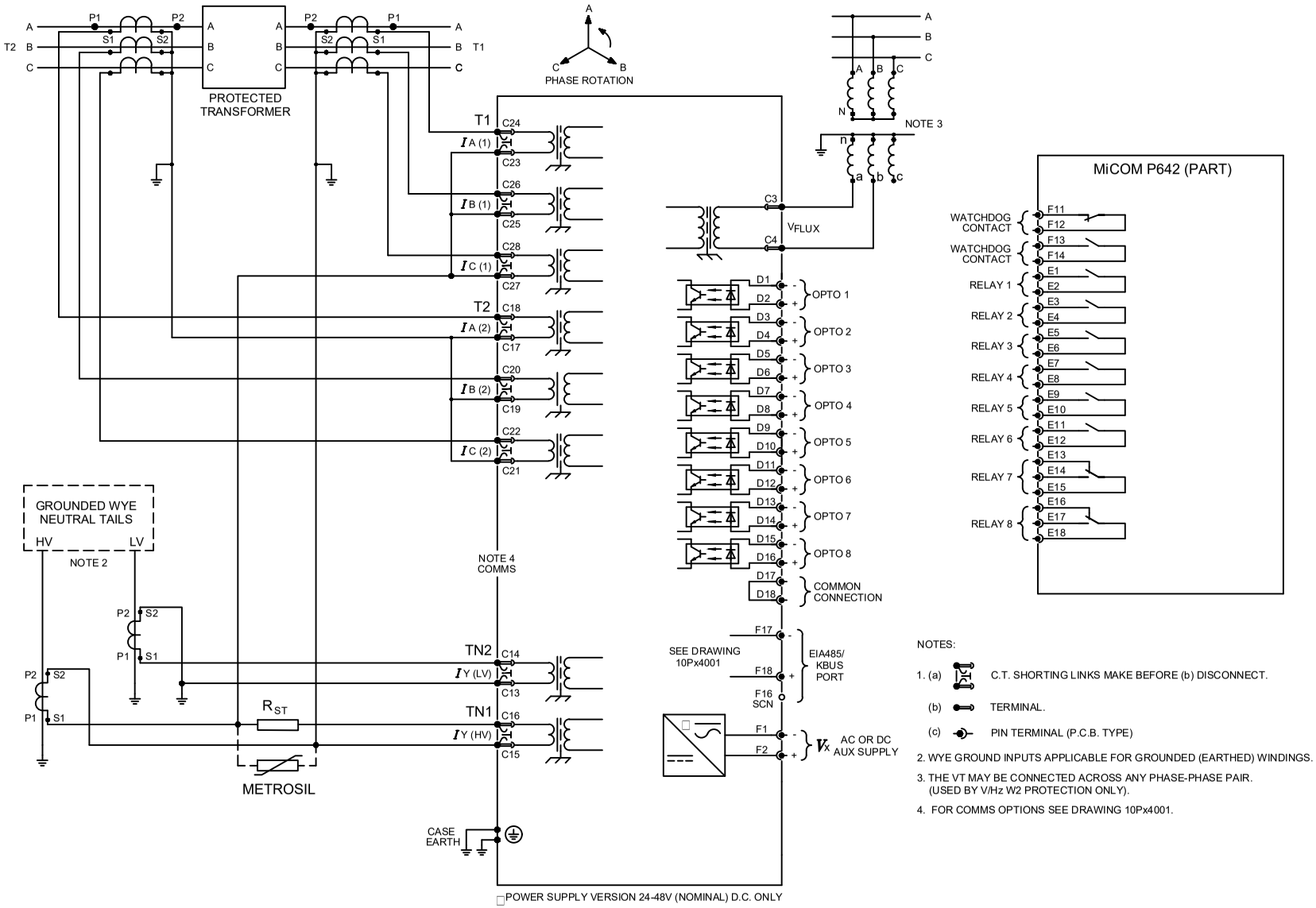
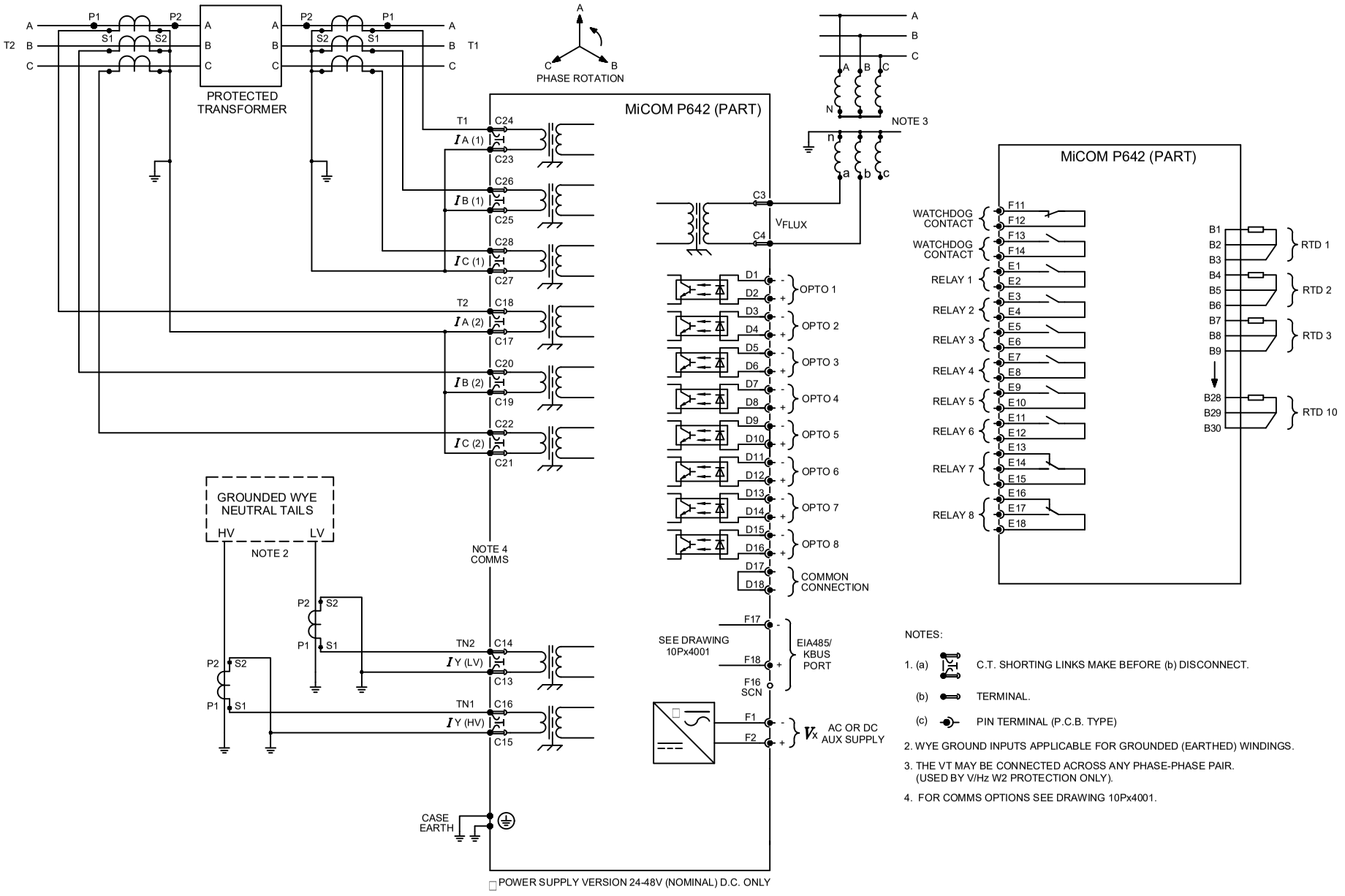


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: H	Revision: CID006234 Outlines updated to GE Format		Title: EXT CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64201	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: K	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (8 I/P & 8 O/P + RTD) WITH 1 POLE VT INPUT (40TE)	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64202	Sht: 1
Date:	Chkd:			Next Sht: -

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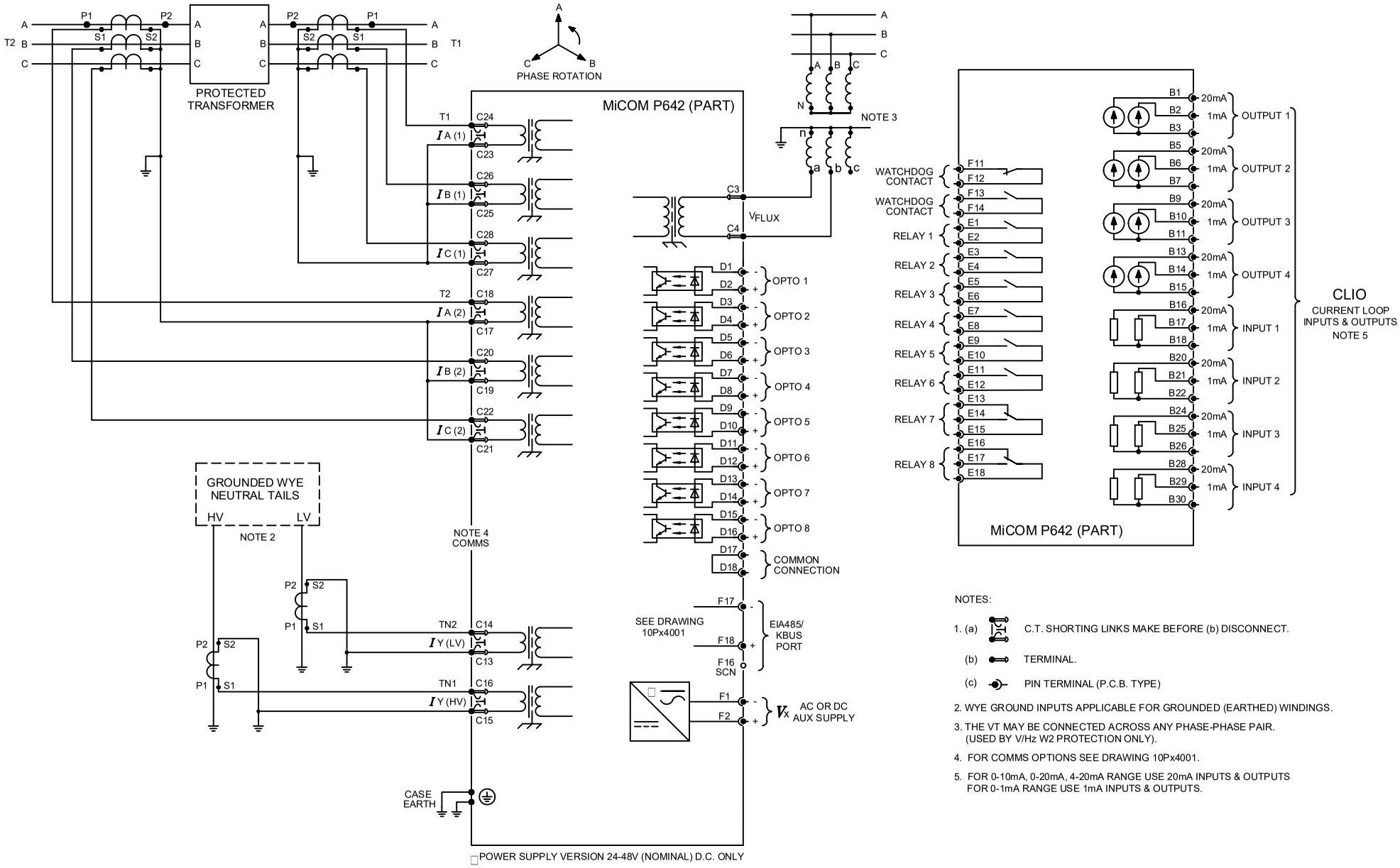

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
5. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: K	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (8 I/P & 8 O/P + CLIO) WITH 1 POLE VT INPUT (40TE)	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64203	Sht: 1
Date:	Chkd:			Next Sht: -

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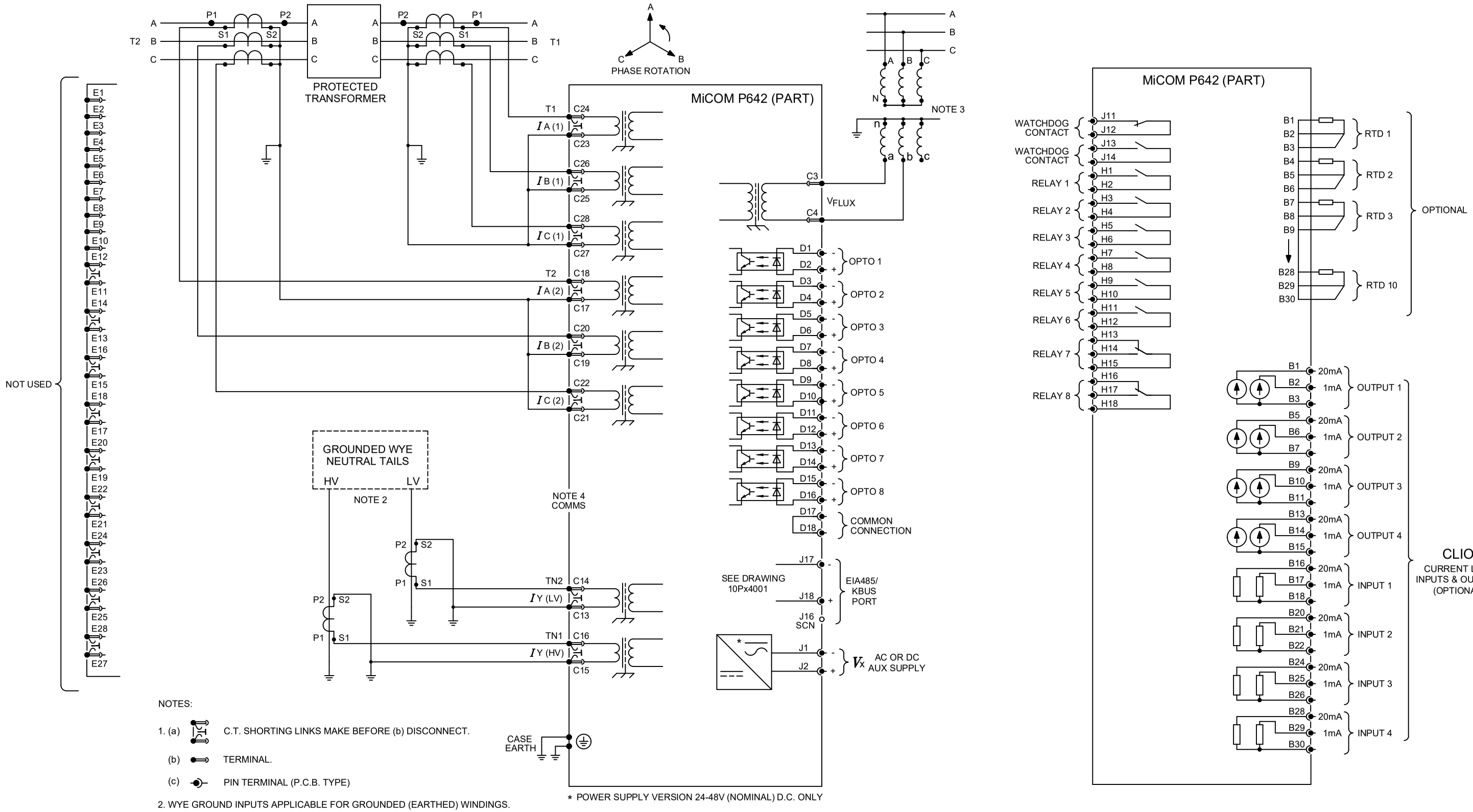

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (8 I/P & 8 O/P) WITH 1 POLE VT INPUT (60TE)	
Date: 01/05/2024	Name: S WOOTTON		Drg No: 10P64217	Sht: 1
Date:	Chkd:			Next Sht: 2

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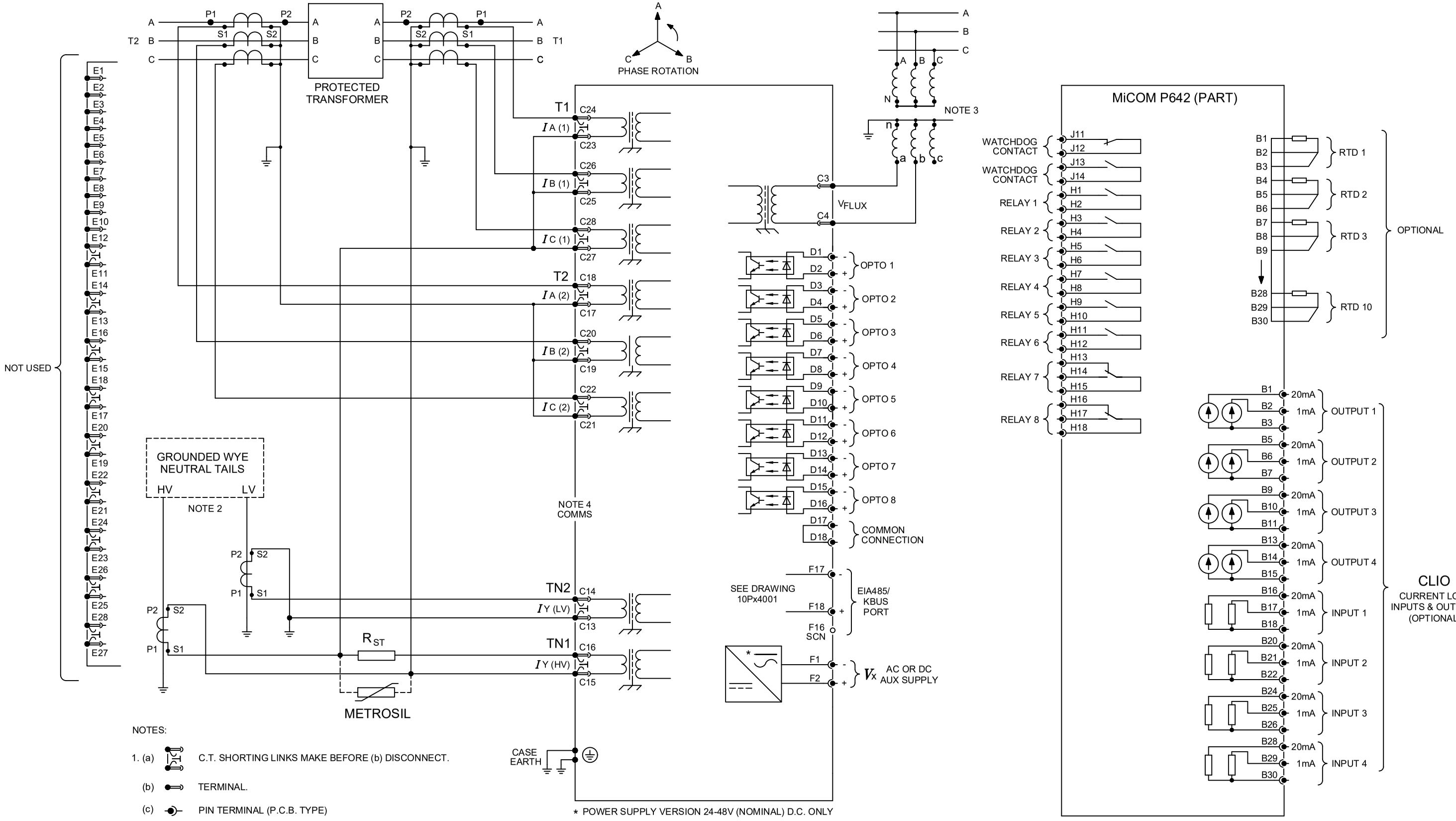
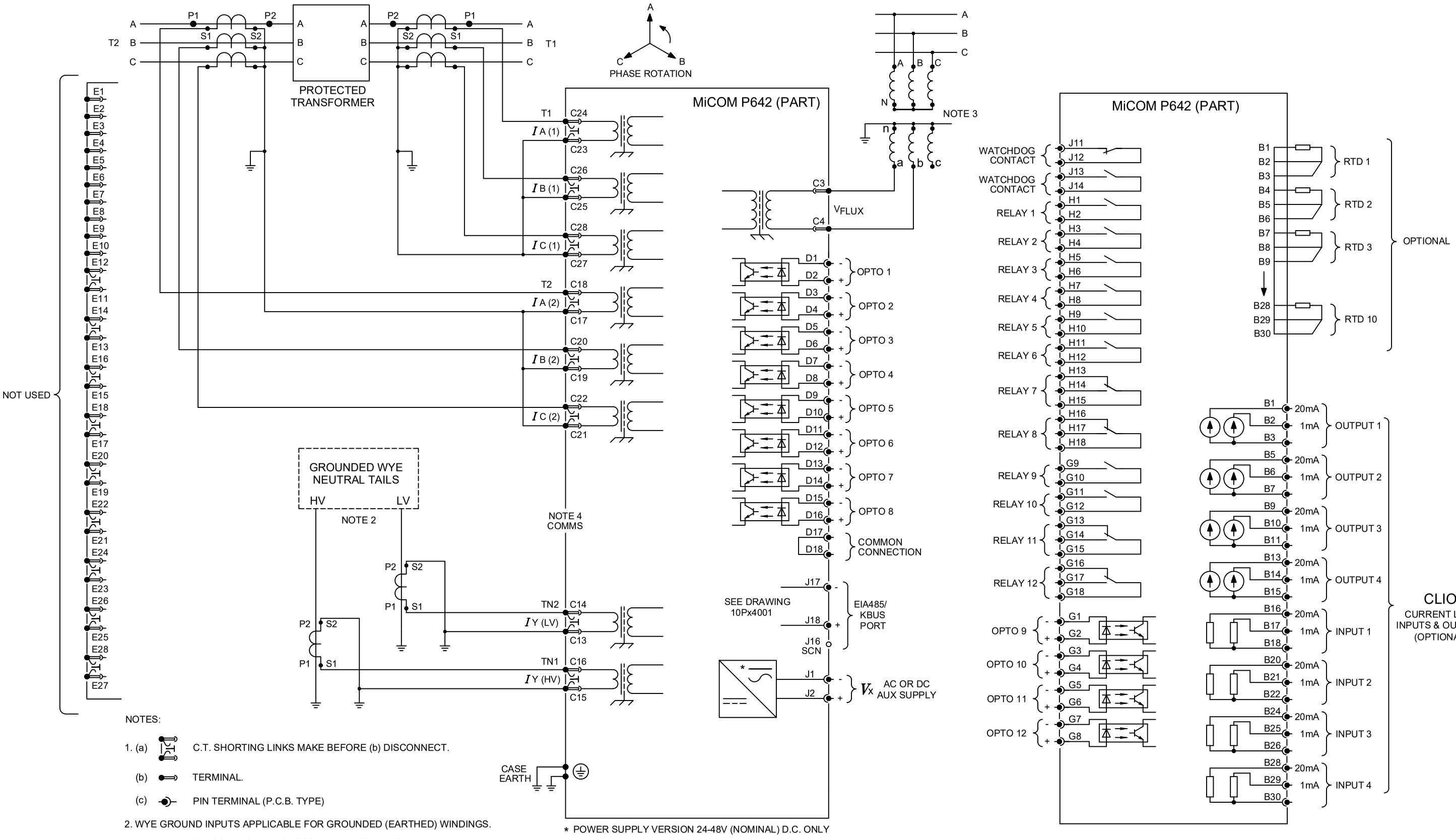


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED		Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (60TE)		
Date: 01/05/2024	Name: S WOOTTON		Drg No: 10P64217	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMNIALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (12 I/P & 12 O/P) WITH 1 POLE VT INPUT (60TE)	
Date: 03/05/2024	Name: S WOOTTON		Drg No: 10P64226	Sht: 1
Date:	Chkd:			Next Sht: 2

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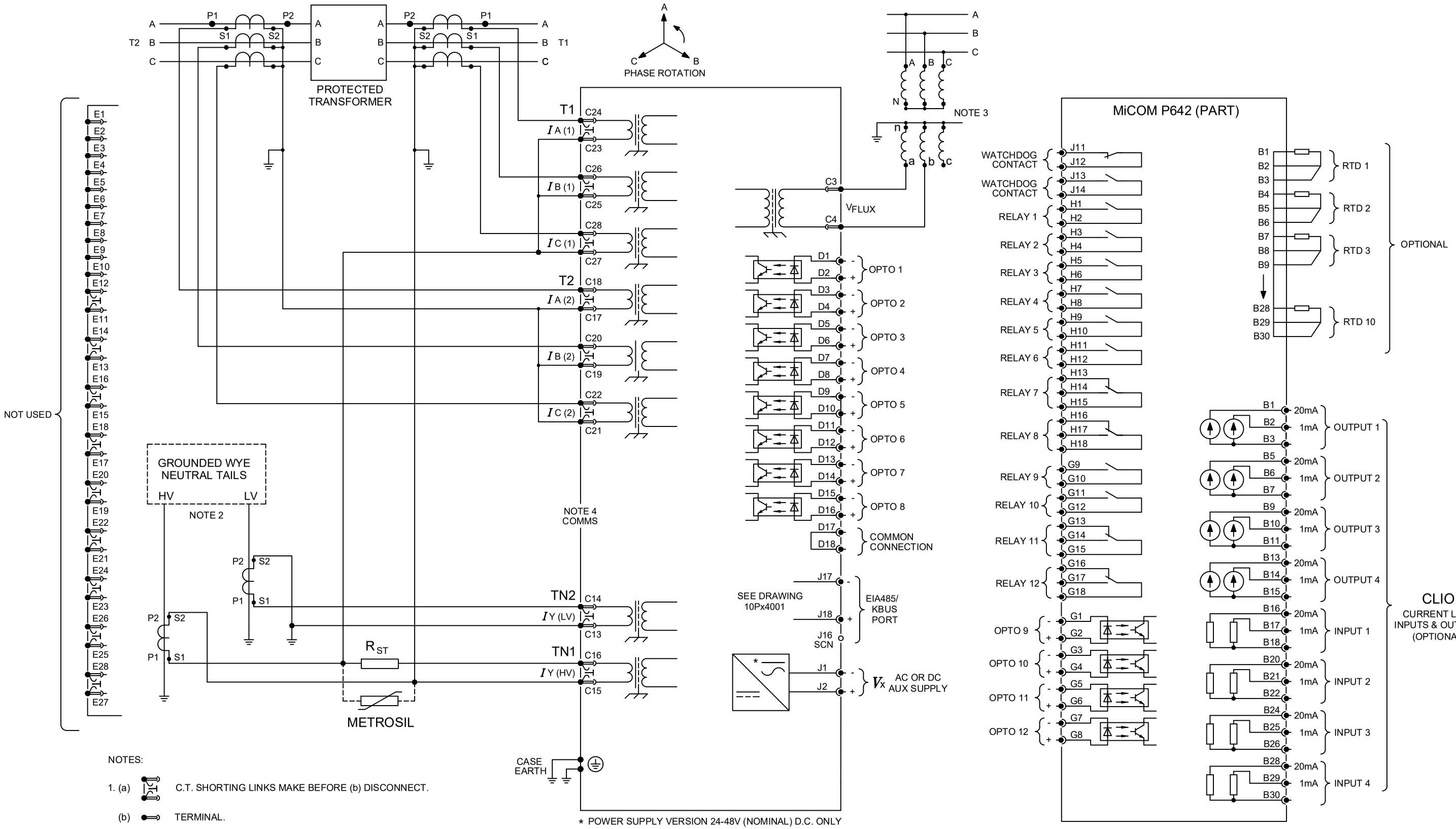

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (60TE)	
Date: 03/05/2024	Name: S WOOTTON		Drg No: 10P64226	Sht: 2
Date:	Chkd:			Next Sht: -

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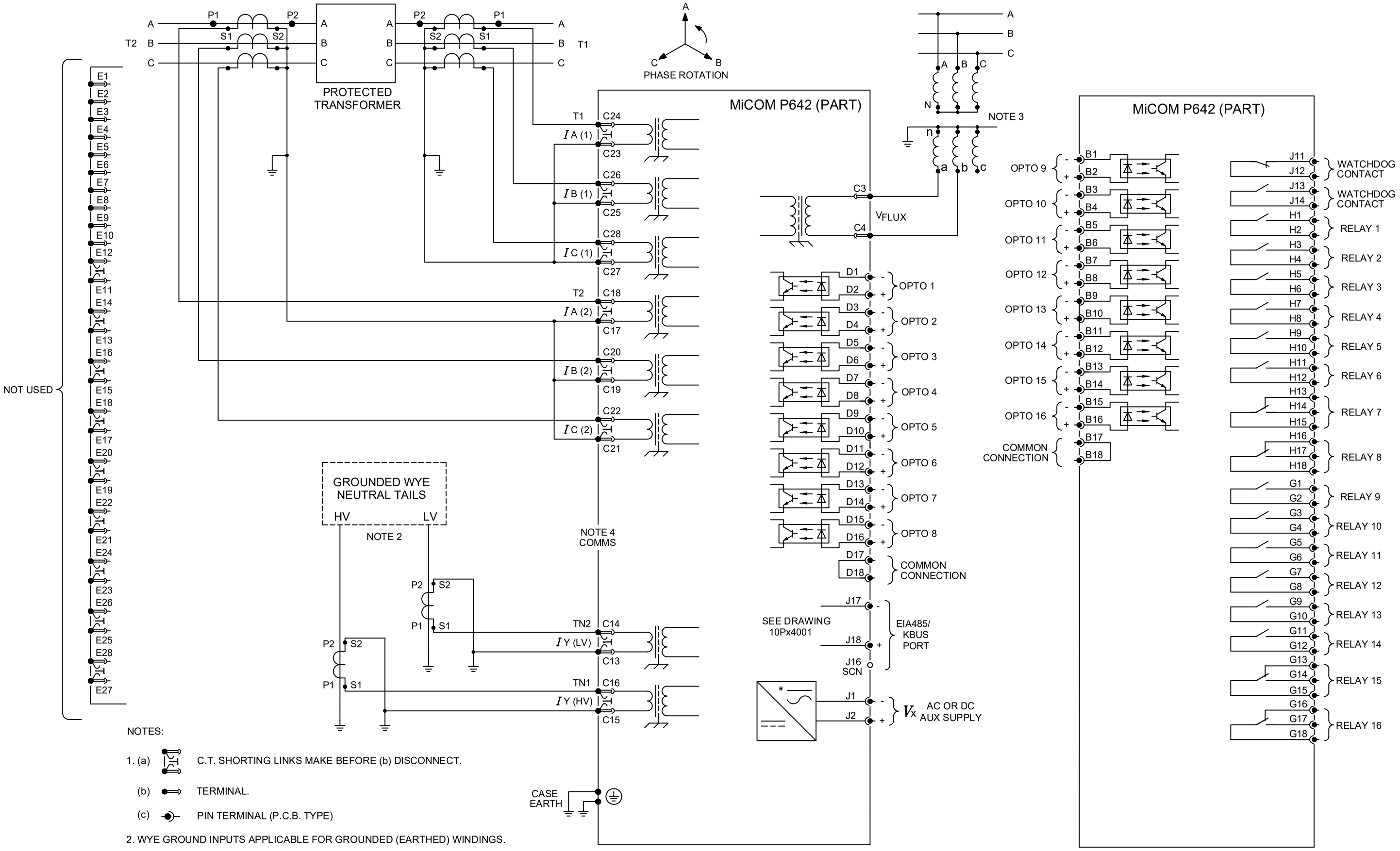

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED..		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P WITH 1 POLE VT INPUT (60TE)	
Date: 07/05/2024	Name: S WOOTTON		Drg No: 10P64233	Sht: 1
Date:	Chkd:			Next Sht: 2

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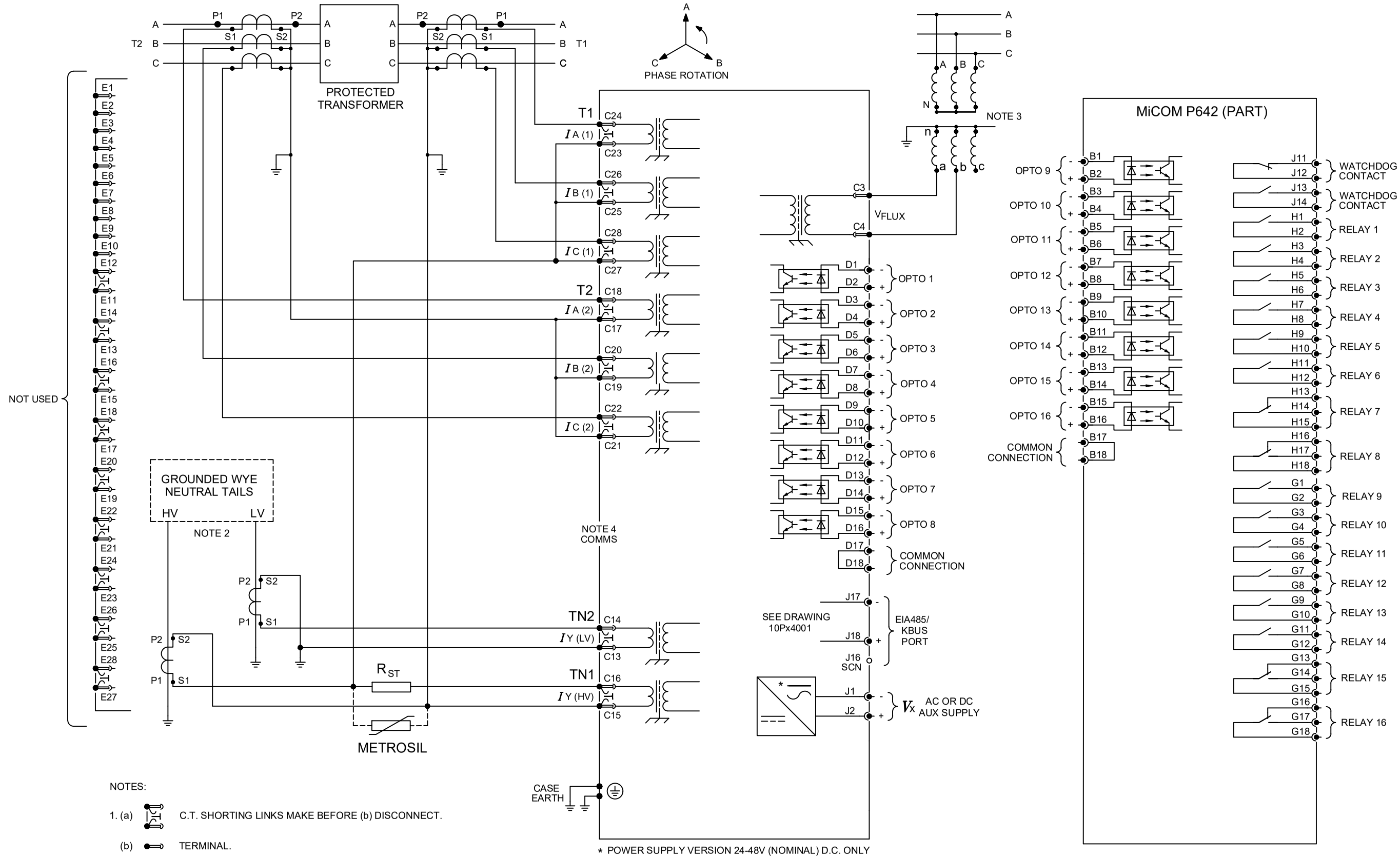
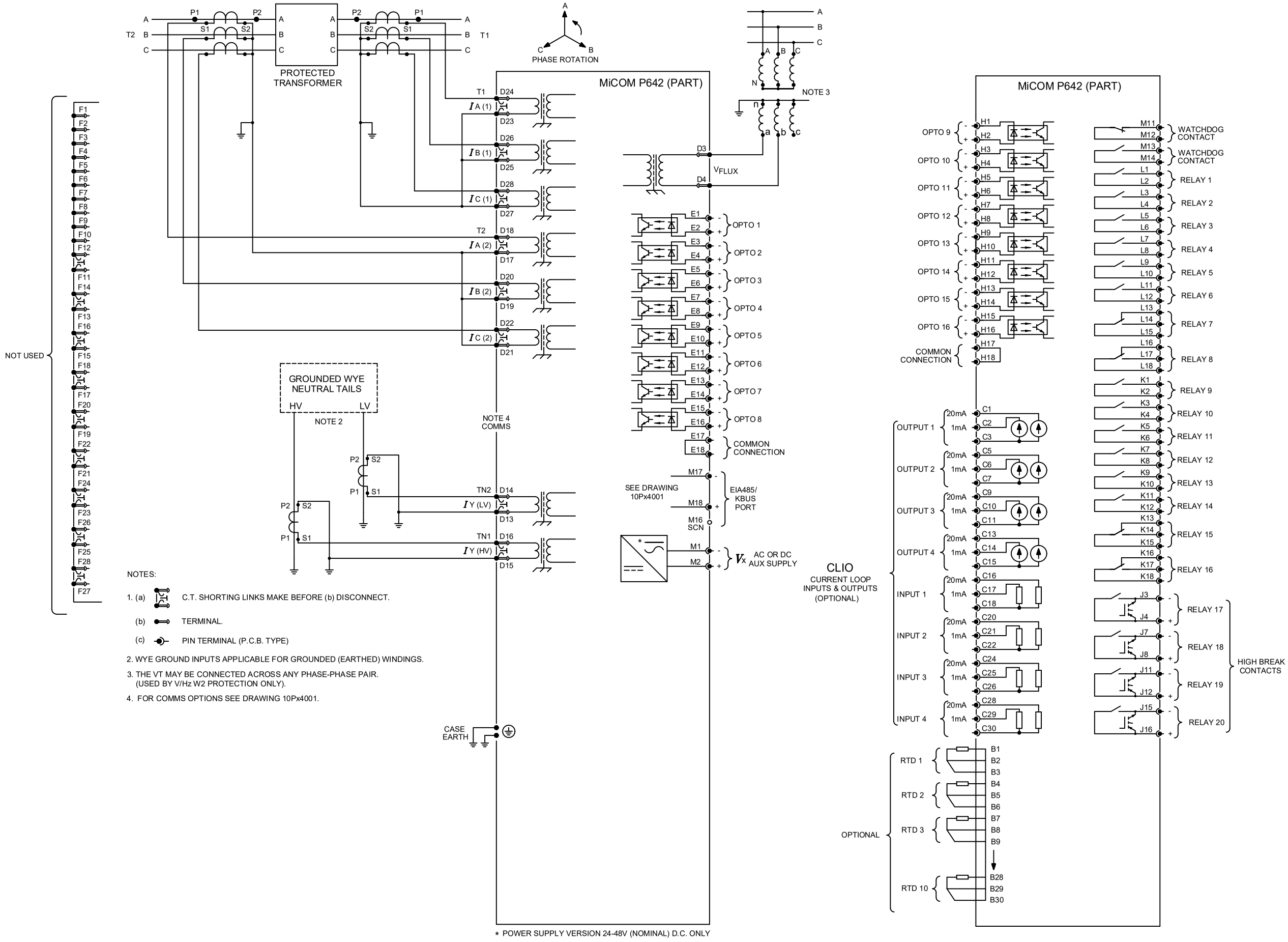


* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXT CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2		
Date: 03/05/2024	Name: S WOOTTON		Drg No: 10P64233	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

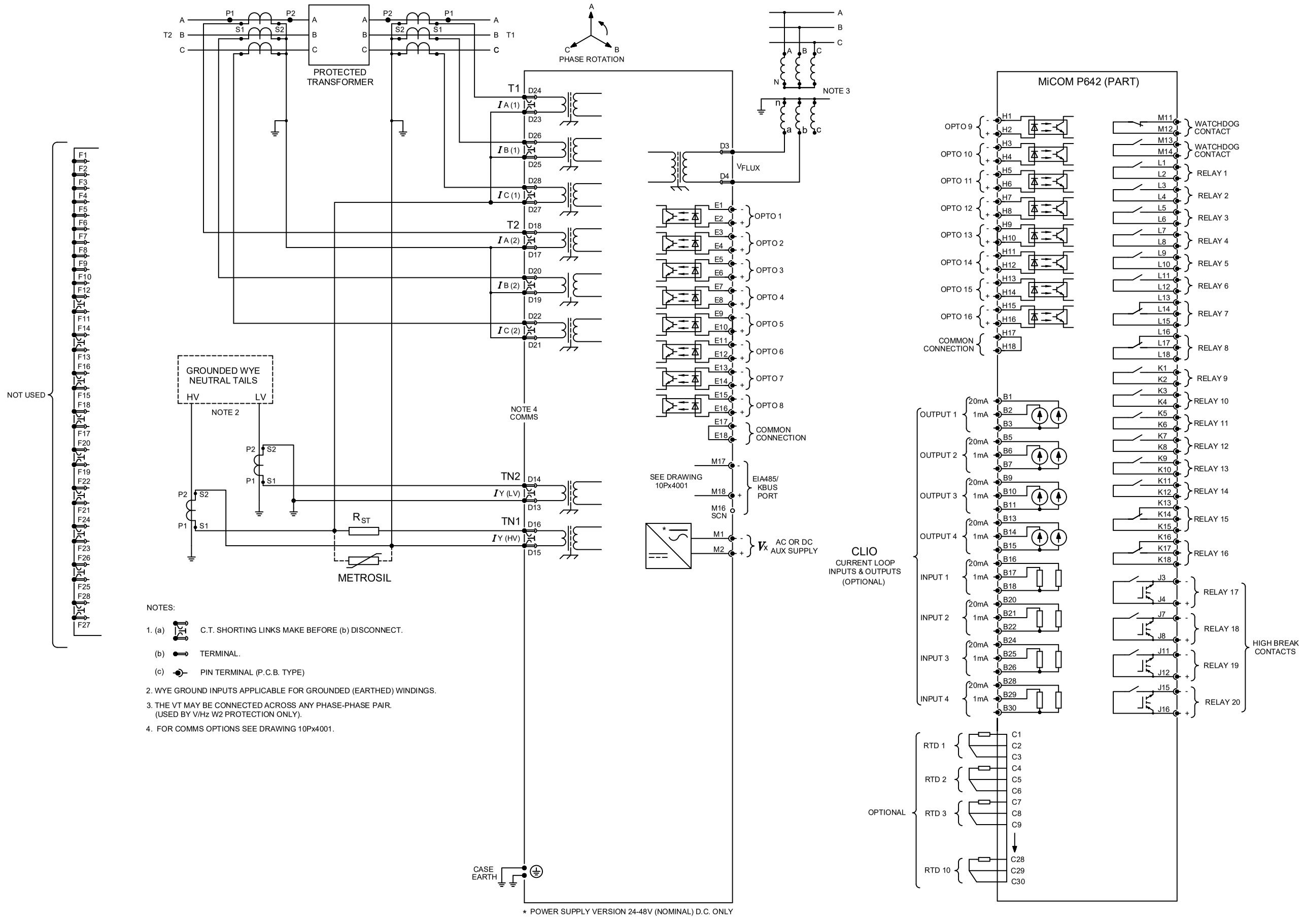


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P + 4 HIGH-SPEED HIGH-BREAK) WITH 1 POLE VT INPUT (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64237	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

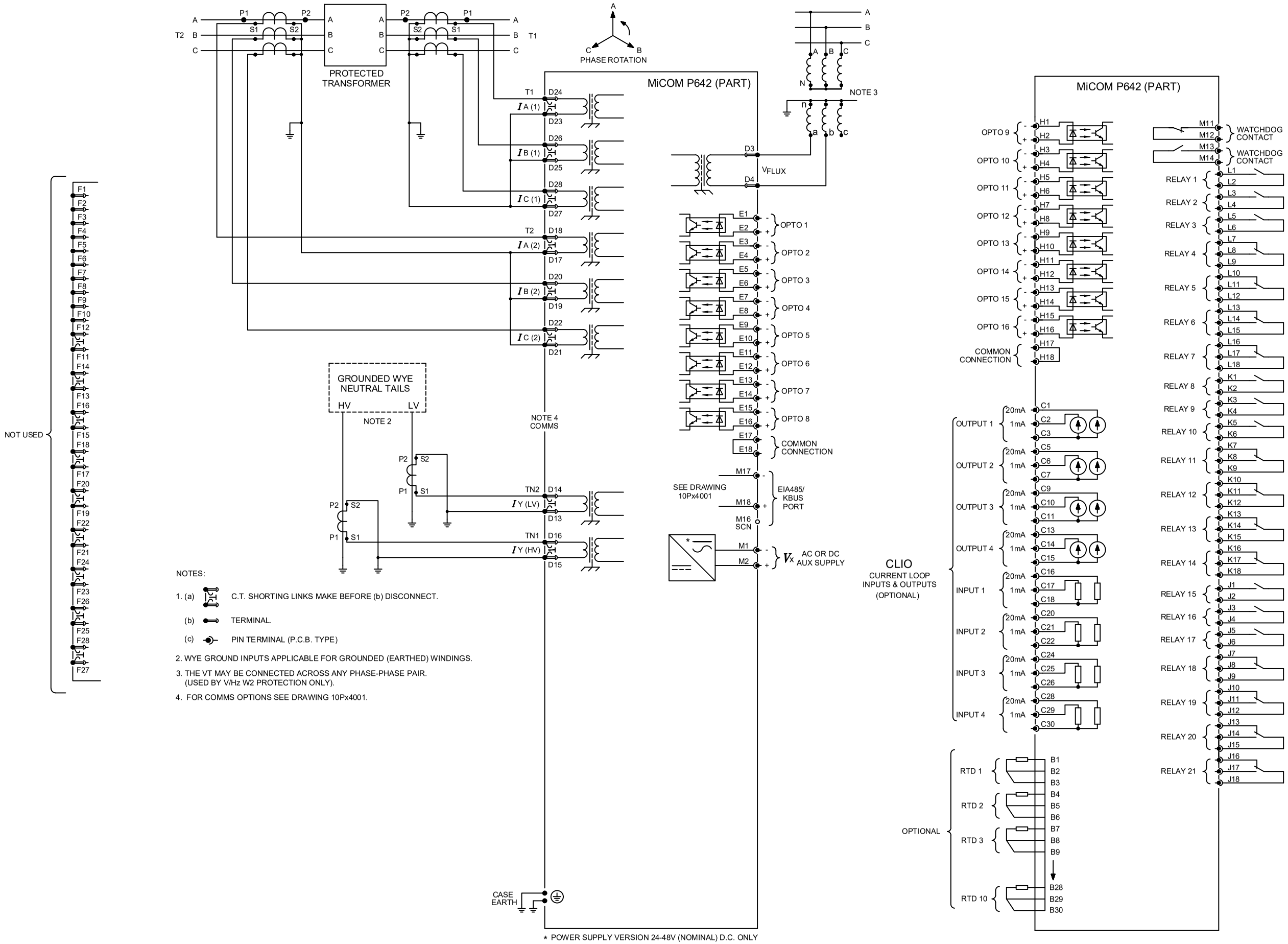


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64237	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title:	EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 21 O/P) WITH 1 POLE VT INPUT (80TE)	
Date: 06/05/2024	Name: S WOOTTON		Drg No:	**10P64241**	Sht: 1
Date:	Chkd:				Next Sht: 2

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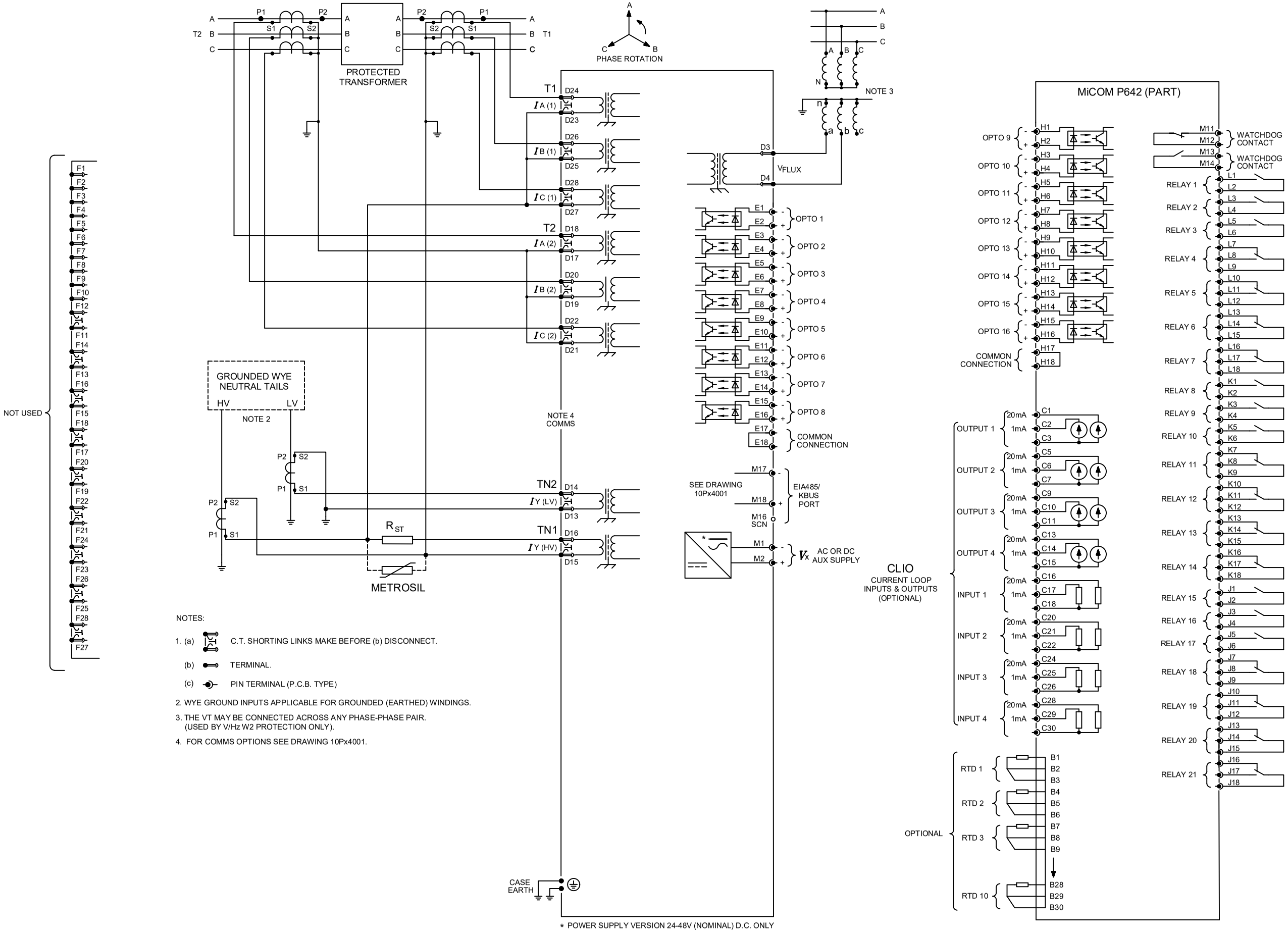
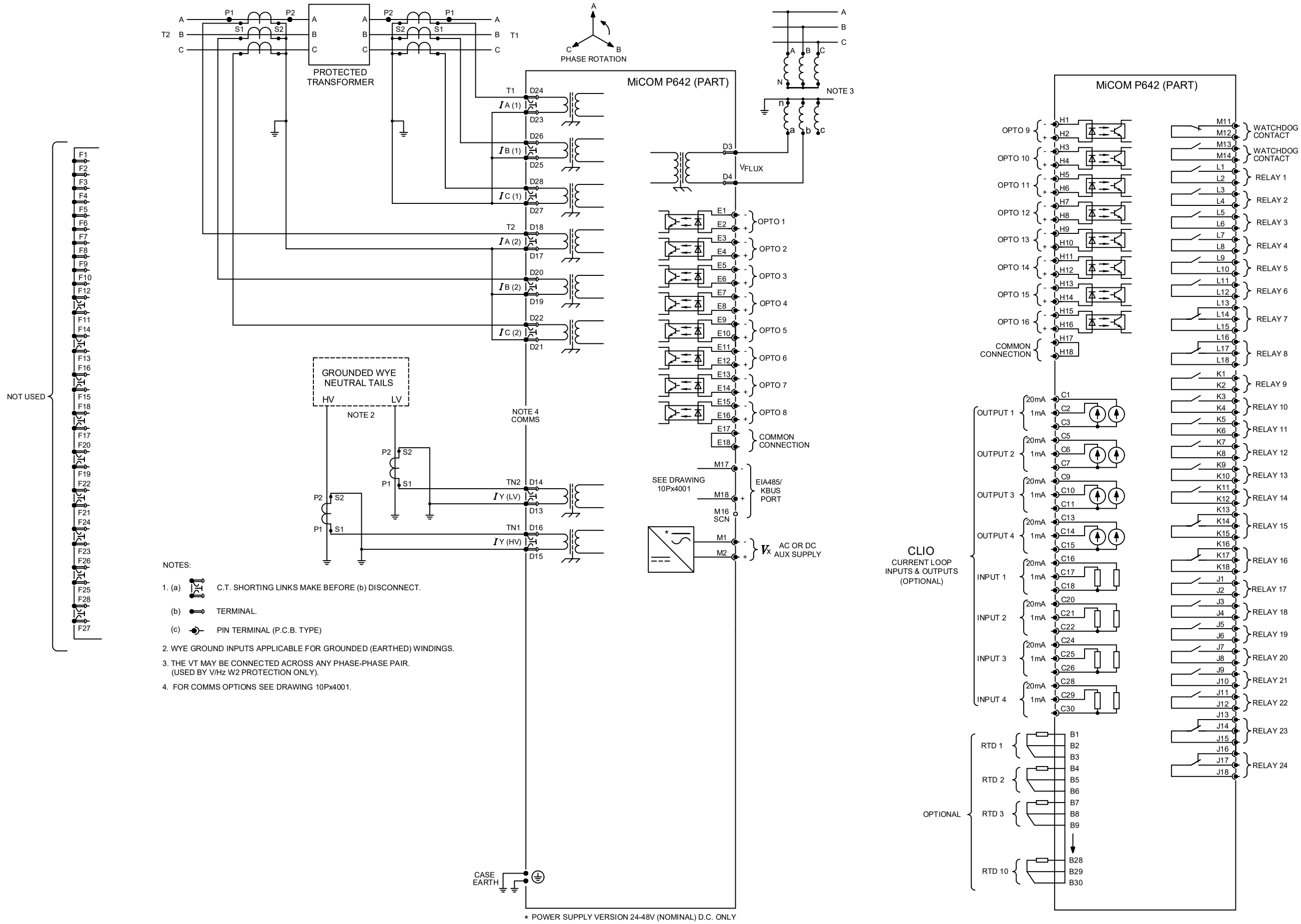


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64241	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 24 O/P) WITH 1 POLE VT INPUT (80TE)	
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64245	Sht: 1
Date:	Chkd:			Next Sht: 2

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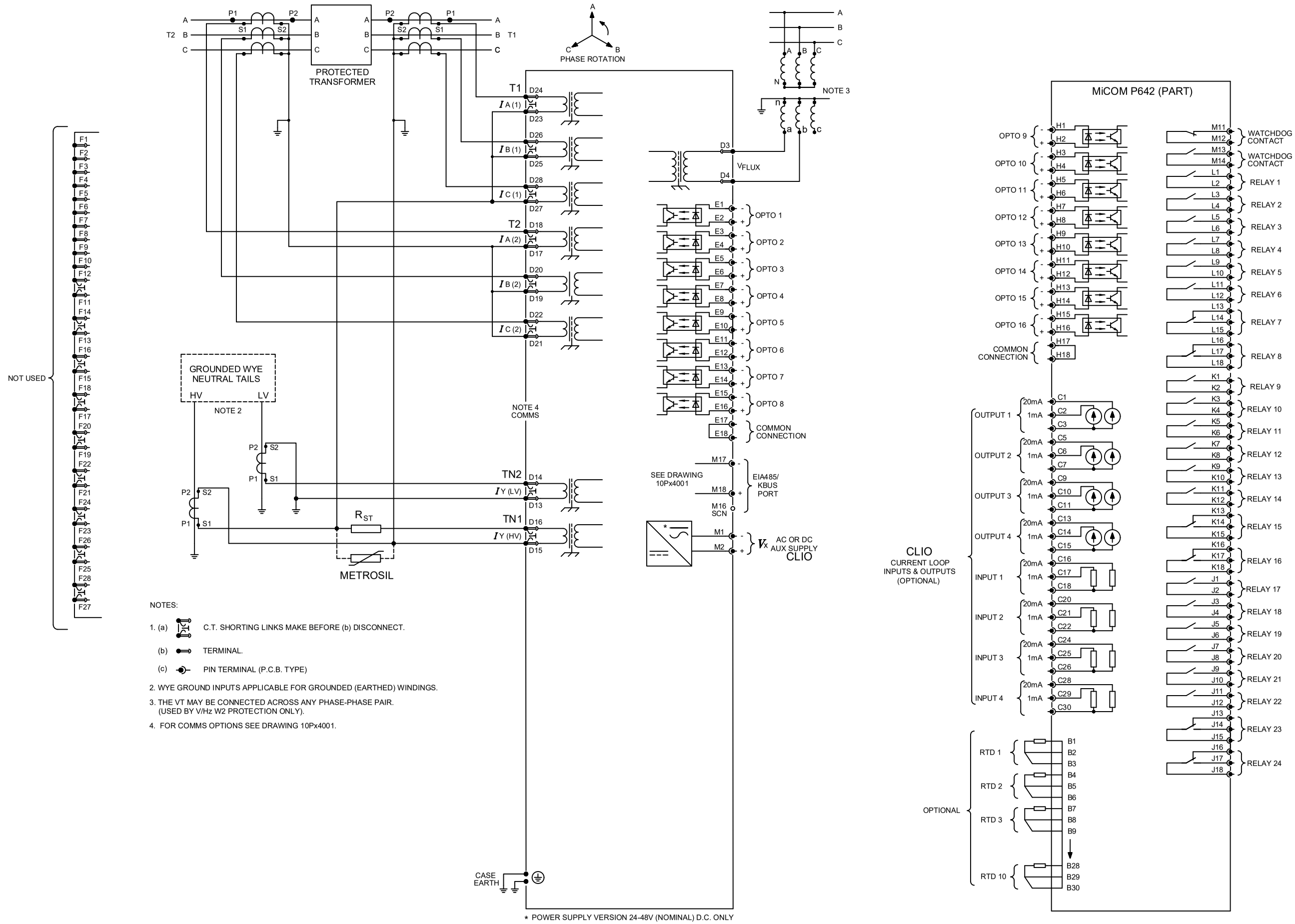

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.	Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)	
Date: 06/05/2024	Name: S WOOTTON	Drg No: **10P64245**	Sht: 2
Date:	Chkd:		Next Sht: -

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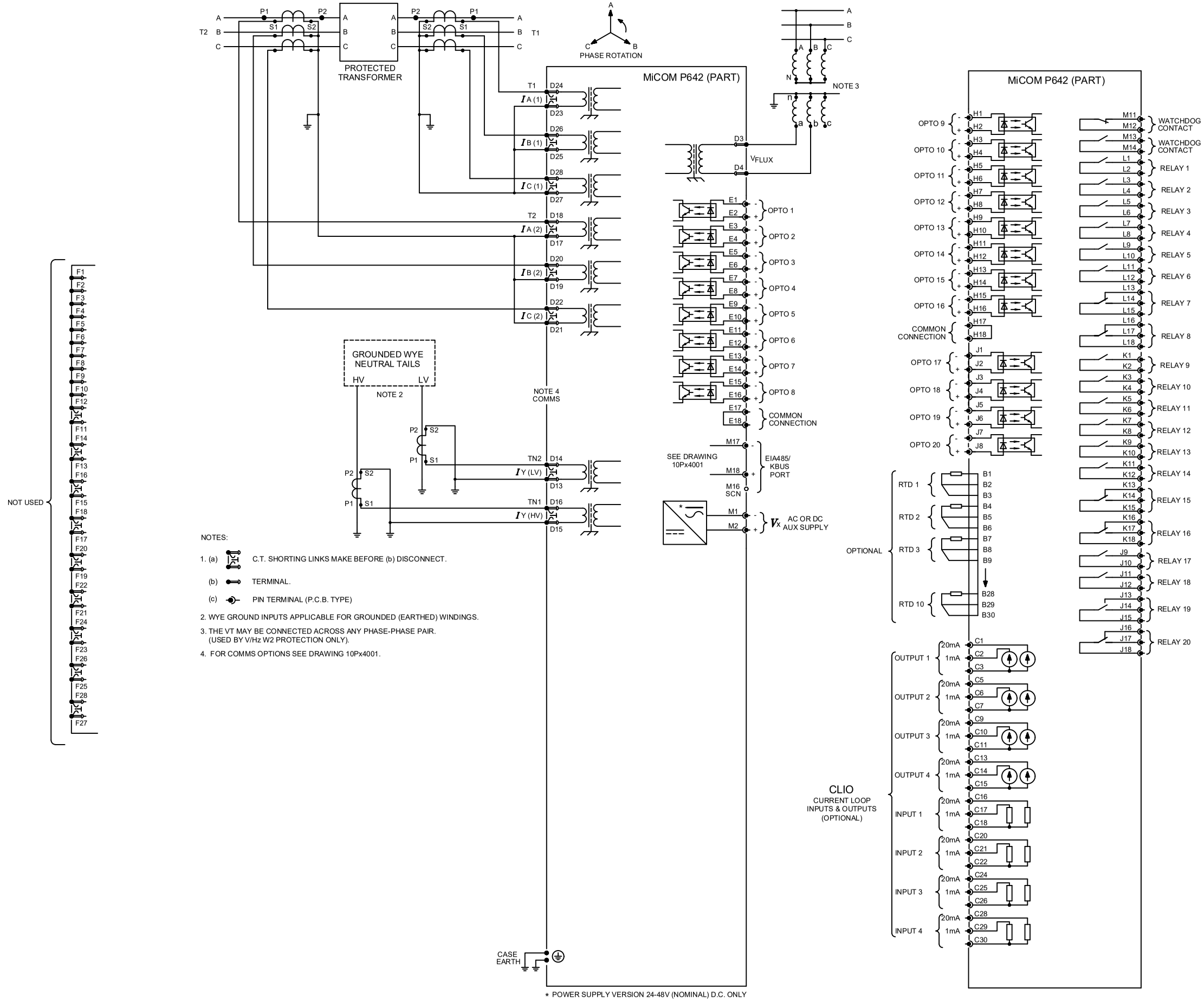

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (20 I/P & 20 O/P) WITH 1 POLE VT INPUT (80TE)	
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64249	Sht: 1
Date:	Chkd:			Next Sht: 2

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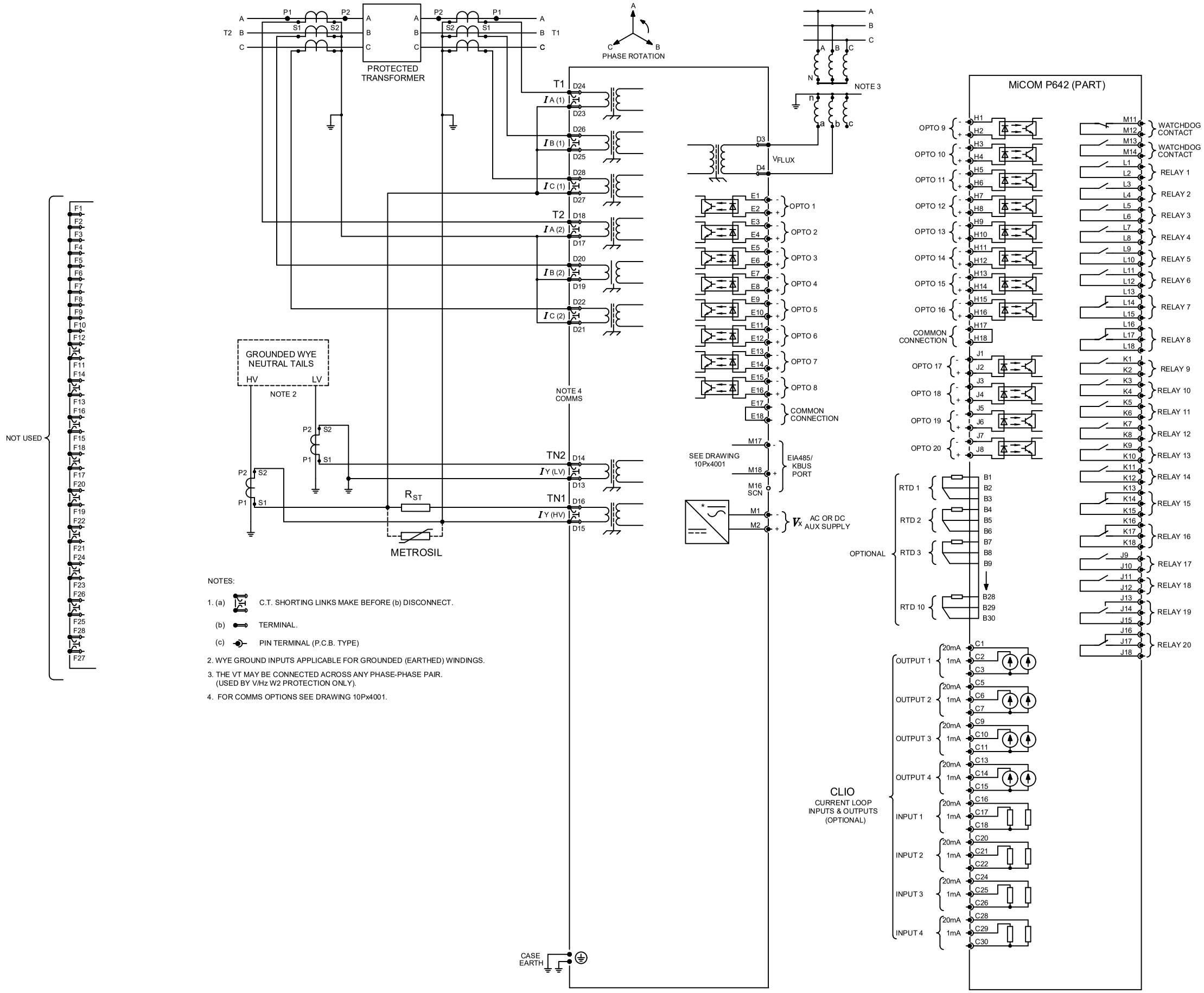

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title:	CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)	
Date: 06/05/2024	Name: S WOOTTON		Drg No:	10P64249	Sht: 2
Date:	Chkd:				Next Sht: -

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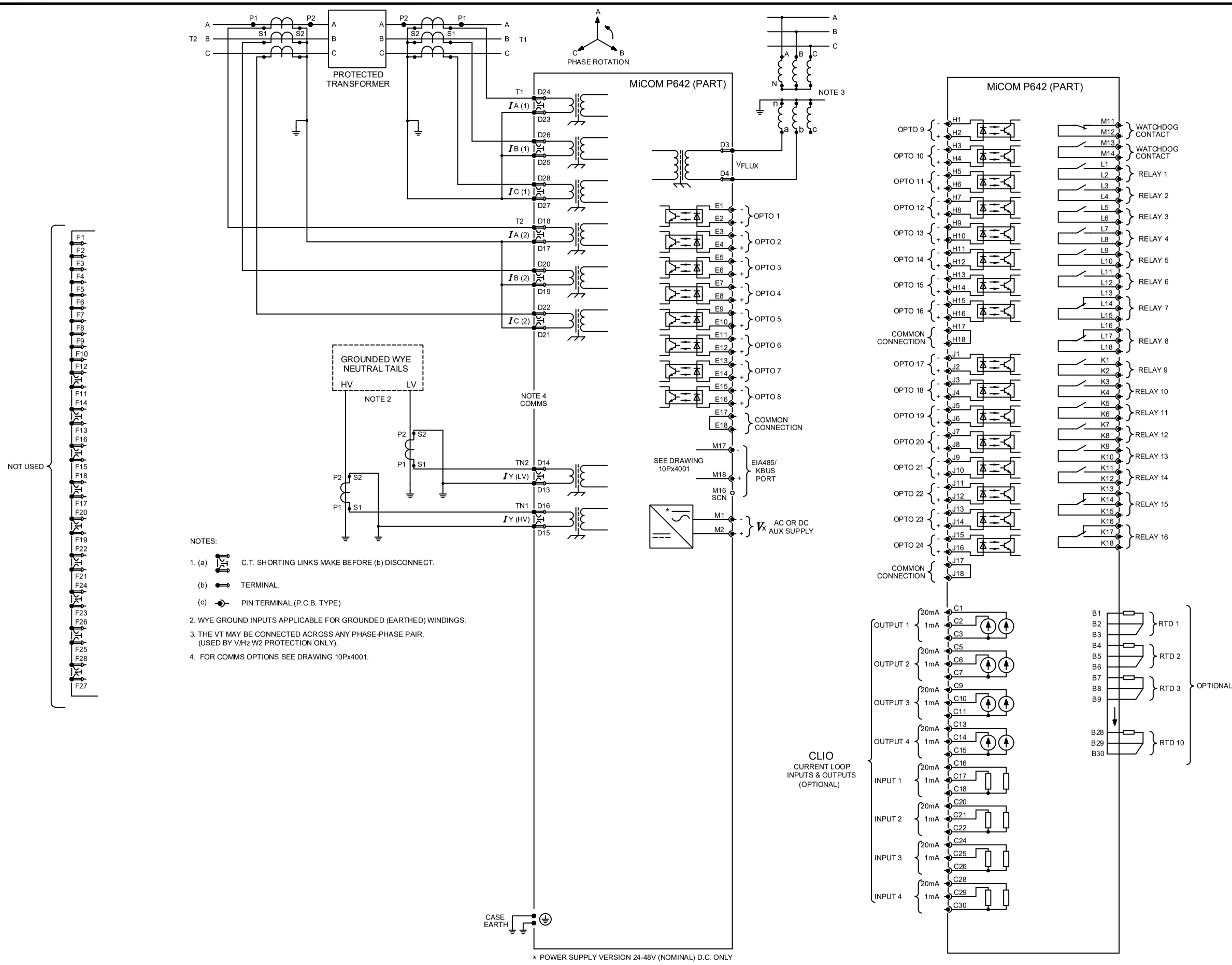
ST16 1WT, UK.



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/P & 16 O/P) WITH 1 POLE VT INPUT (80TE)	
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64257	Sht: 1
Date:	Chkd:			Next Sht: 2

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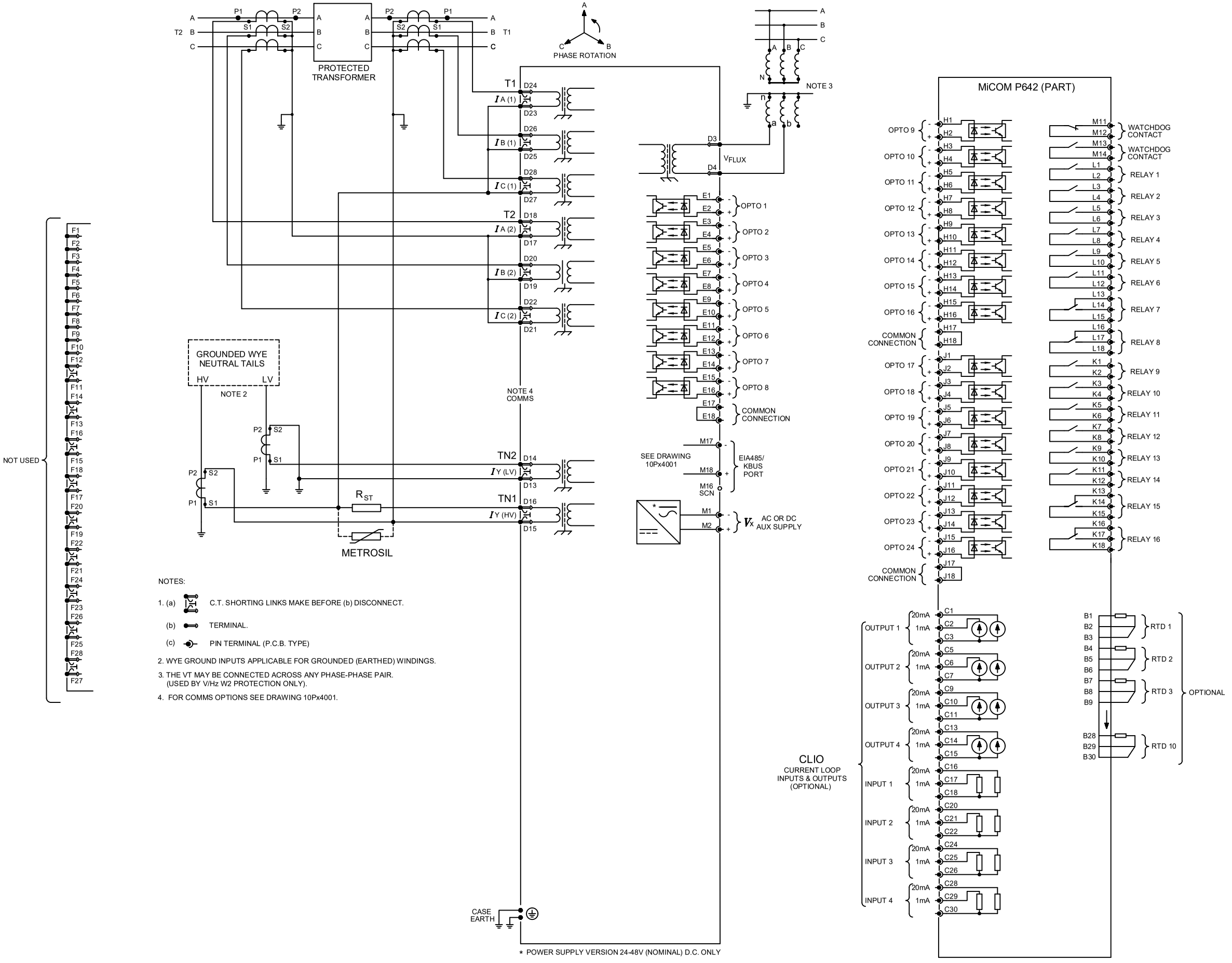
ST16 1WT, UK.



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title:	CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64257	Sht: 2
Date:	Chkd:			Next Sht: -

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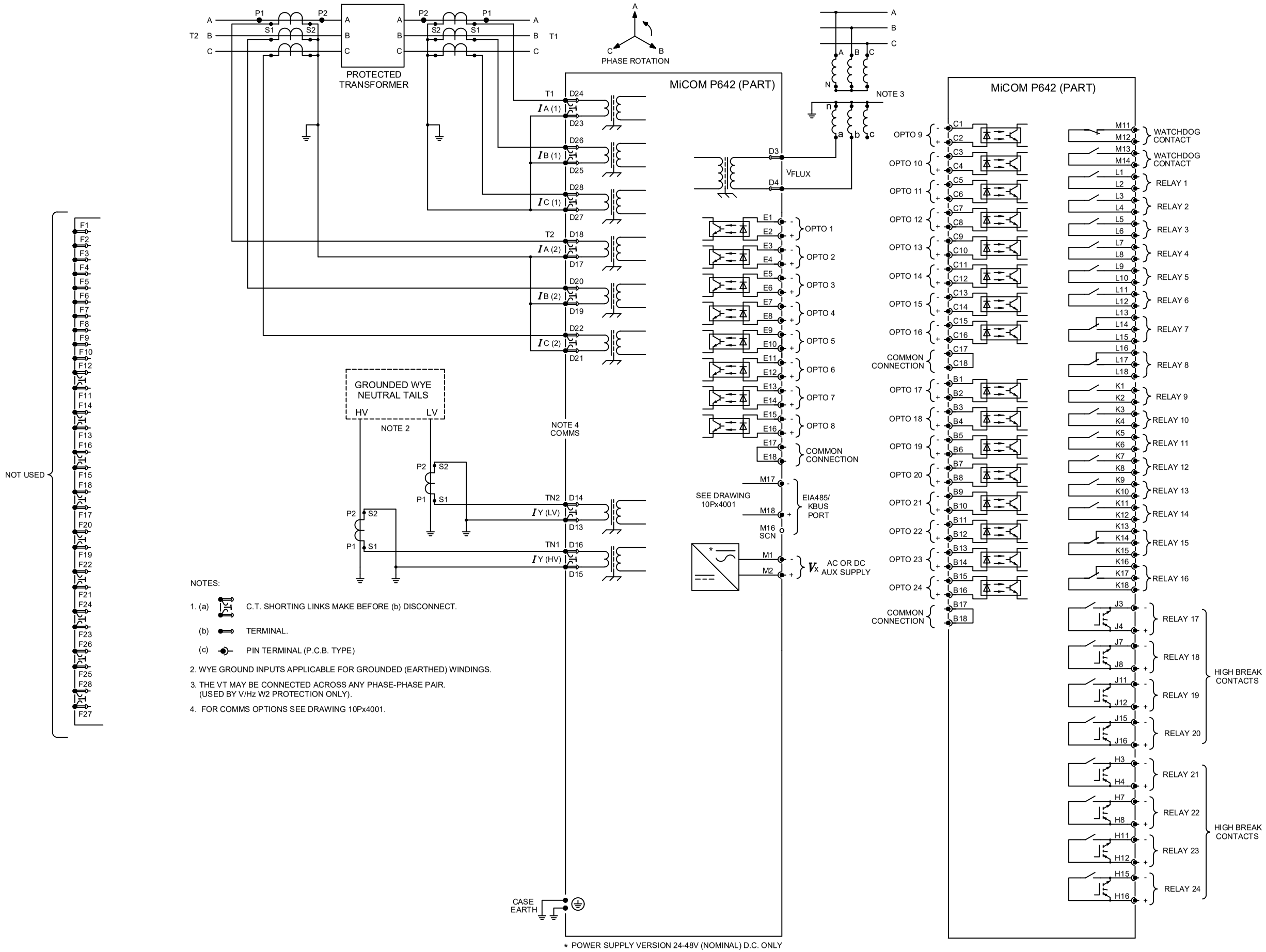

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: C	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P + 8 HS HB) WITH 1 POLE VT INPUT (80TE)	
Date: 07/05/2024	Name: S WOOTTON		Drg No: 10P64258	Sht: 1
Date:	Chkd:			Next Sht: 2

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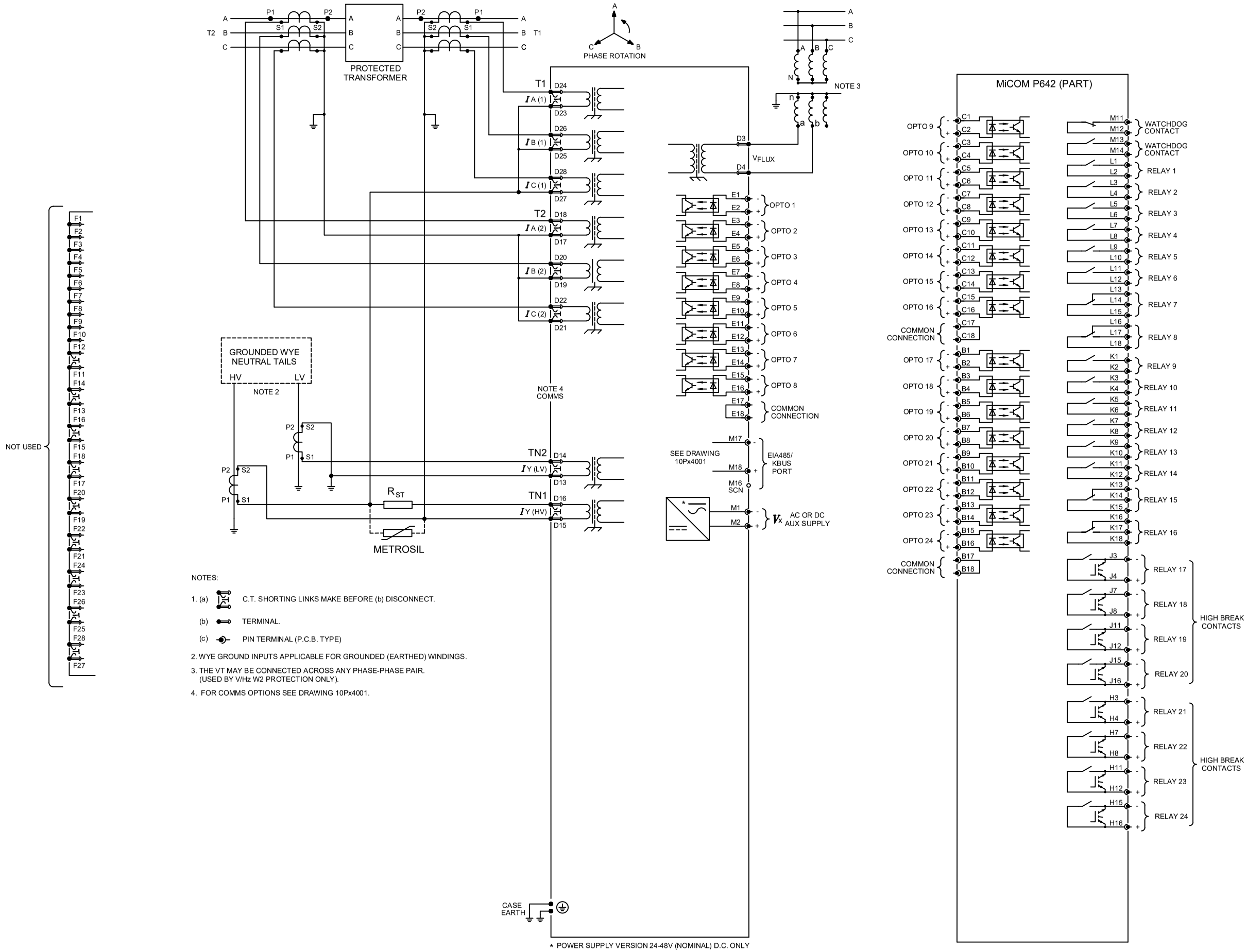

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: C	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXT CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)	
Date: 08/05/2024	Name: S WOOTTON		Drg No: 10P64258	Sht: 2
Date:	Chkd:			Next Sht: -

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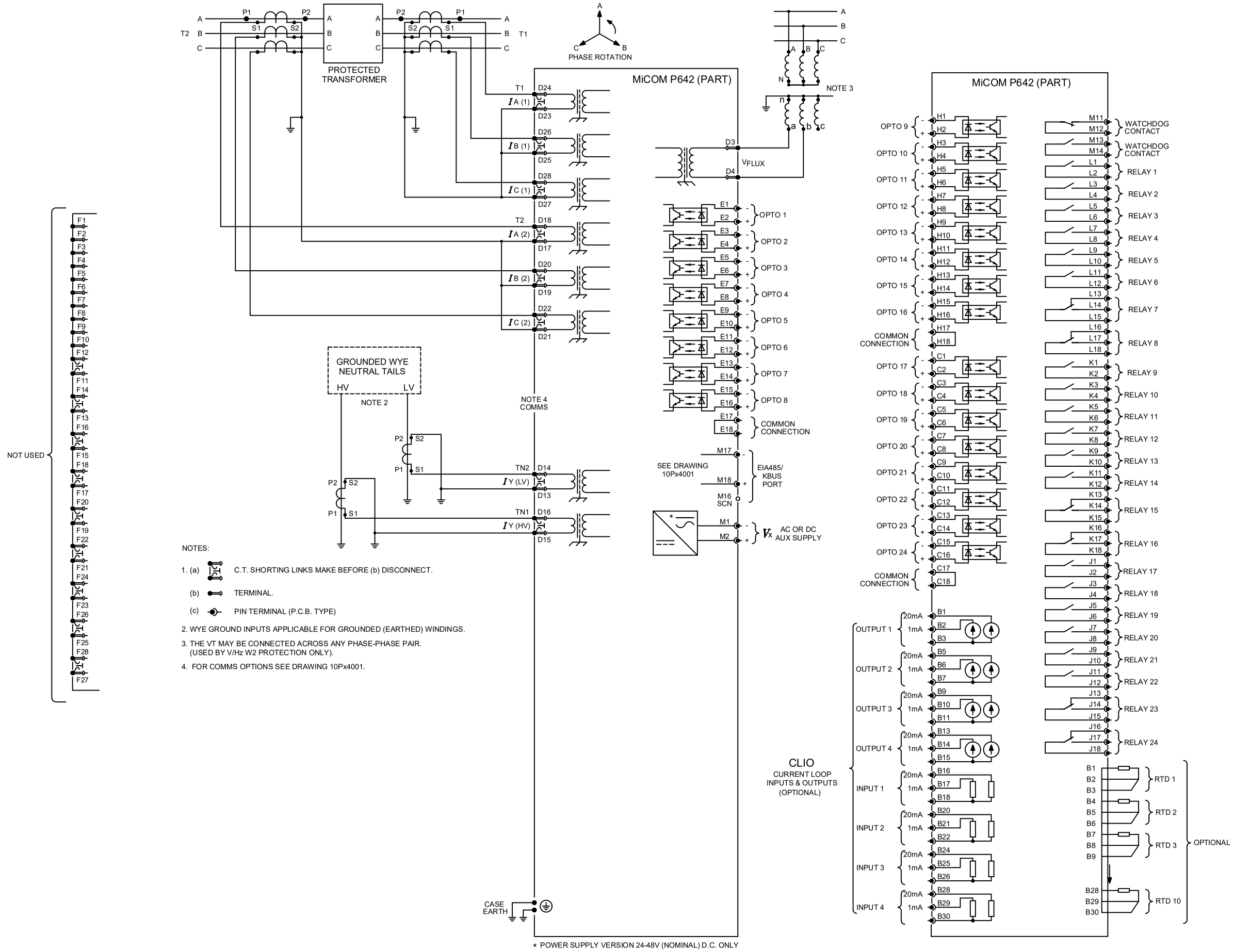
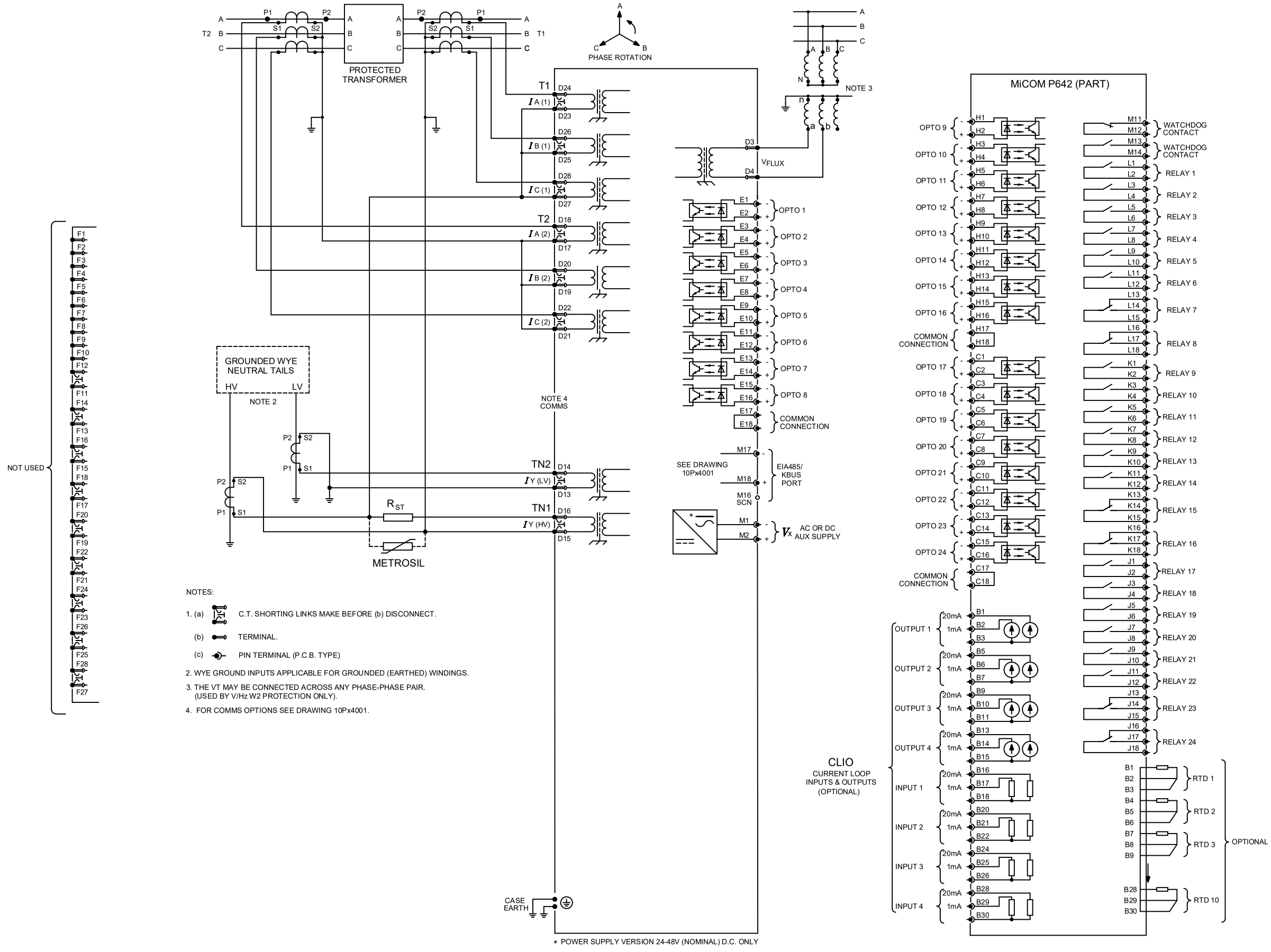


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/P & 24 O/P WITH 1 POLE VT INPUT (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64259	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

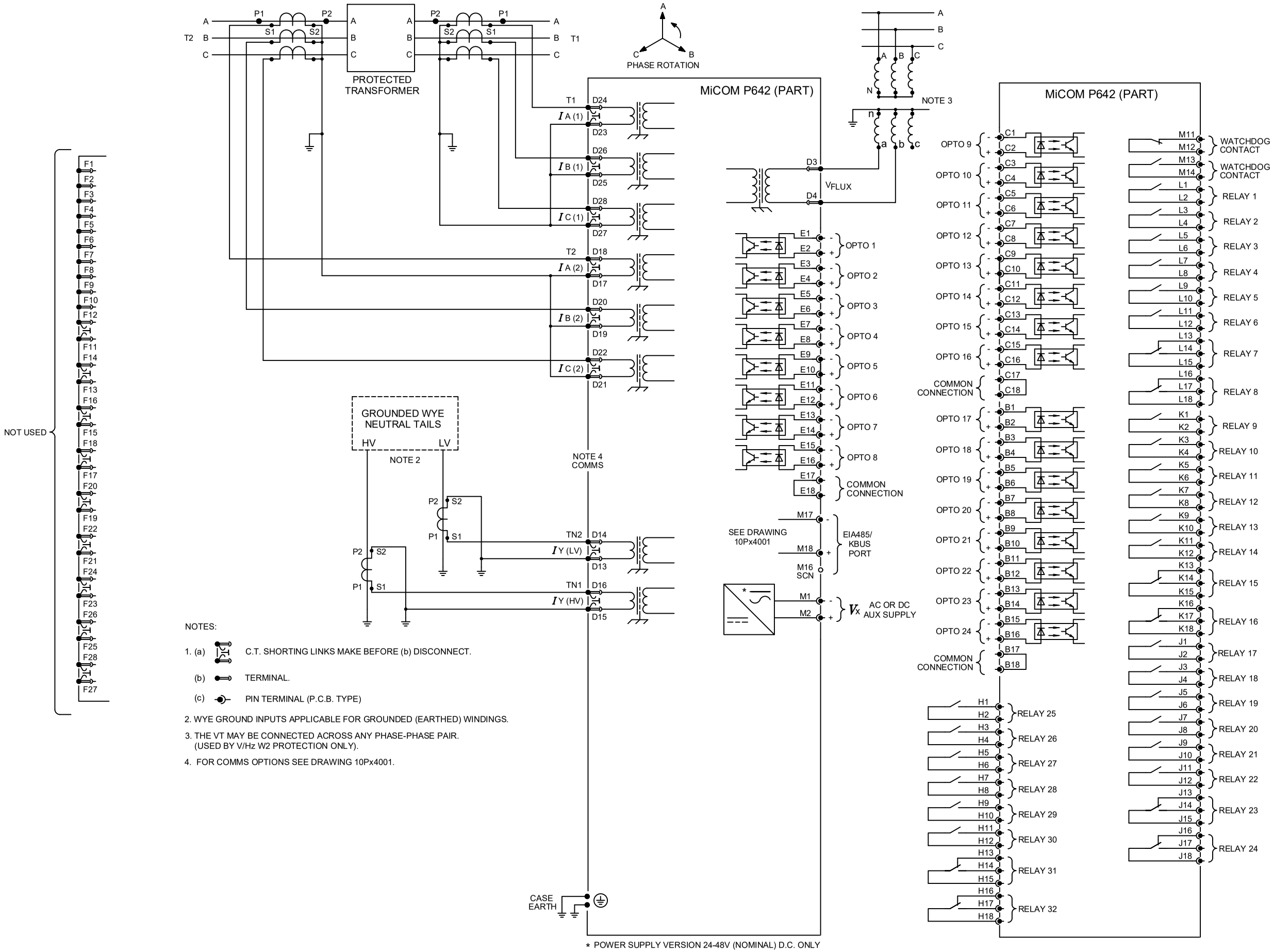


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64259	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

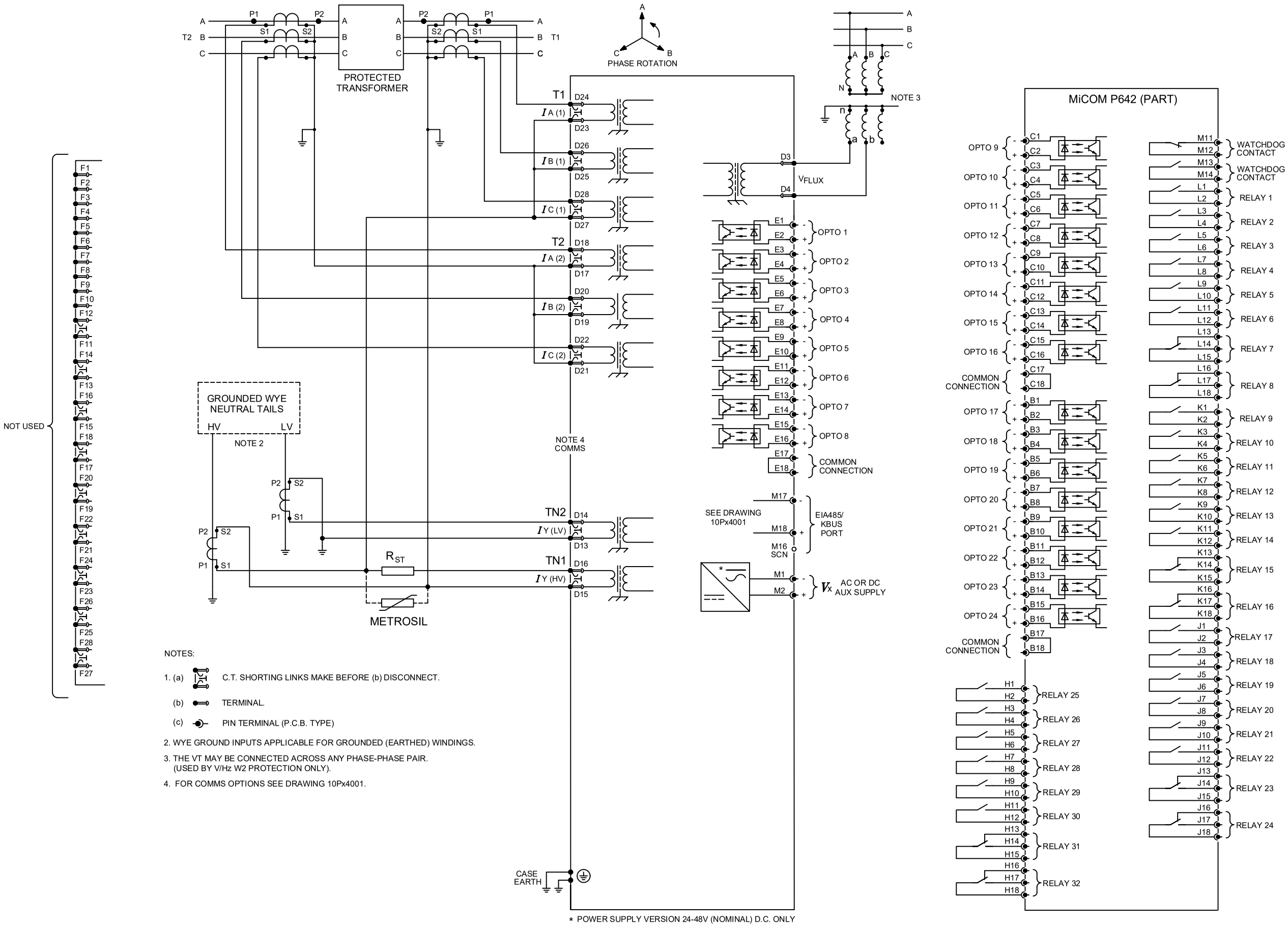


NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: EXTERNAL CONNECTION DIAGRAM: 2 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/P & 32 O/P) WITH 1 POLE VT INPUT (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64262	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

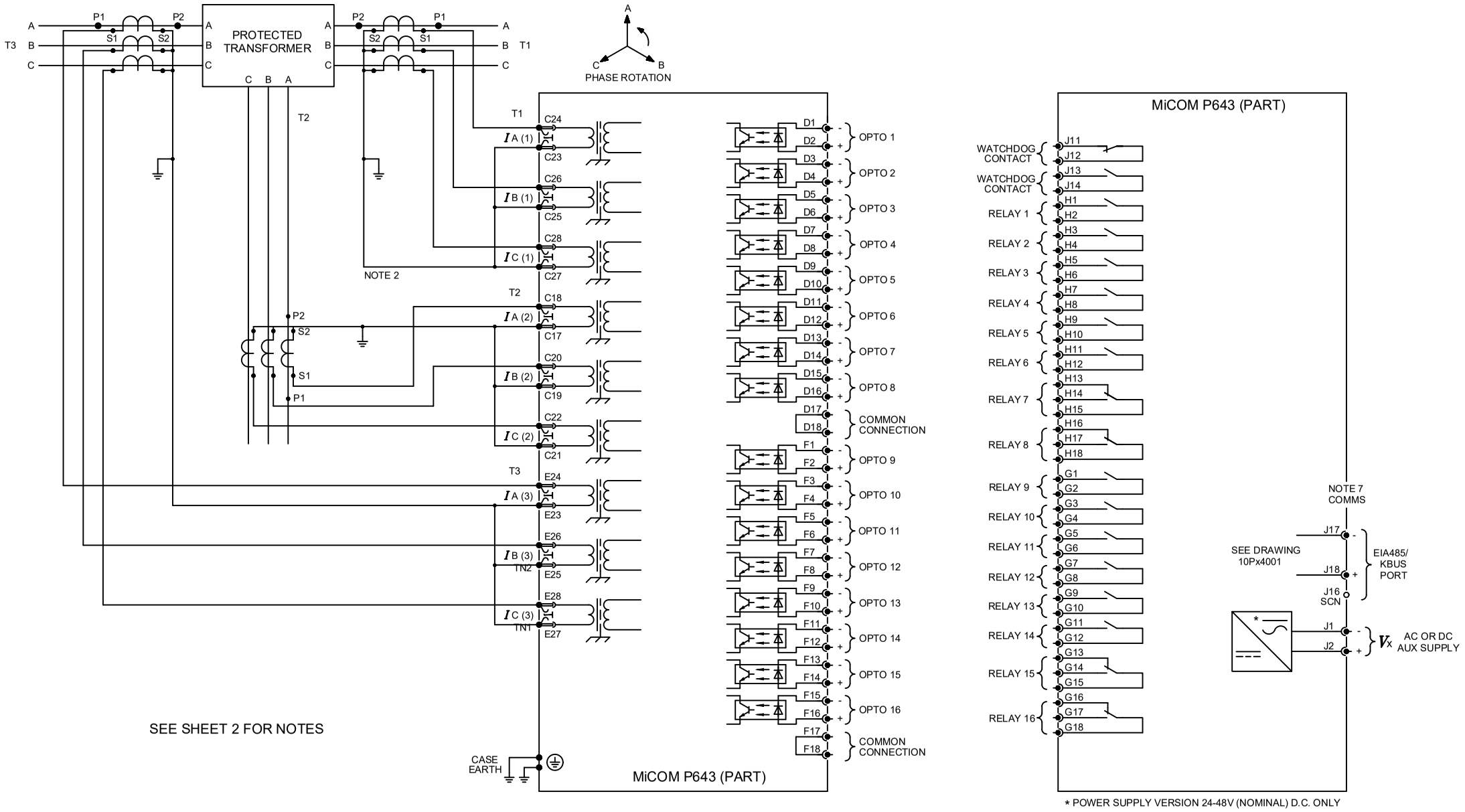


NOTES:

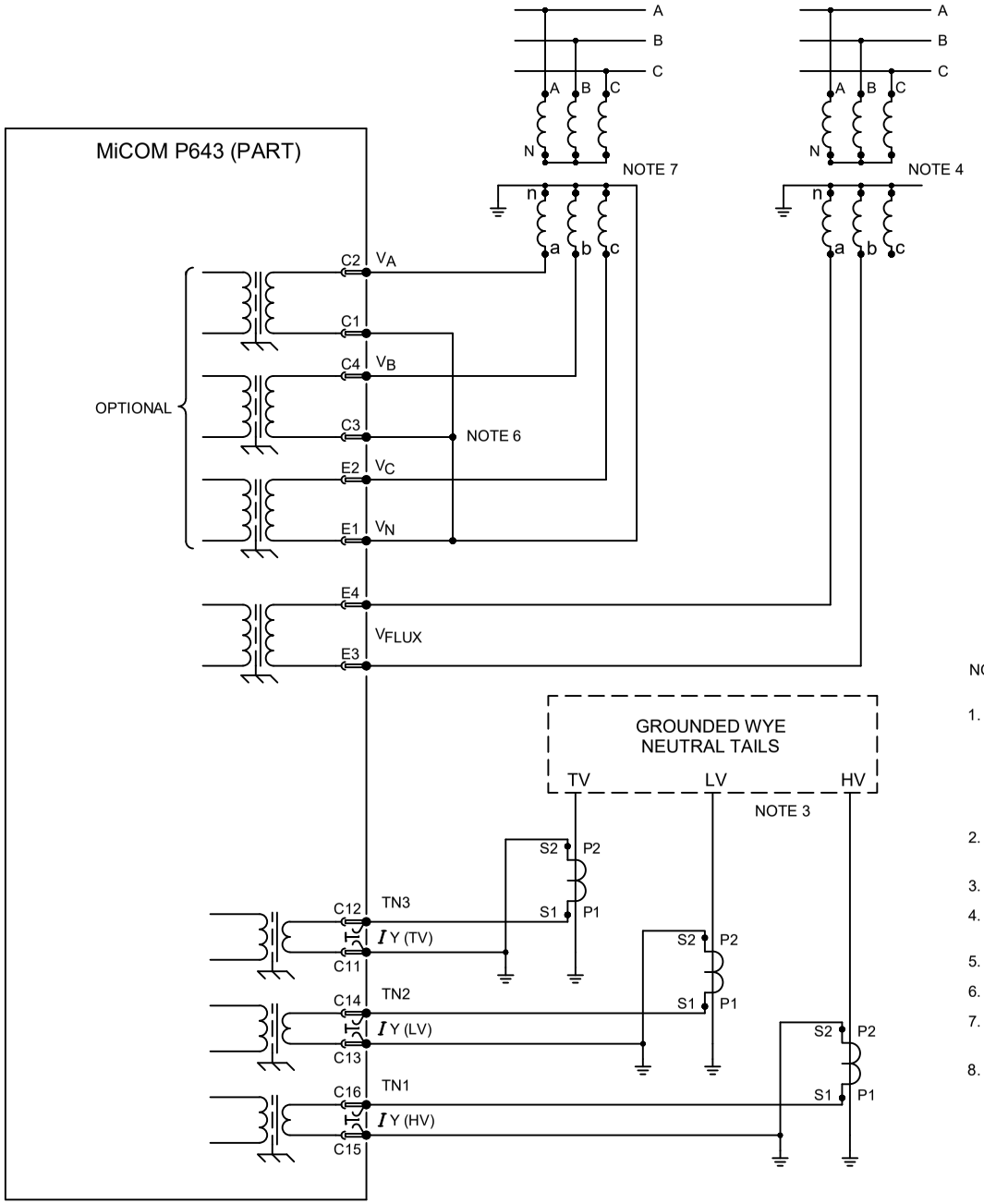
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

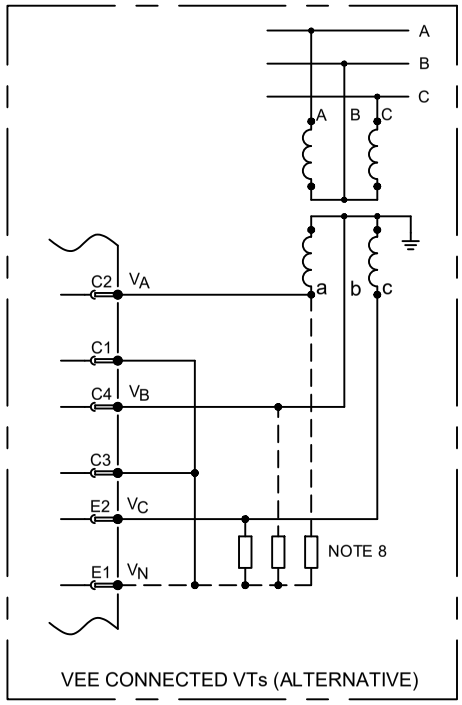
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Issue: B	Revision: CID008334. NOT USED TERMINALS ADDED.		Title: CONN DIAG:HIGH Z REF FOR 2 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 (80TE)		
Date: 06/05/2024	Name: S WOOTTON		Drg No: 10P64262	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: G	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64301	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

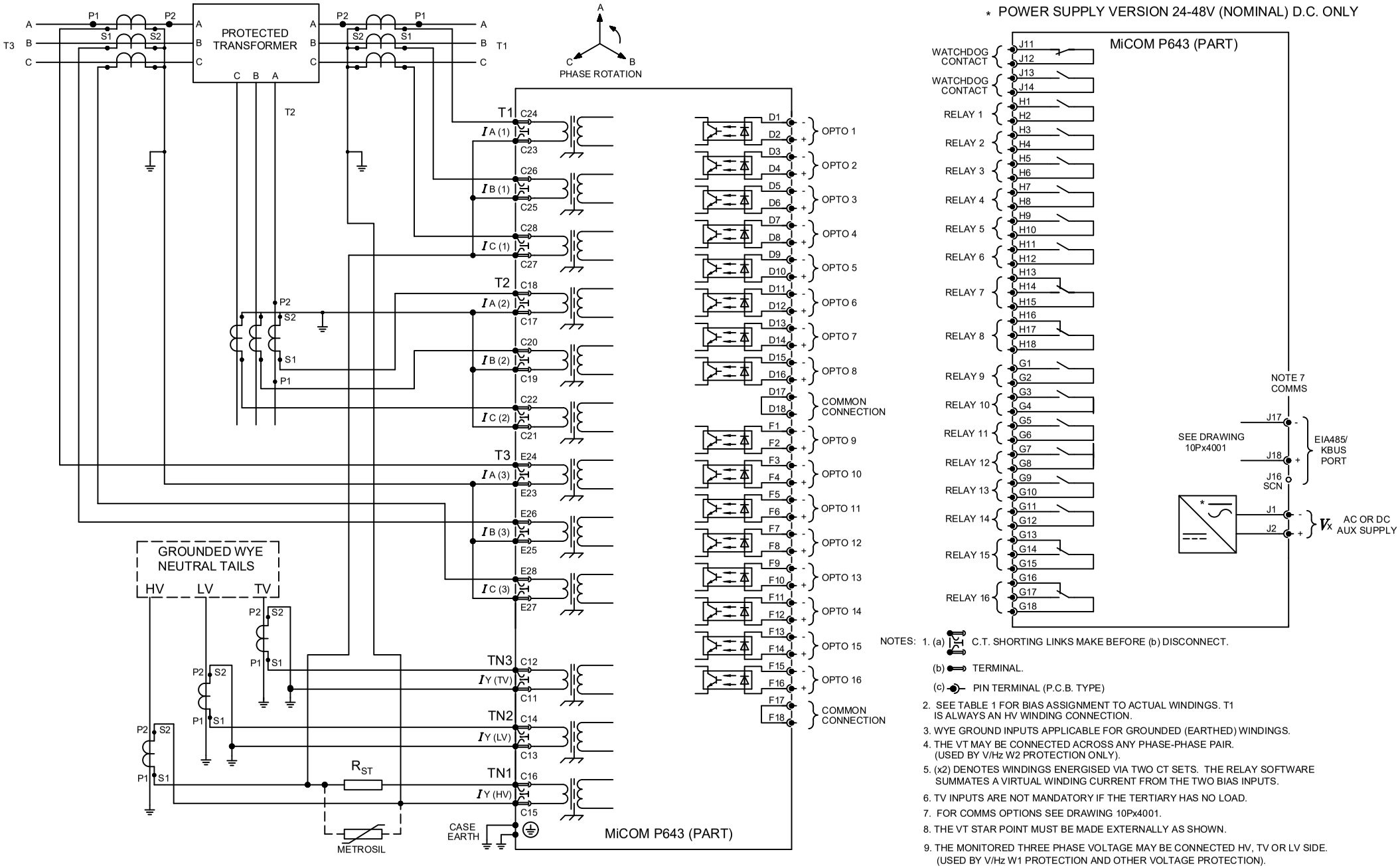




NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64301	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: E	Revision: CID006234 Outlines updated to GE Format		Title: EXT CONN DIAG:HIGH Z REF FOR 3 BIAS I/P TRANSFORMER DIFF SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2 &T3.	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64301	Sht: 3
Date:	Chkd:			Next Sht: -

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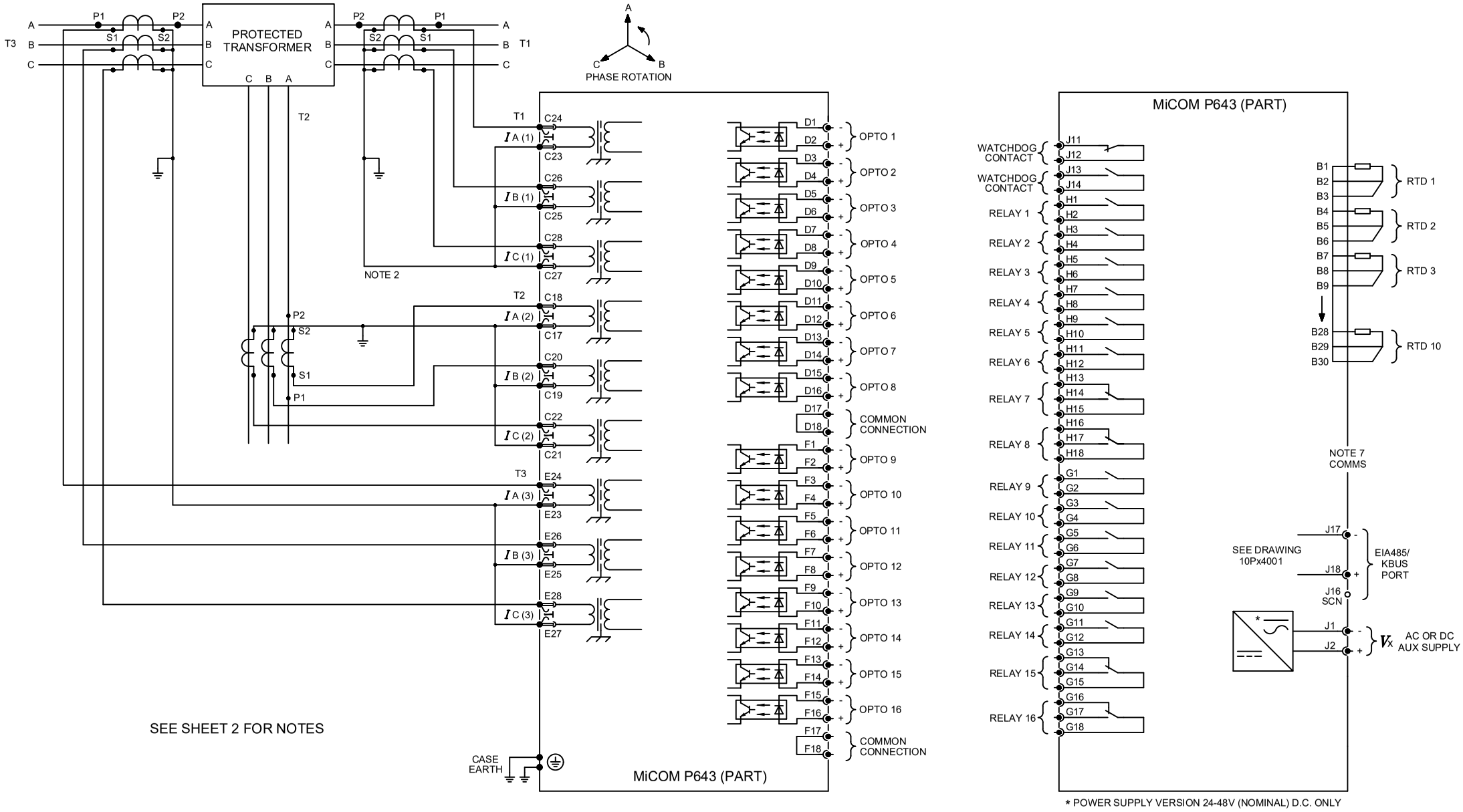
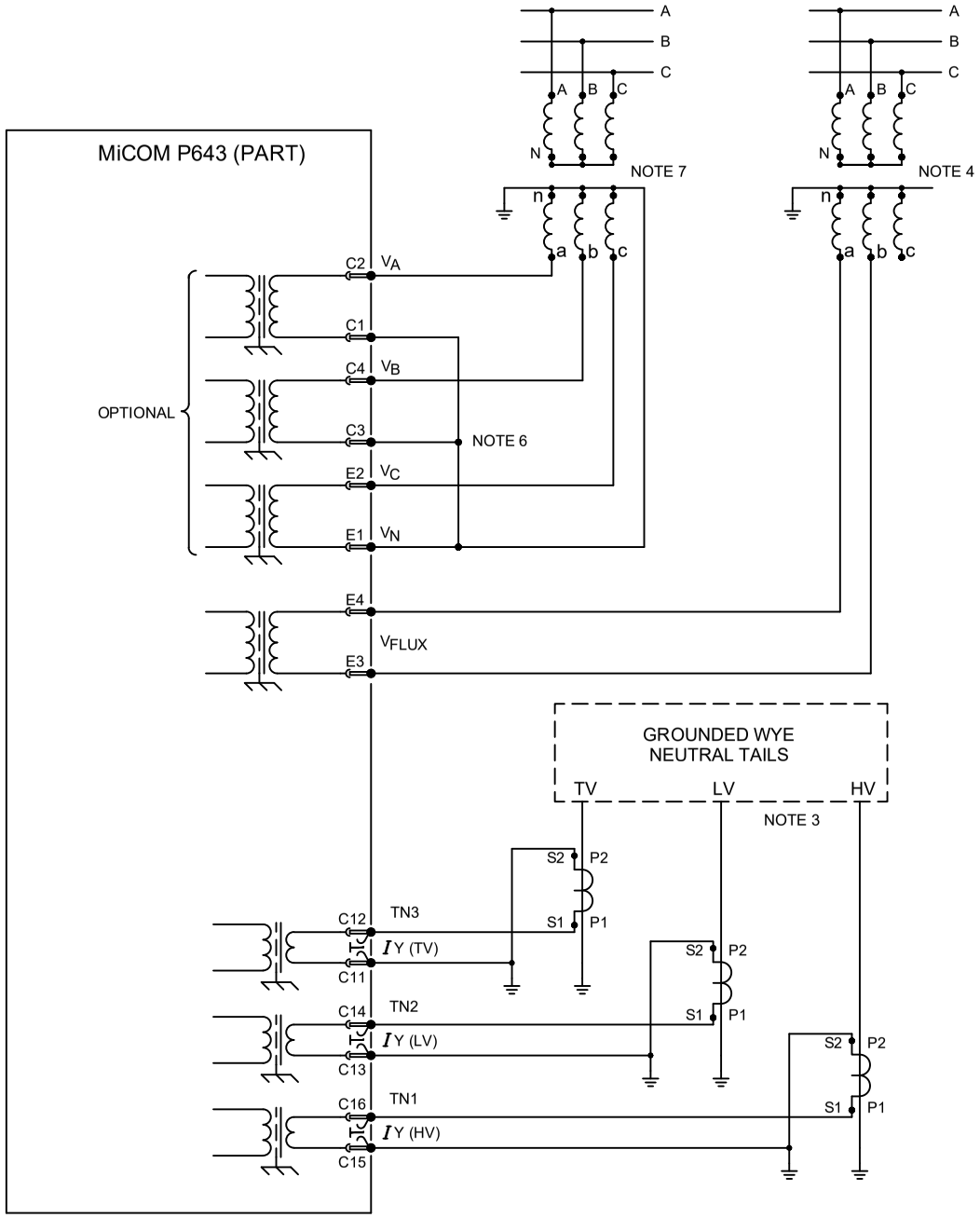
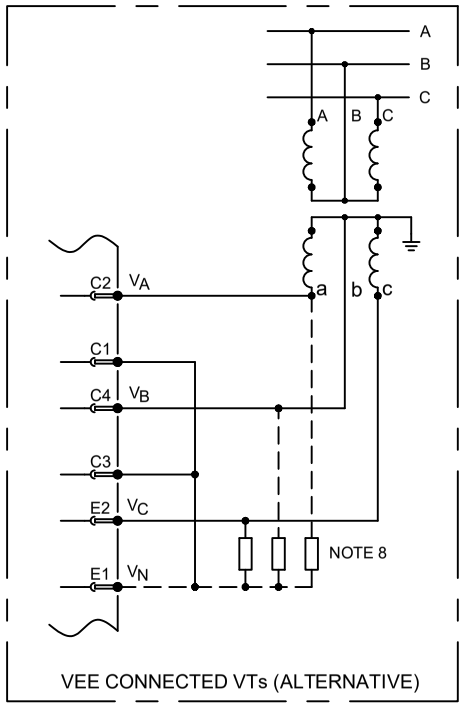


Issue: G	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 16 O/P + RTD) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64302	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

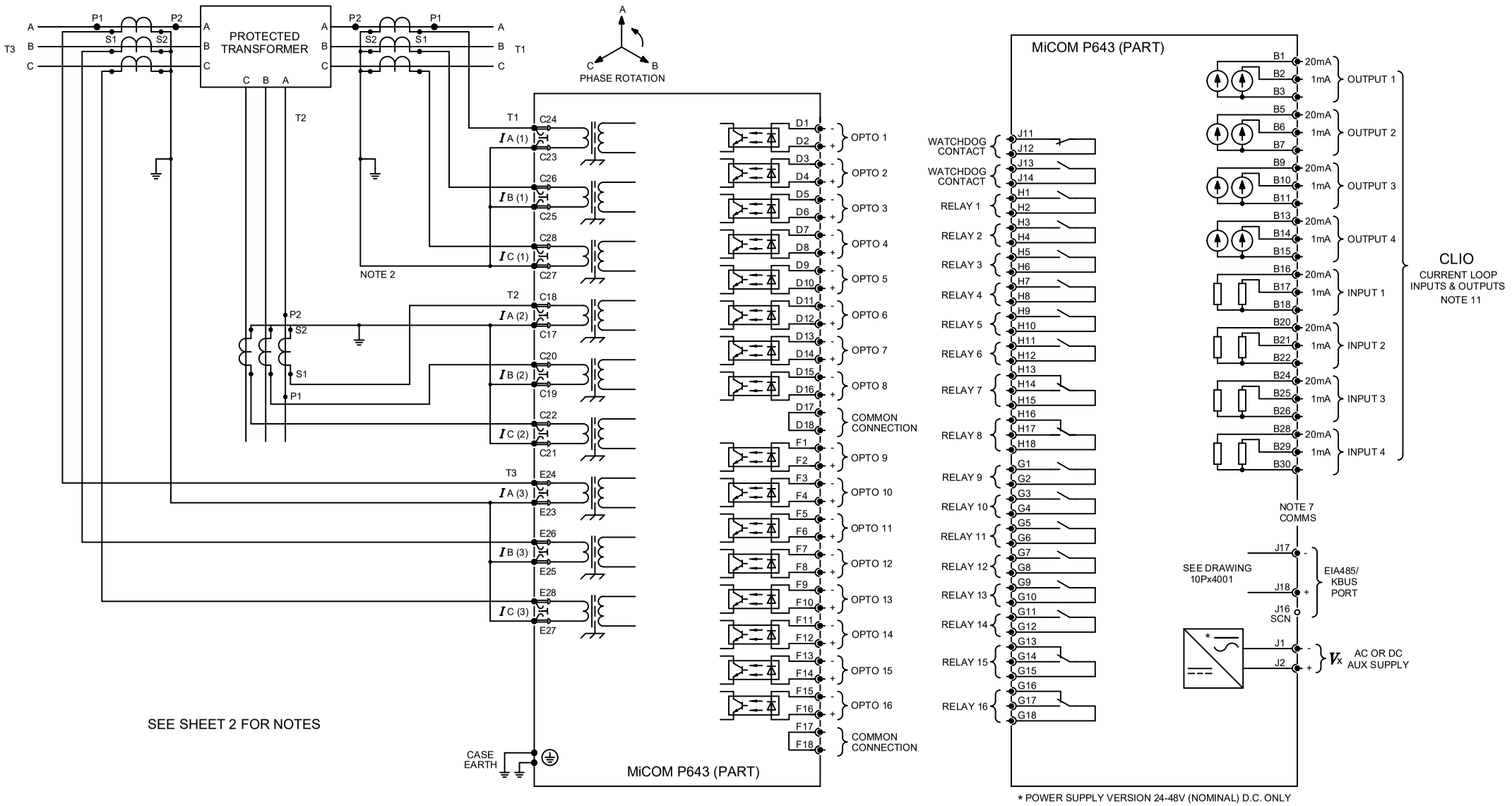




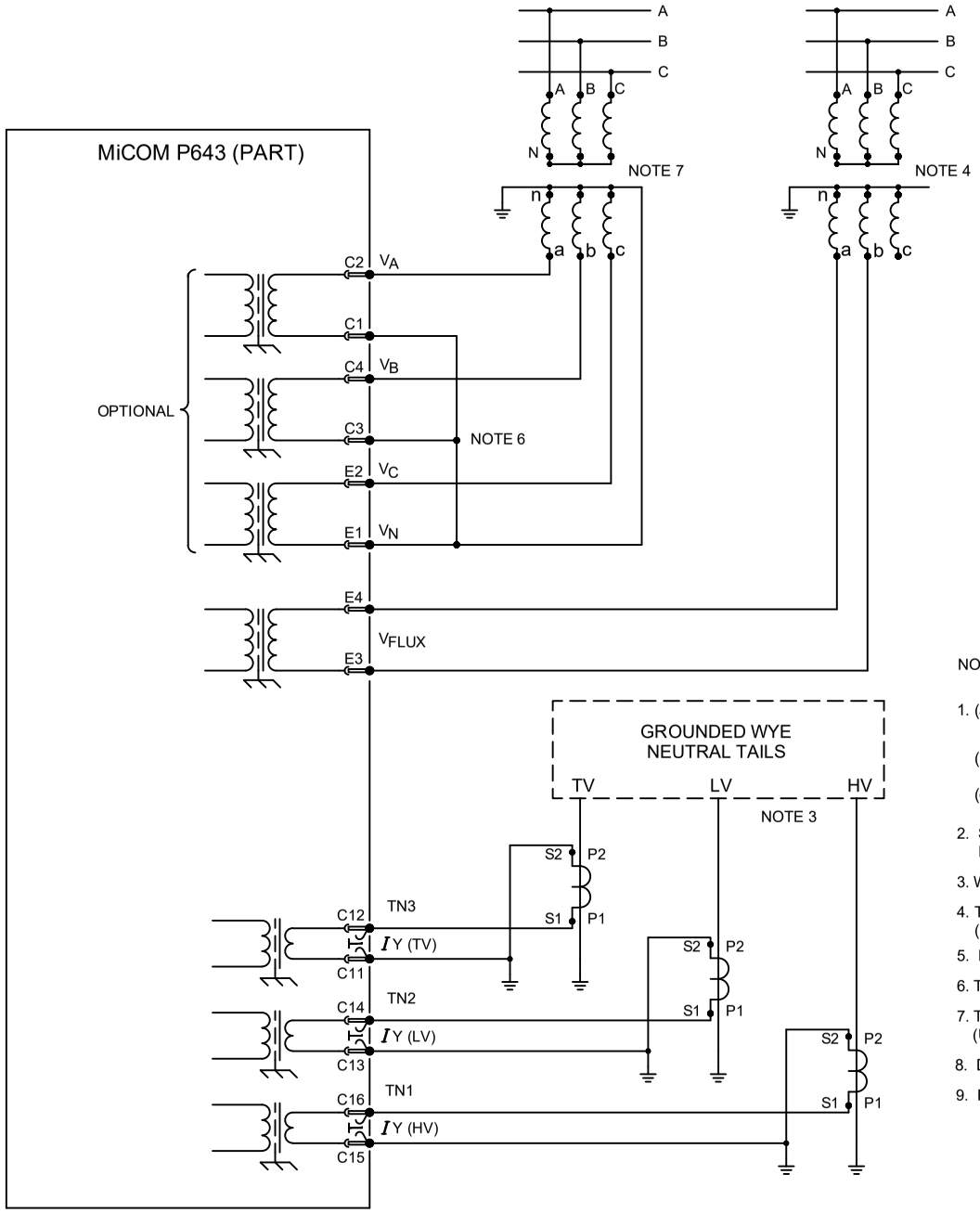
NOTES:

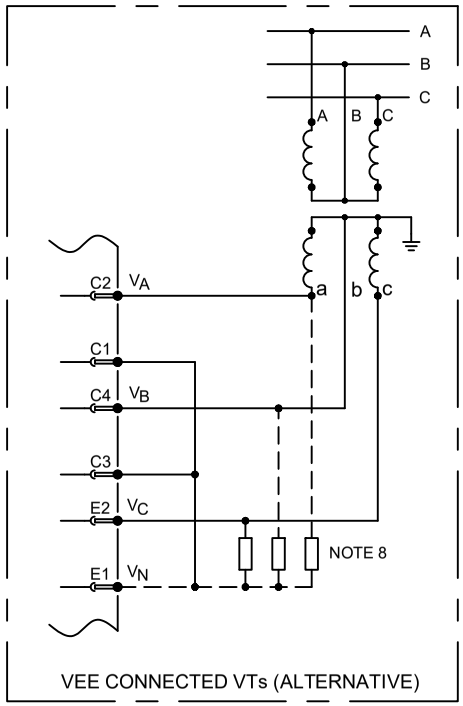
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 16 O/P + RTD) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64302	Sht: 2	©UK Grid Solutions Ltd St Leonards Building Harry Kerr Drive, Stafford. ST16 1WT, UK
Date:	Chkd:			Next Sht: -	



Issue: H	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 16 O/P + CLIO) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64303	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 16 O/P + CLIO) WITH 4 POLE VT INPUTS (60TE)	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64303	Sht: 2
Date:	Chkd:			Next Sht: -

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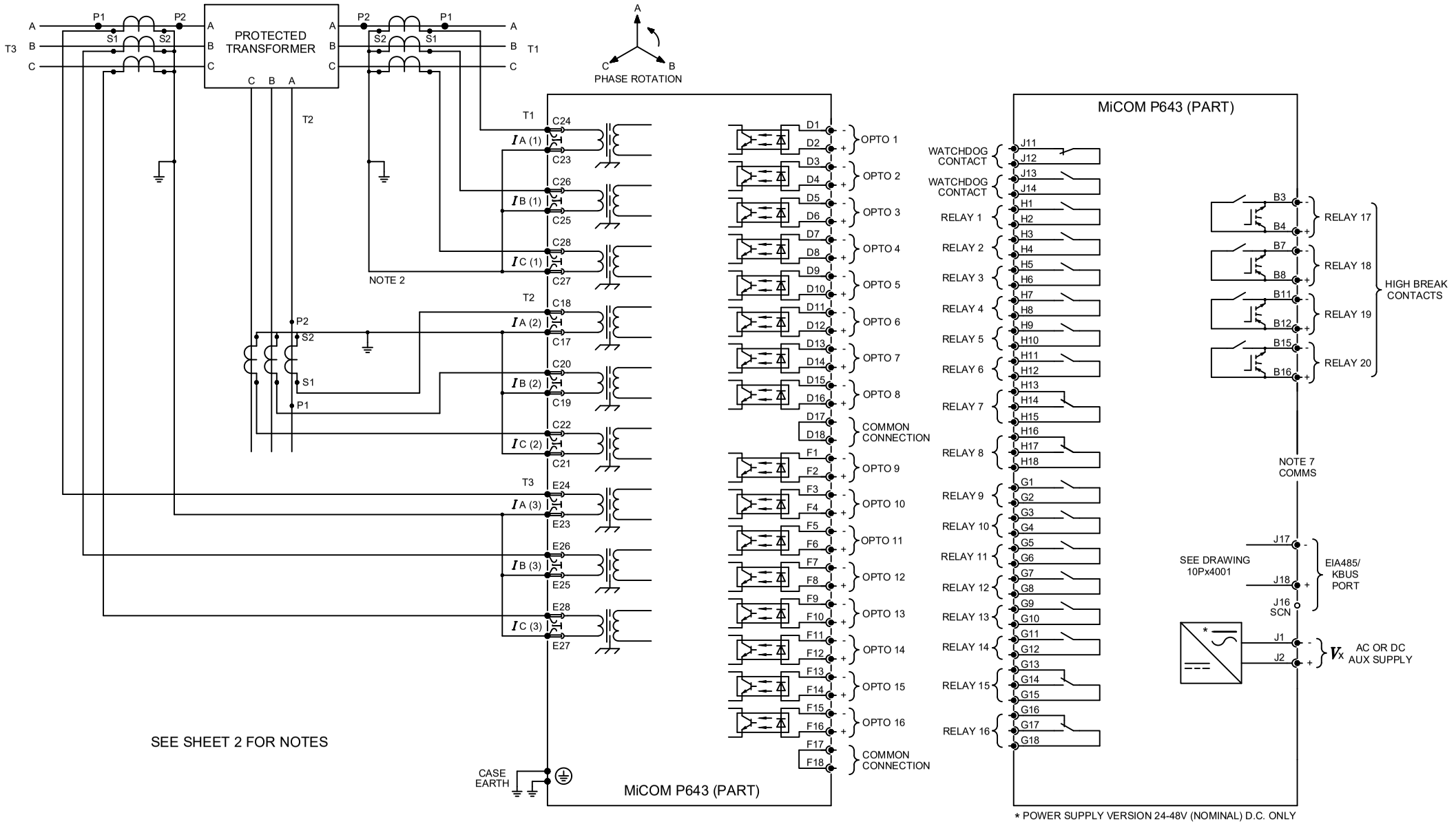
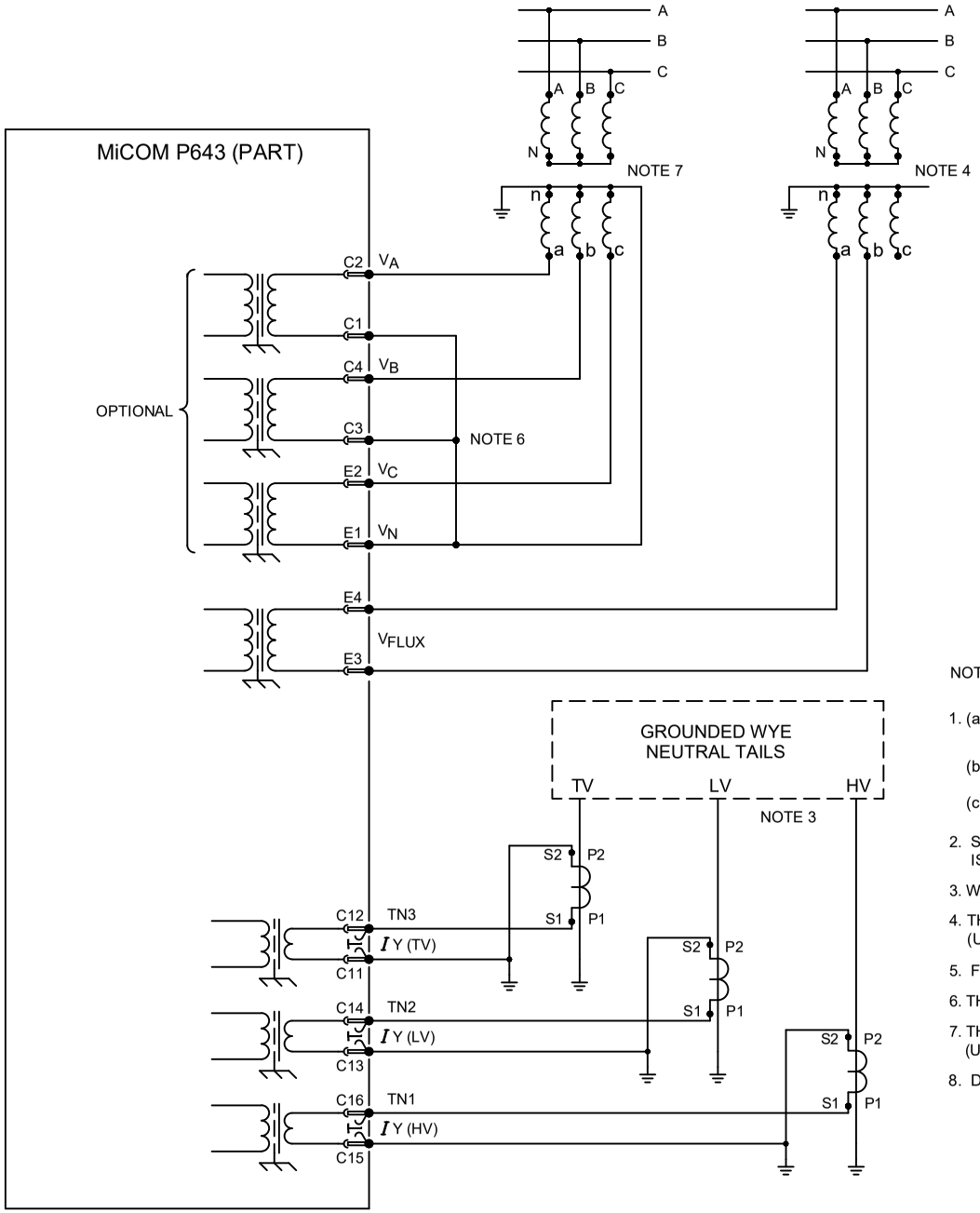
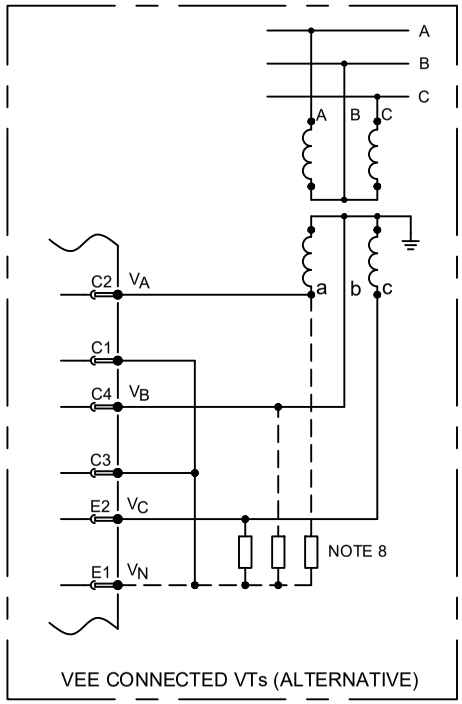


Issue: G	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P 20 O/P) WITH 4 POLE VT INPUT (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64306	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
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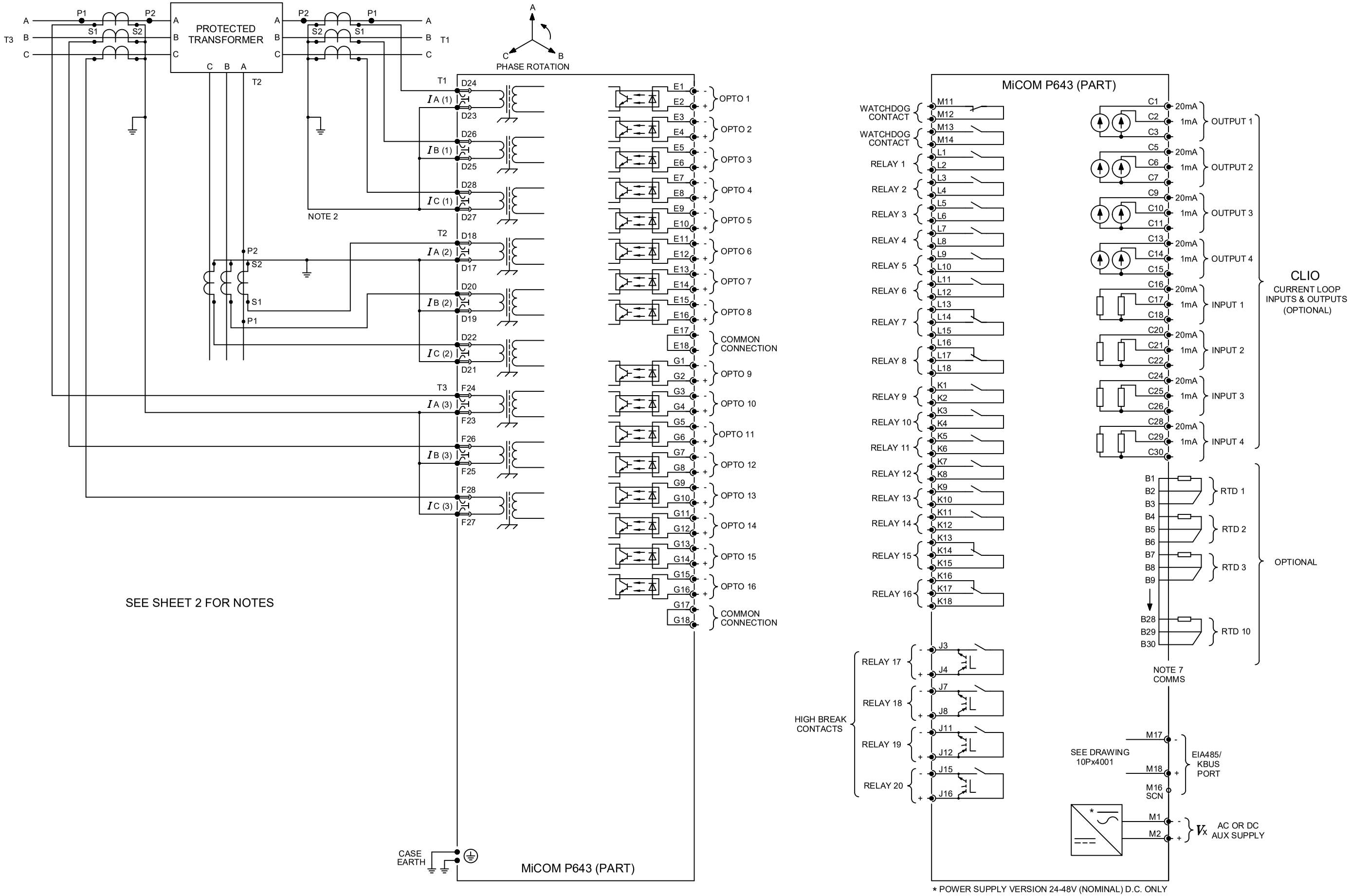
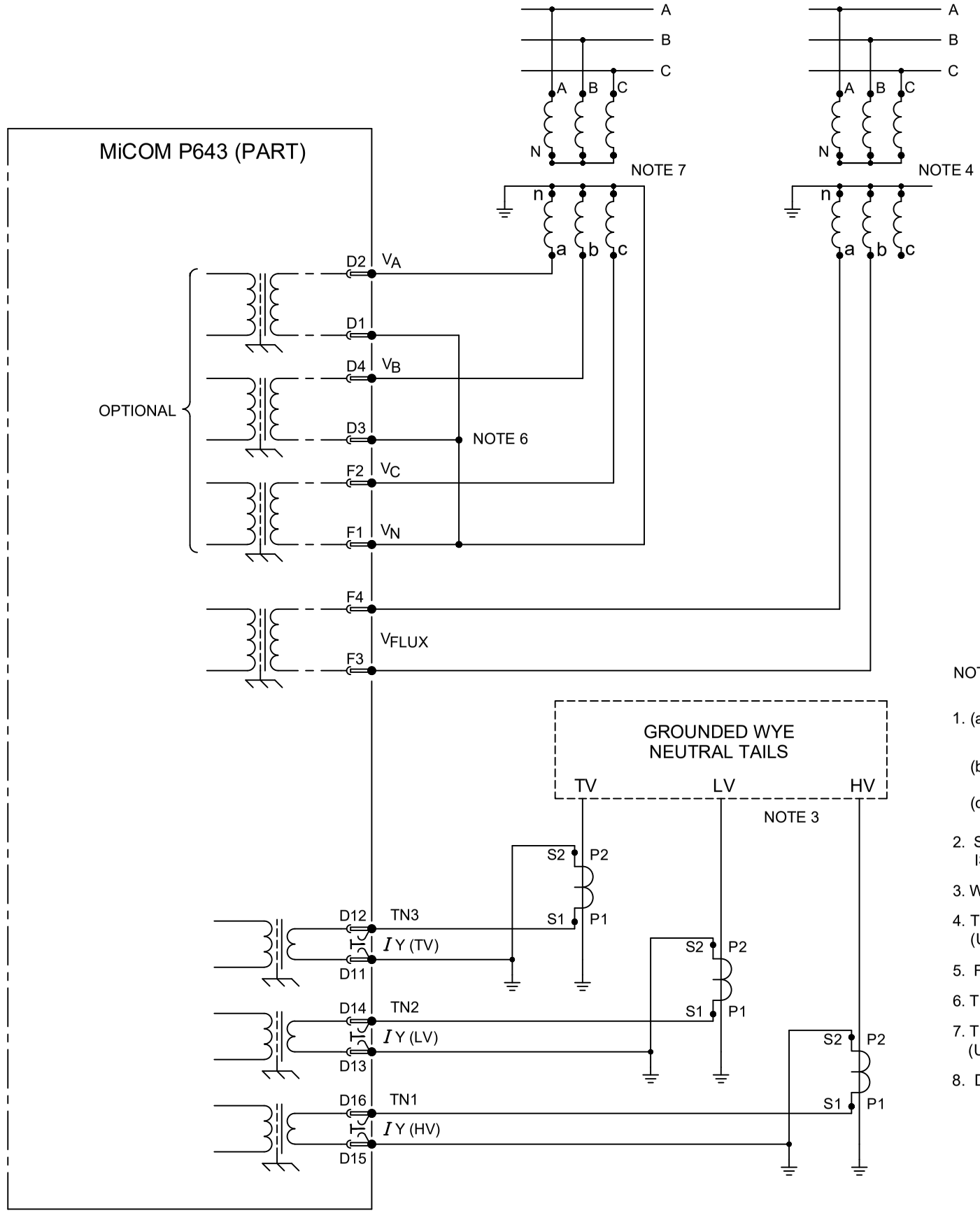
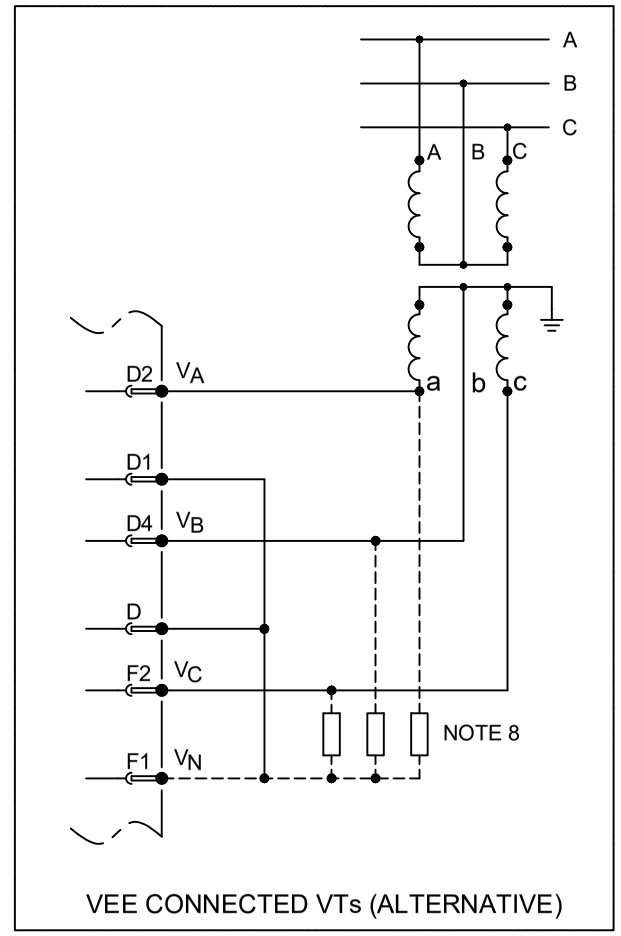
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P 20 O/P) WITH 4 POLE VT INPUT (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64306	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 31/01/2023	Name: S WOOTTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64330	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
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5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/16O+4 HB) 80TE	
Date: 05/05/2023	Name: S WOOTTON		Drg No: 10P64330	Sht: 2
Date:	Chkd:			Next Sht: -

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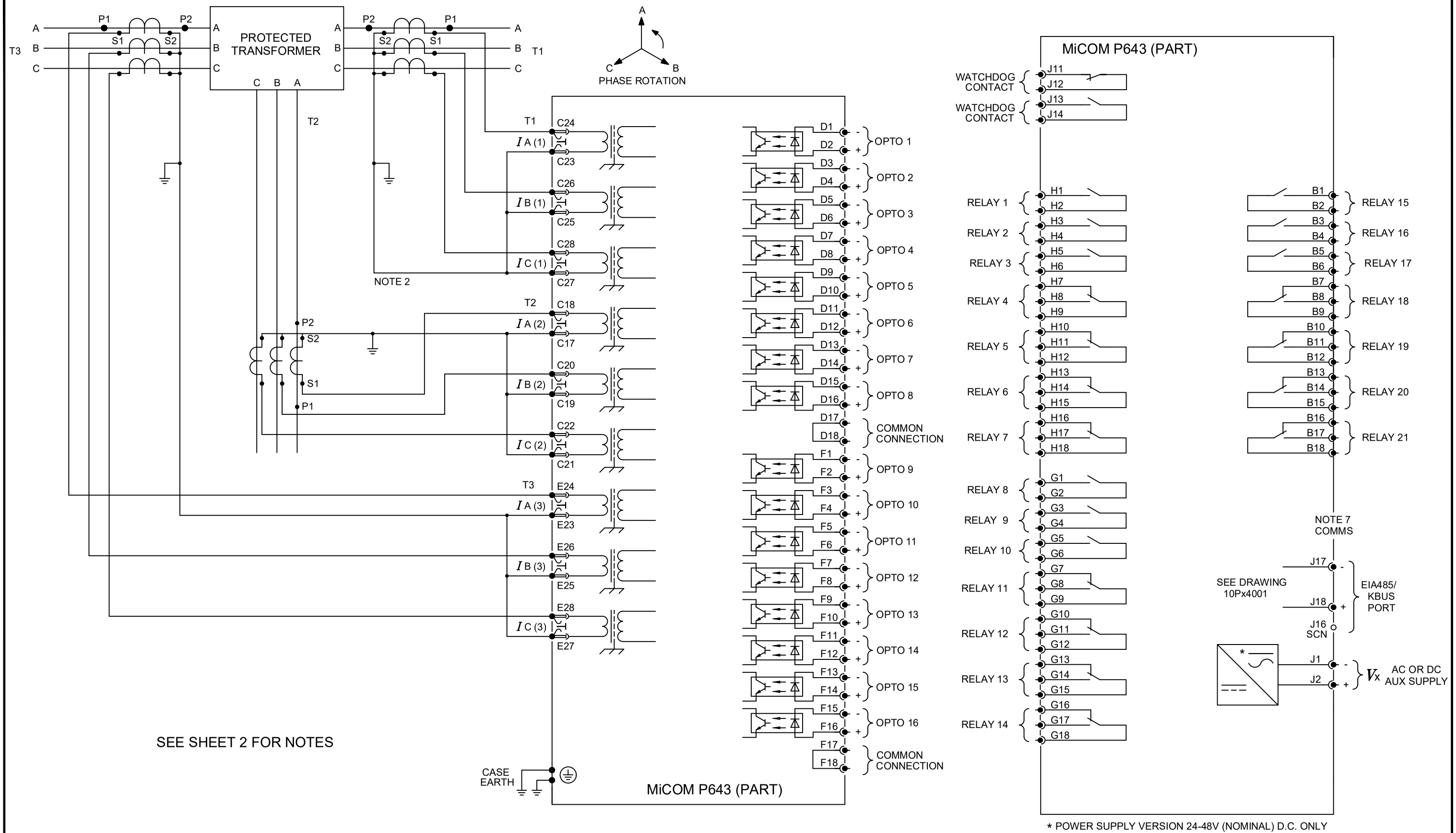
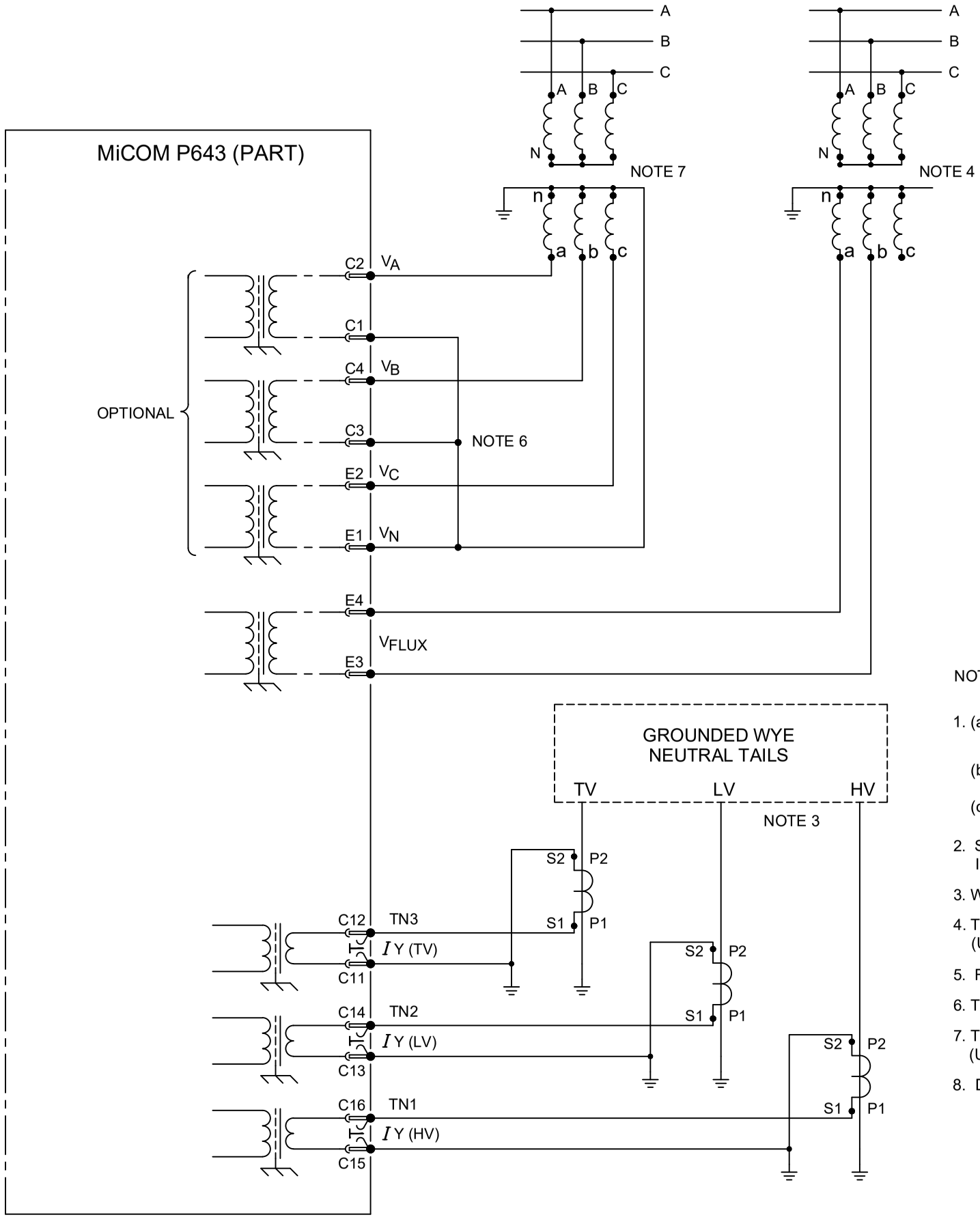
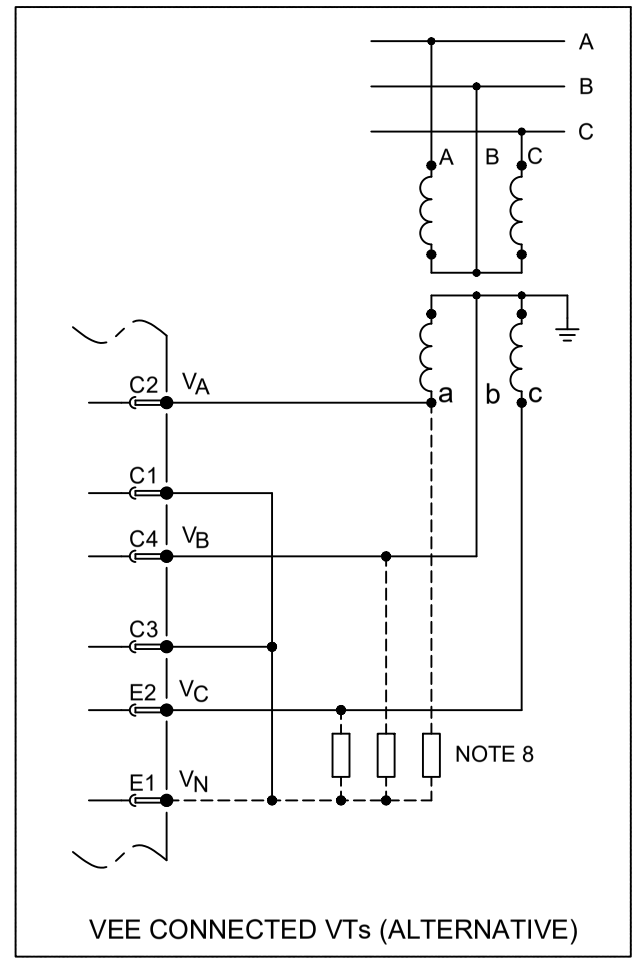


Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (16 I/P & 21 O/P) 60TE		
Date: 26/1/2023	Name: S WOOTTON		Drg No: 10P64322	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CICD007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (16 I/P & 21 O/P) 60TE	
Date: 26/04/2023	Name: S WOOTTON		Drg No: 10P64322	Sht: 2
Date:	Chkd:			Next Sht: -

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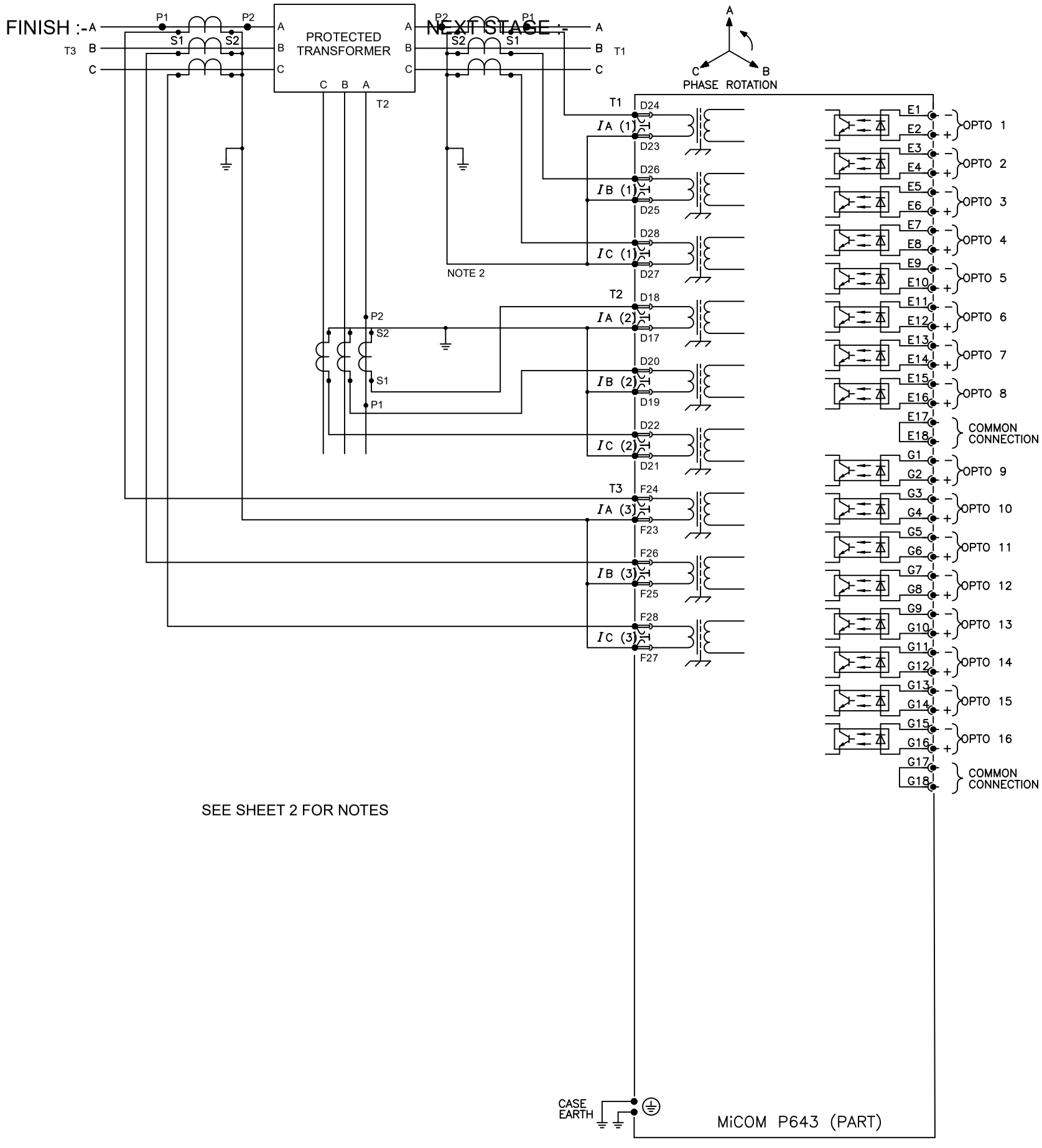
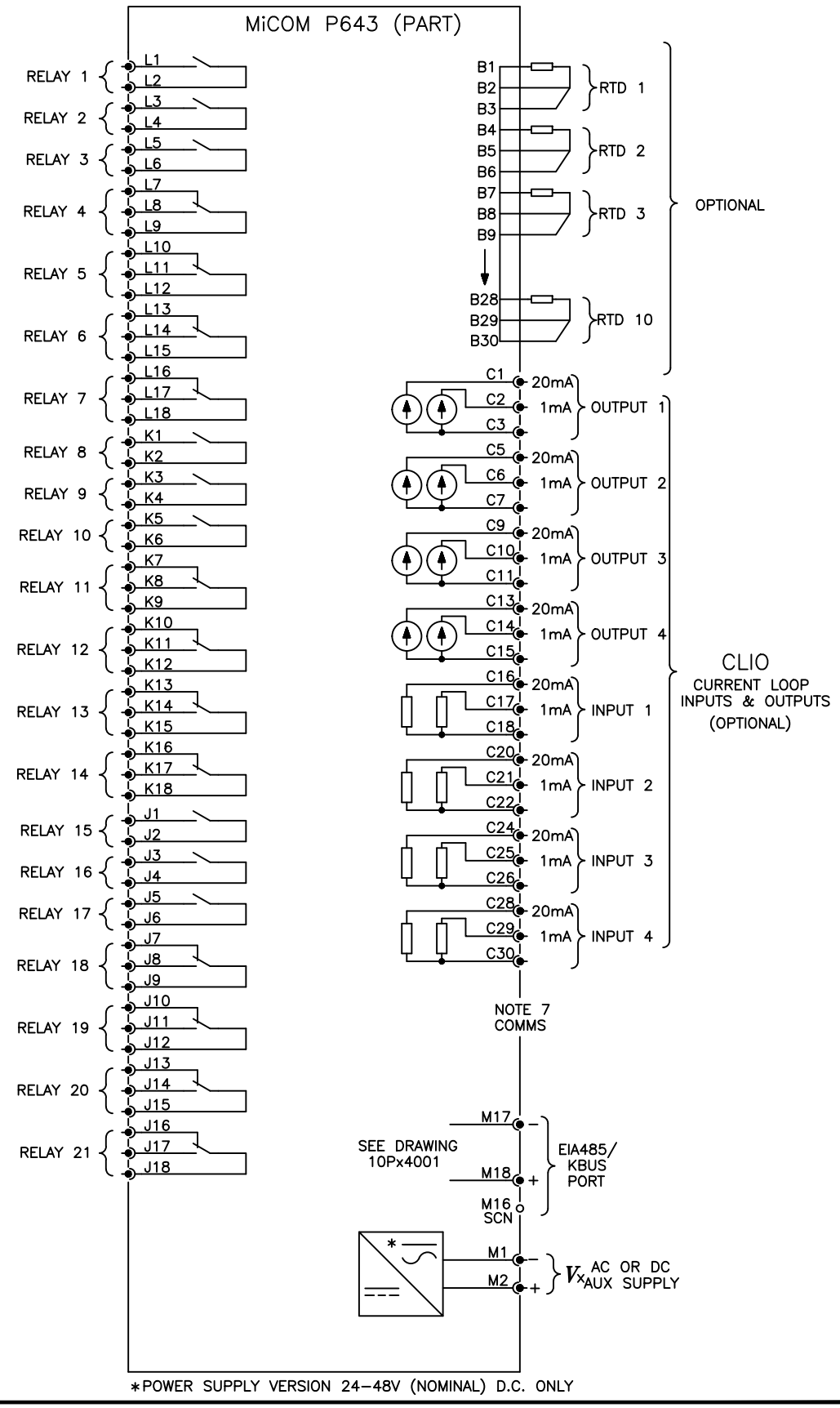
FINISH :-

NEXT STAGE :-



SEE SHEET 2 FOR NOTES



*POWER SUPPLY VERSION 24–48V (NOMINAL) D.C. ONLY

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE	
Date: 01/03/2023	Name: S WOOTTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64335	Sht: 1
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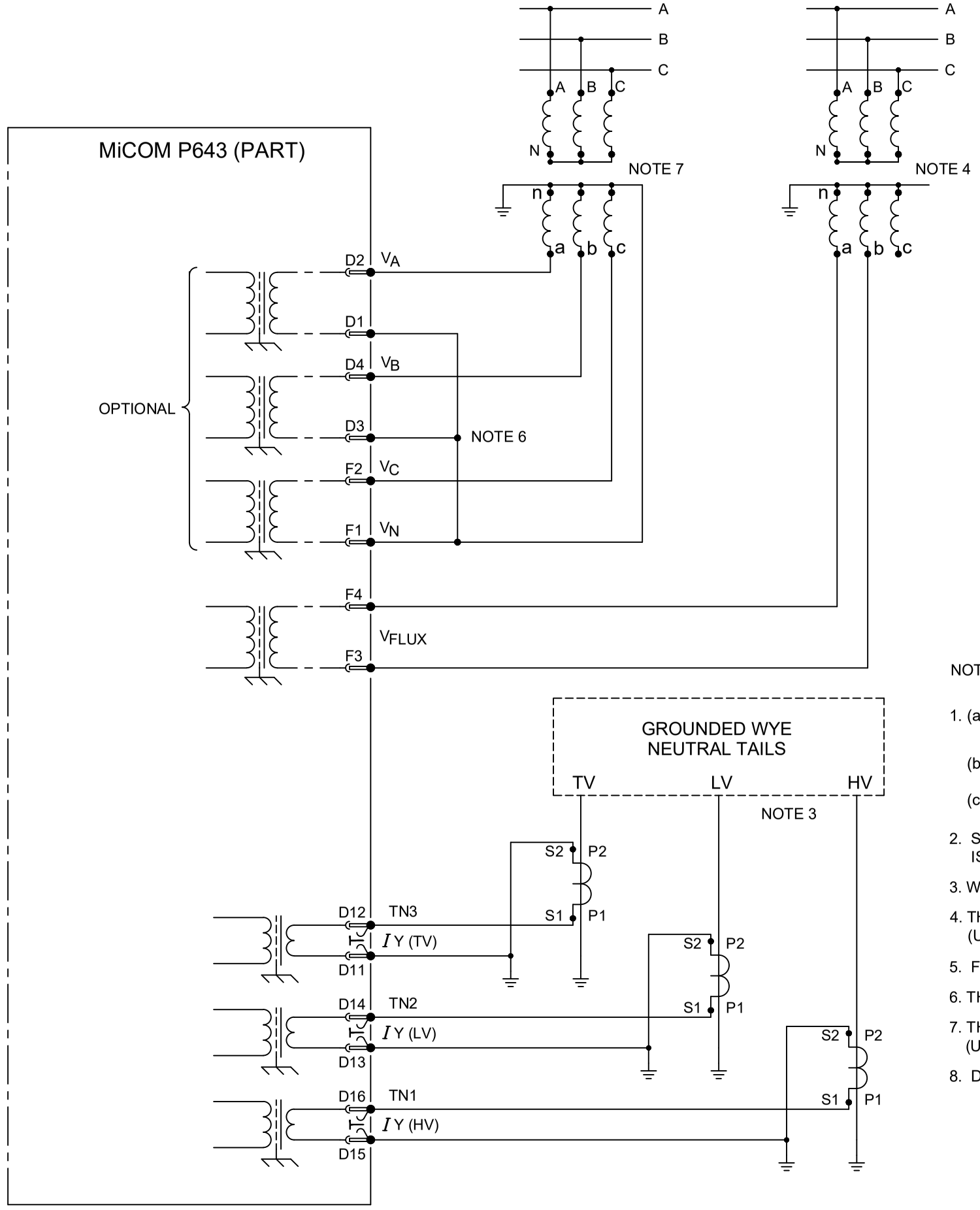

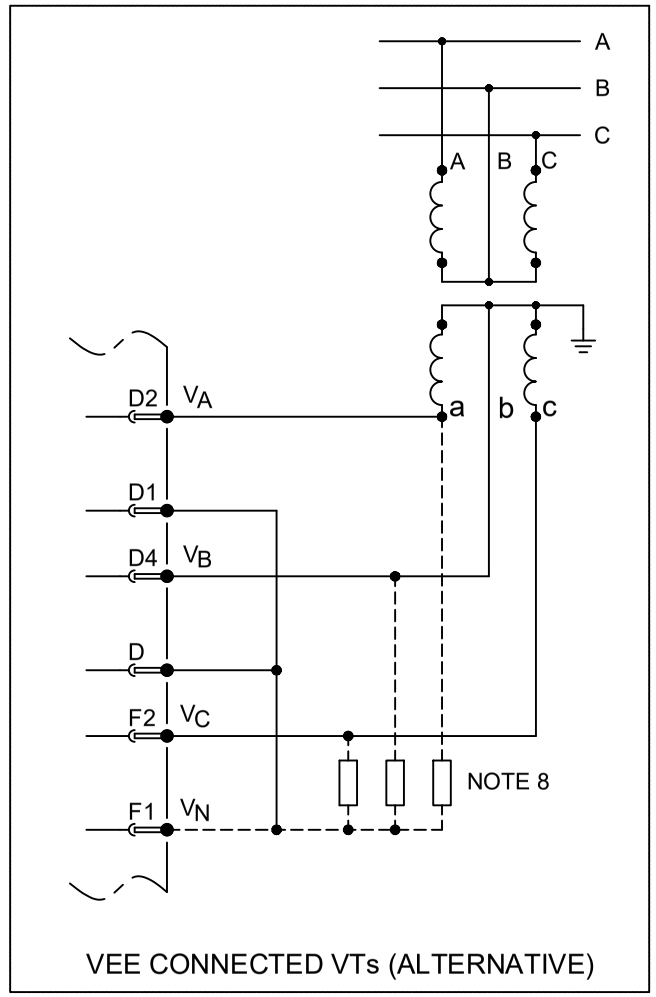

VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
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5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
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7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/21O) 80TE	
Date: 02/06/2023	Name: S WOOTTON		Drg No: 10P64335	Sht: 2
Date:	Chkd:			Next Sht: -

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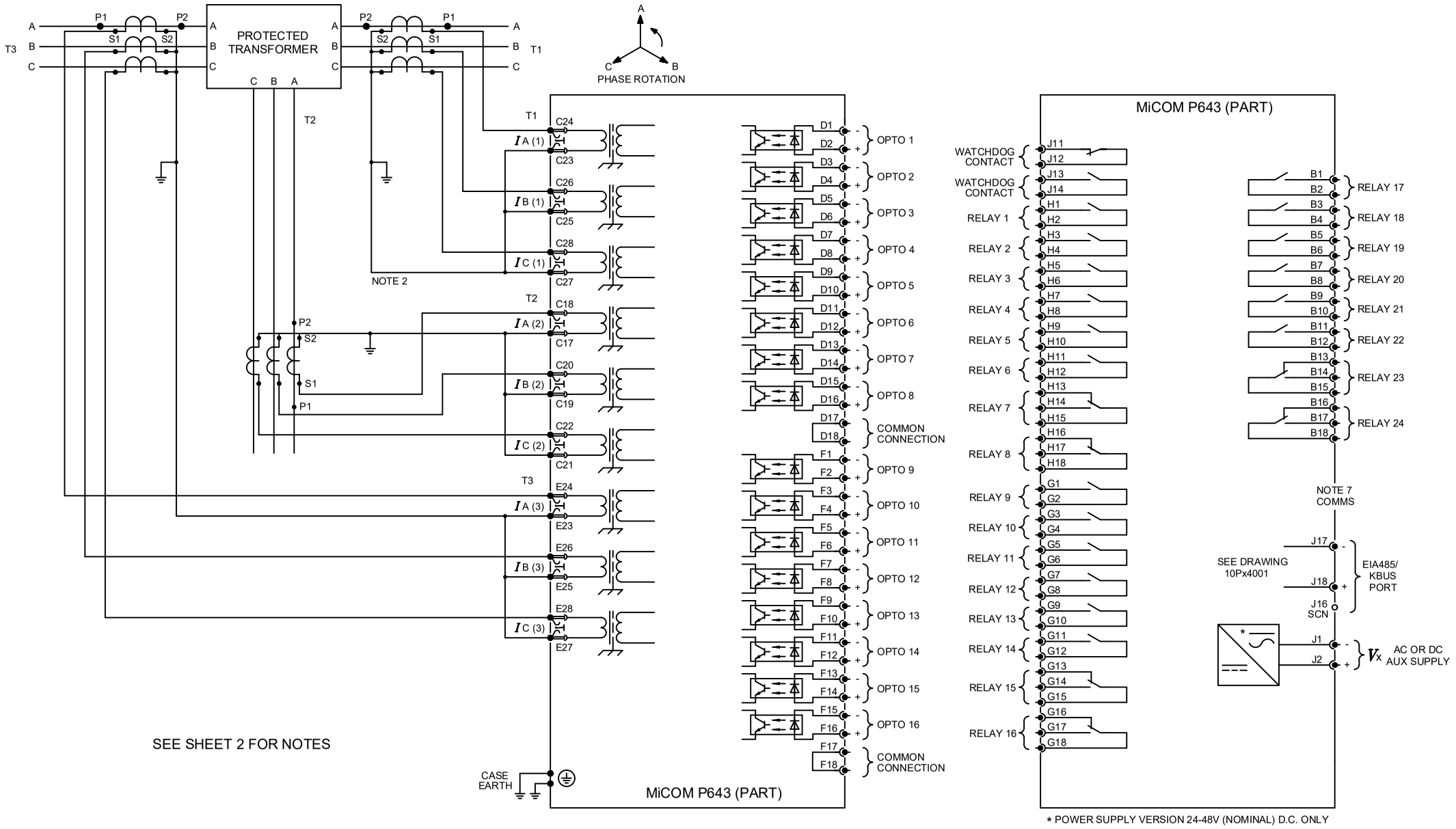
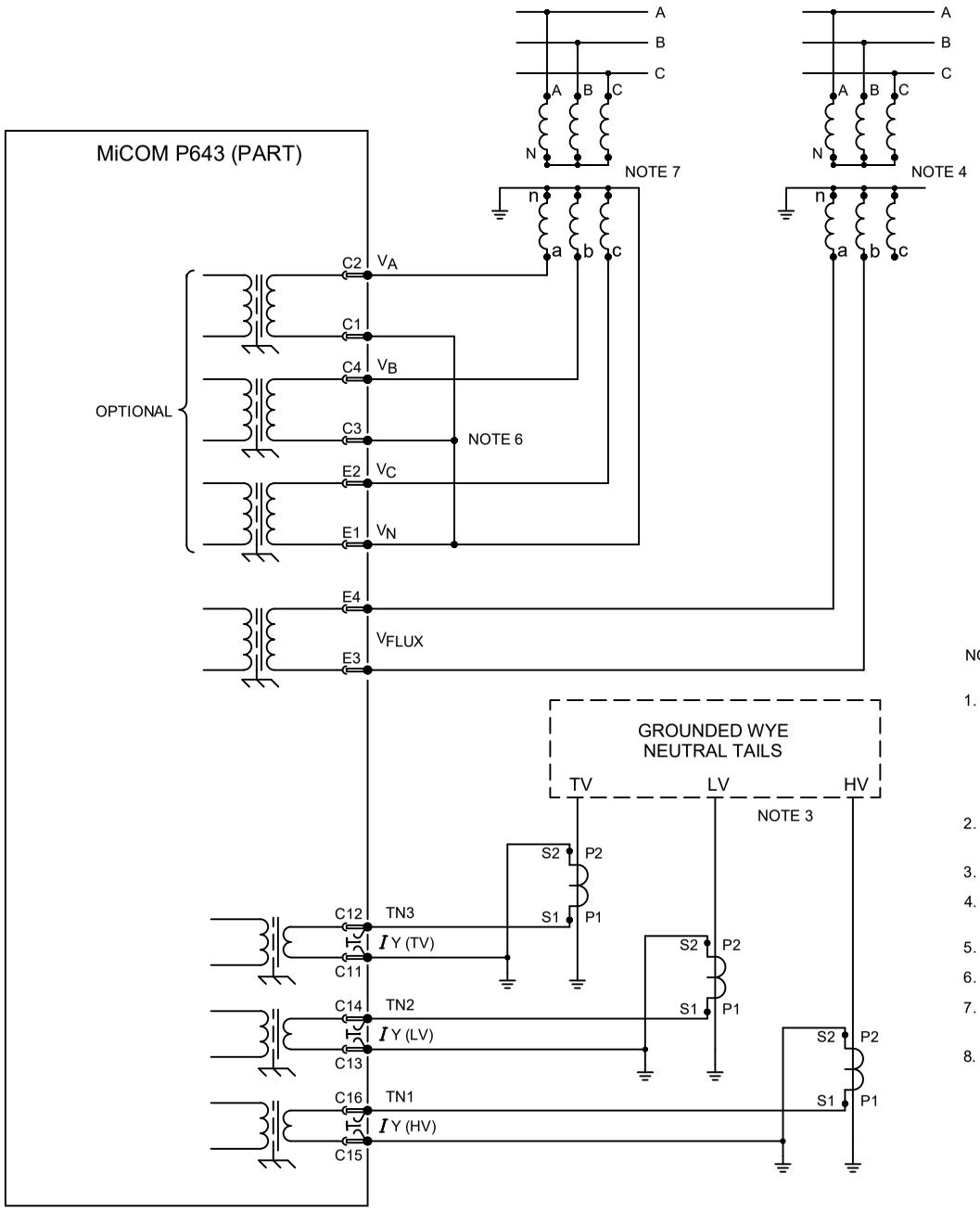
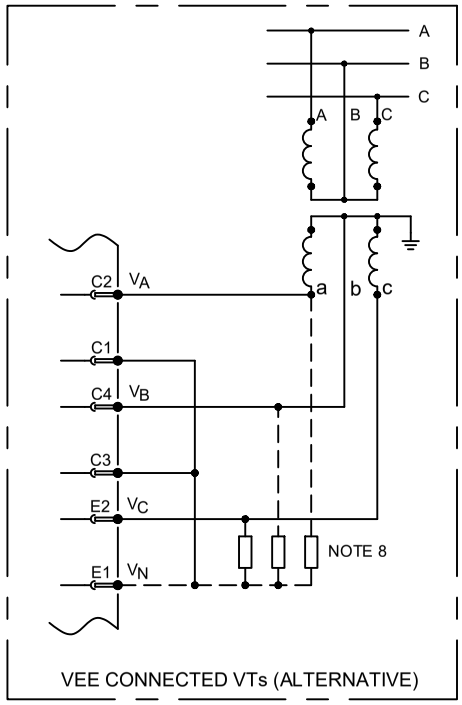


Issue: G	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 24 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64305	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
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Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/O & 24 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64305	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

FINISH :-

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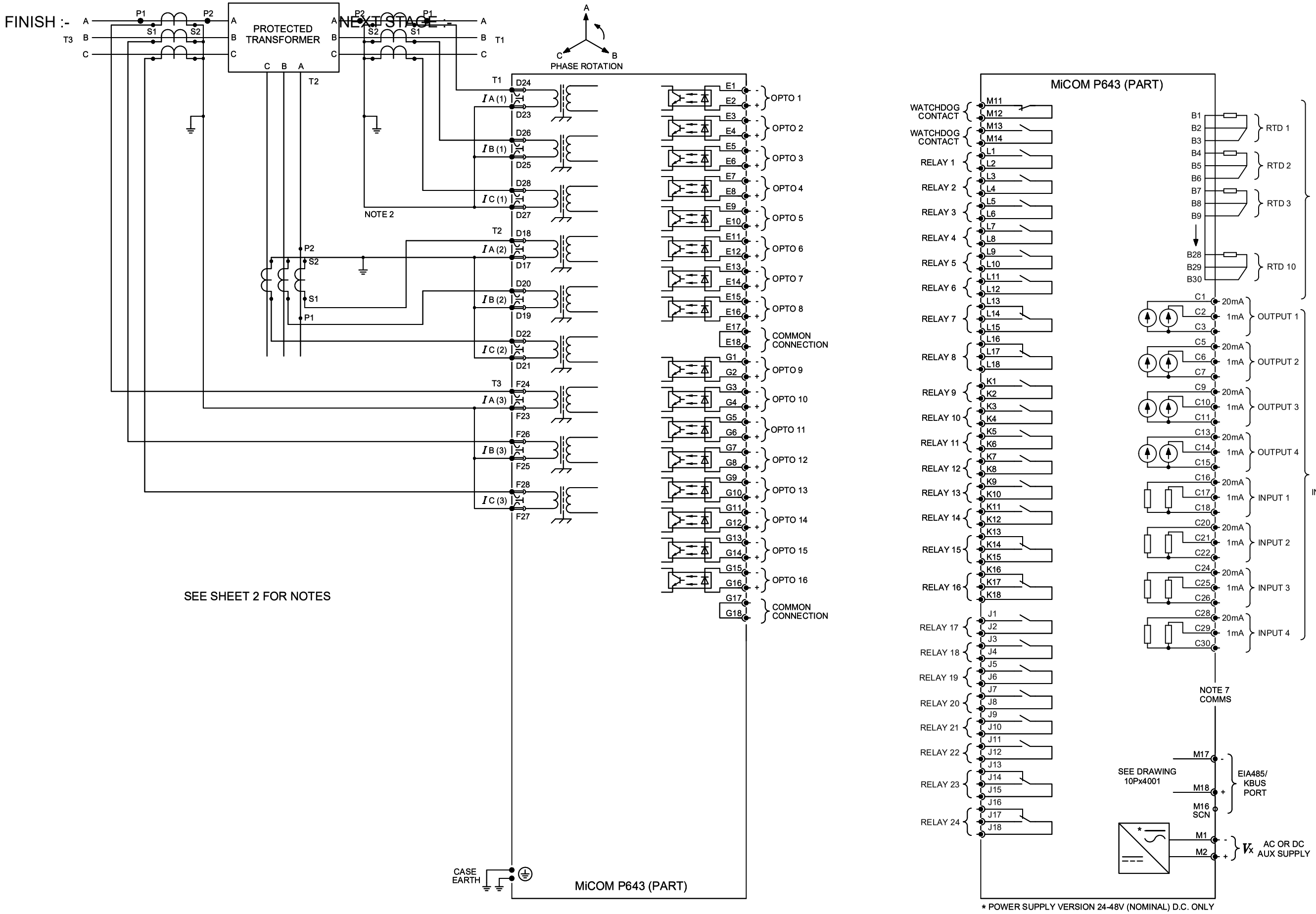
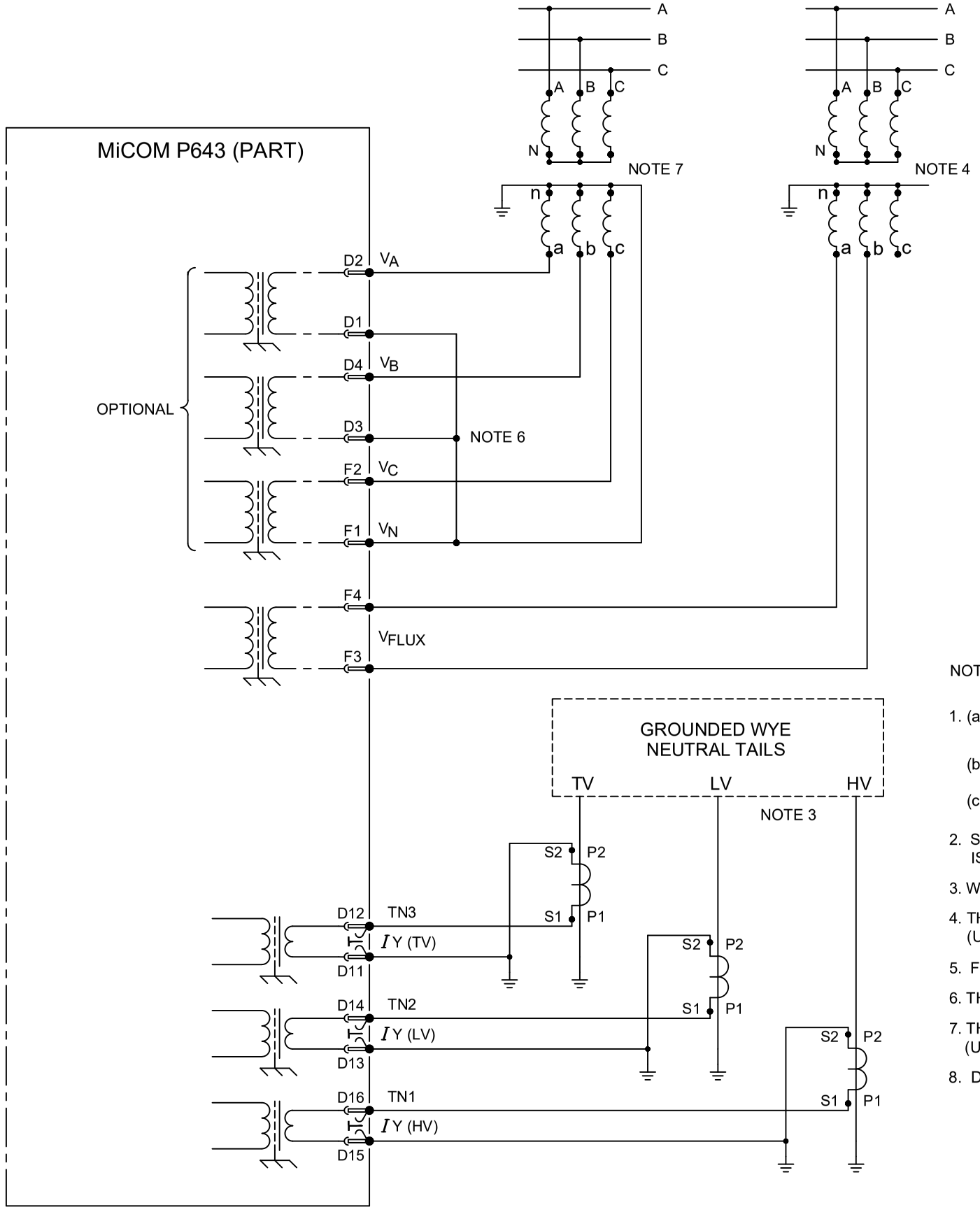
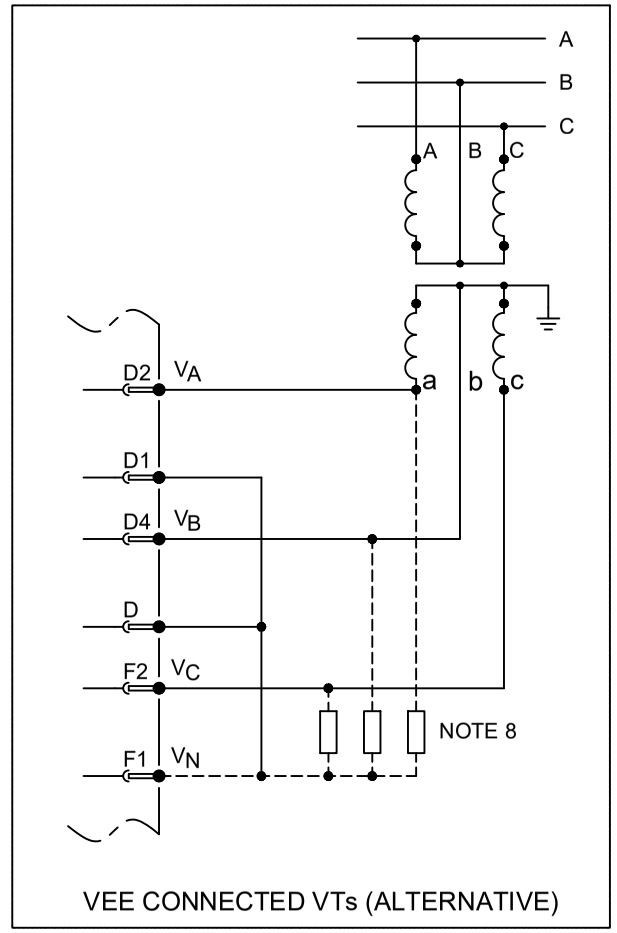


SEE SHEET 2 FOR NOTES

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 02/03/2023	Name: S WOOTTON		Drg No: 10P64339	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





VEE CONNECTED VTs (ALTERNATIVE)

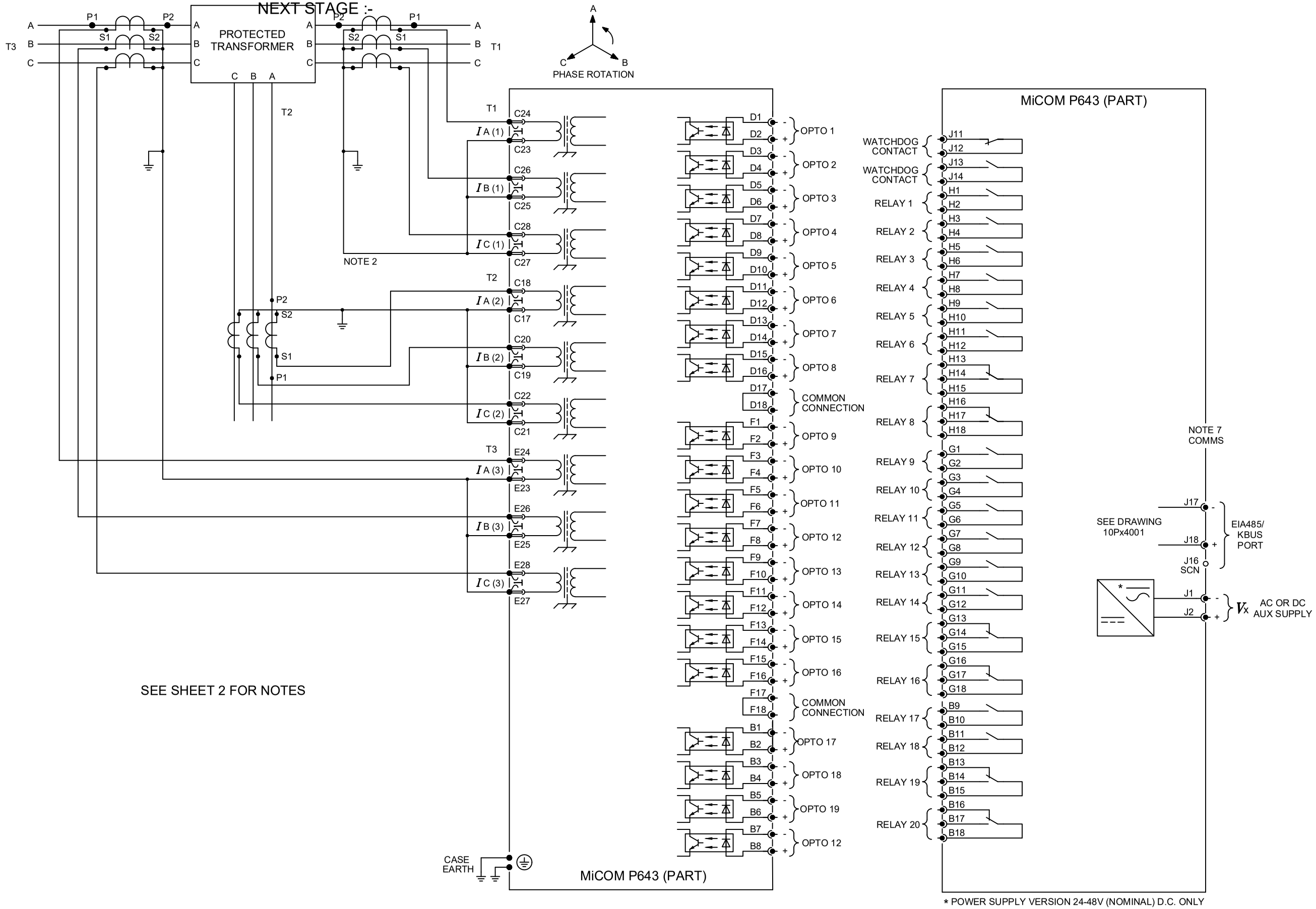
NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/24O) 80TE		
Date: 05/06/2023	Name: S WOOTTON		Drg No: 10P64339	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

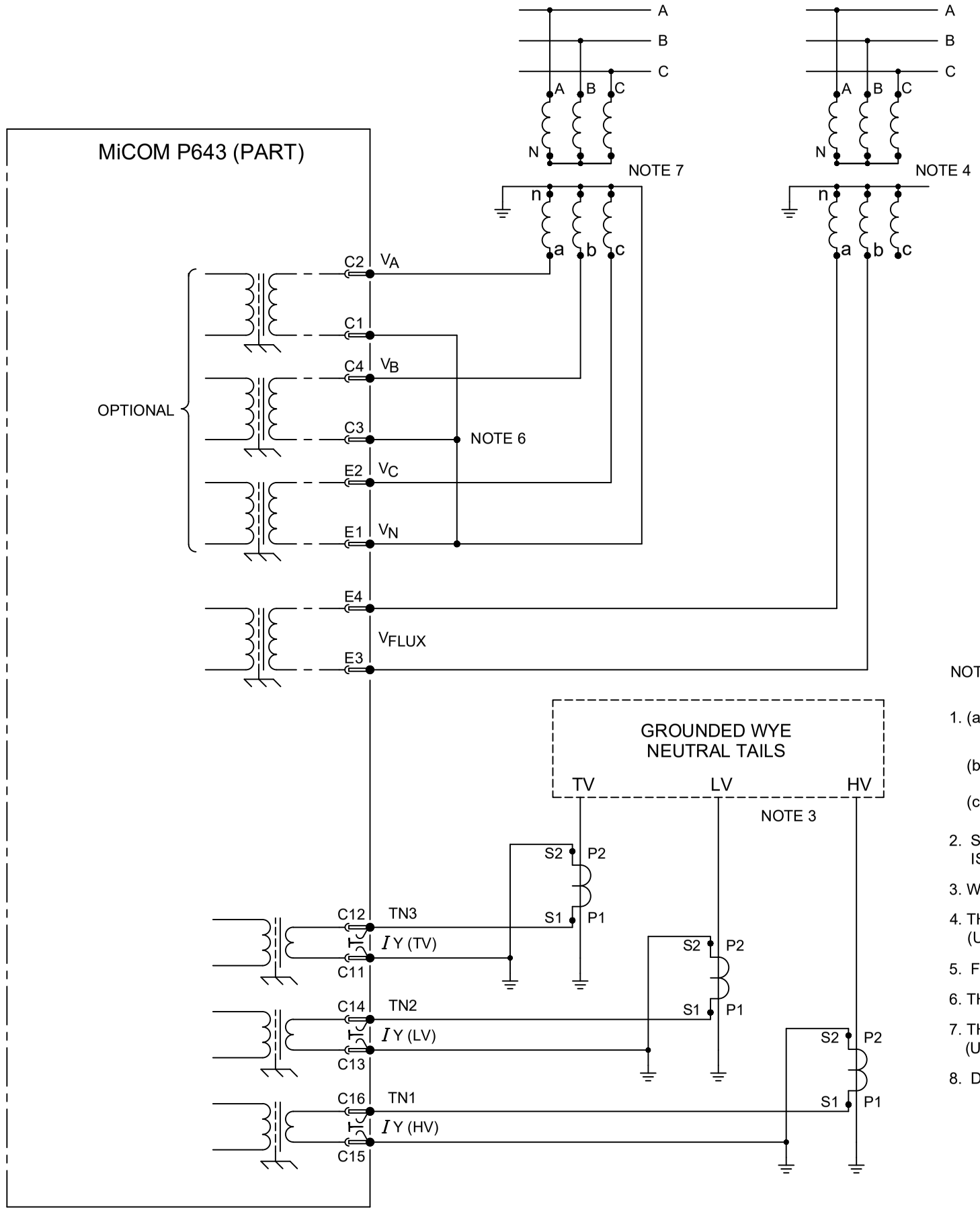
FINISH :-

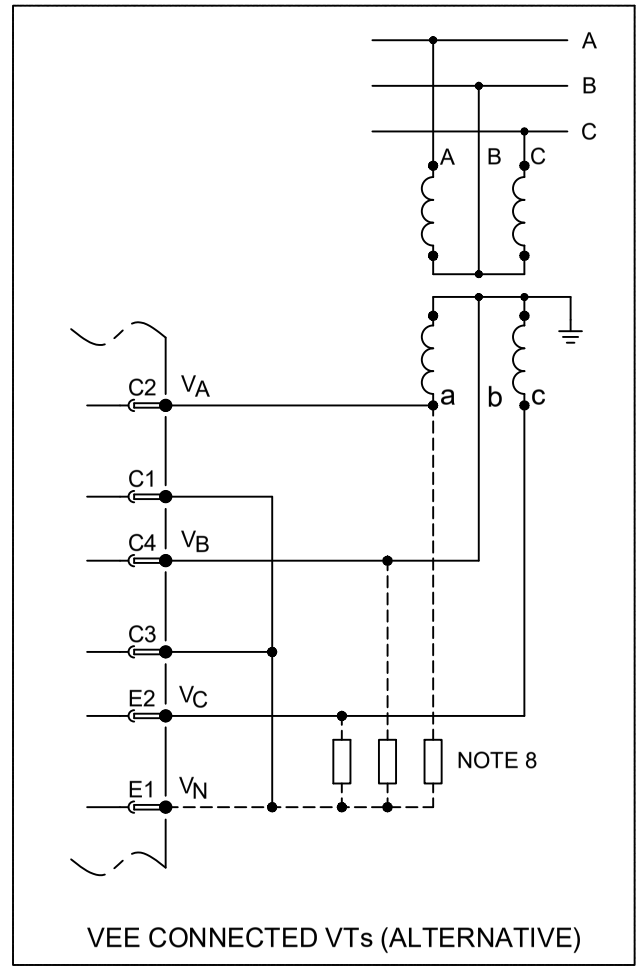
NEXT STAGE :-



SEE SHEET 2 FOR NOTES

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (20I/20O) 60TE		
Date: 03/03/2023	Name: S WOOTTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64345	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (20I/20O) 60TE	
Date: 18/04/2023	Name: S WOOTTON		Drg No: 10P64345	Sht: 2
Date:	Chkd:			Next Sht: -

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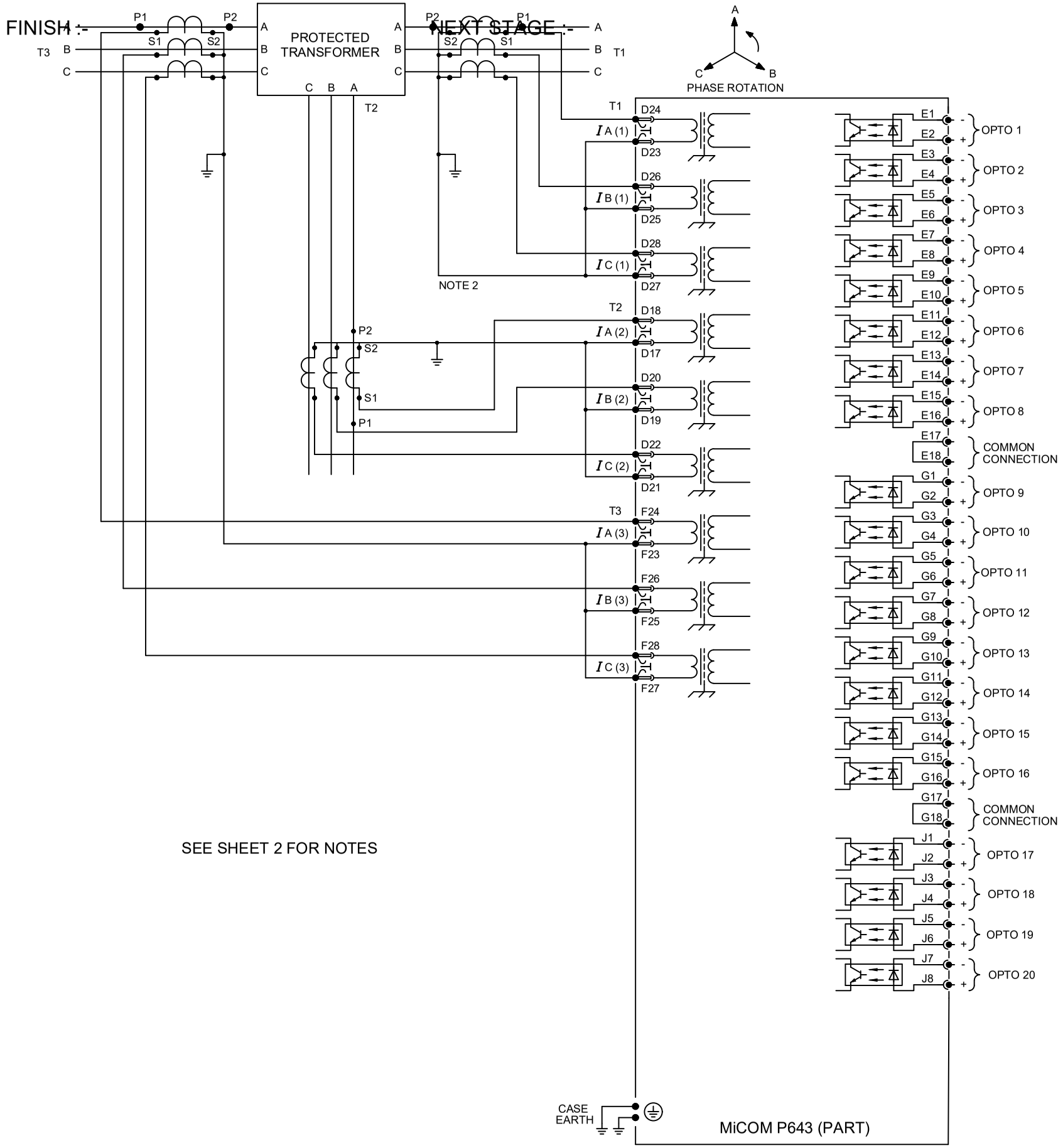
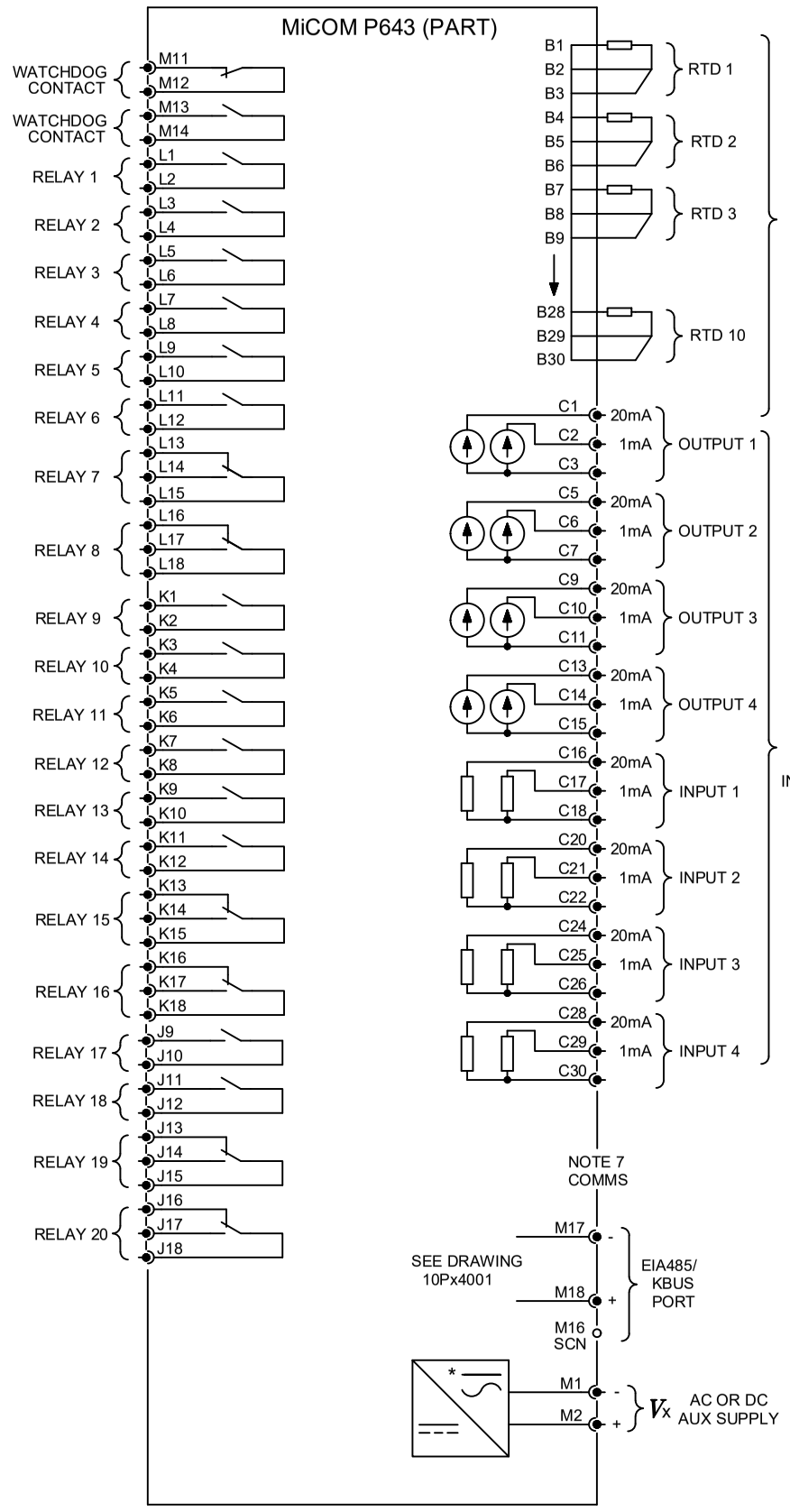
Harry Kerr Drive,
Stafford.
ST16 1WT, UK.

FINISH :-

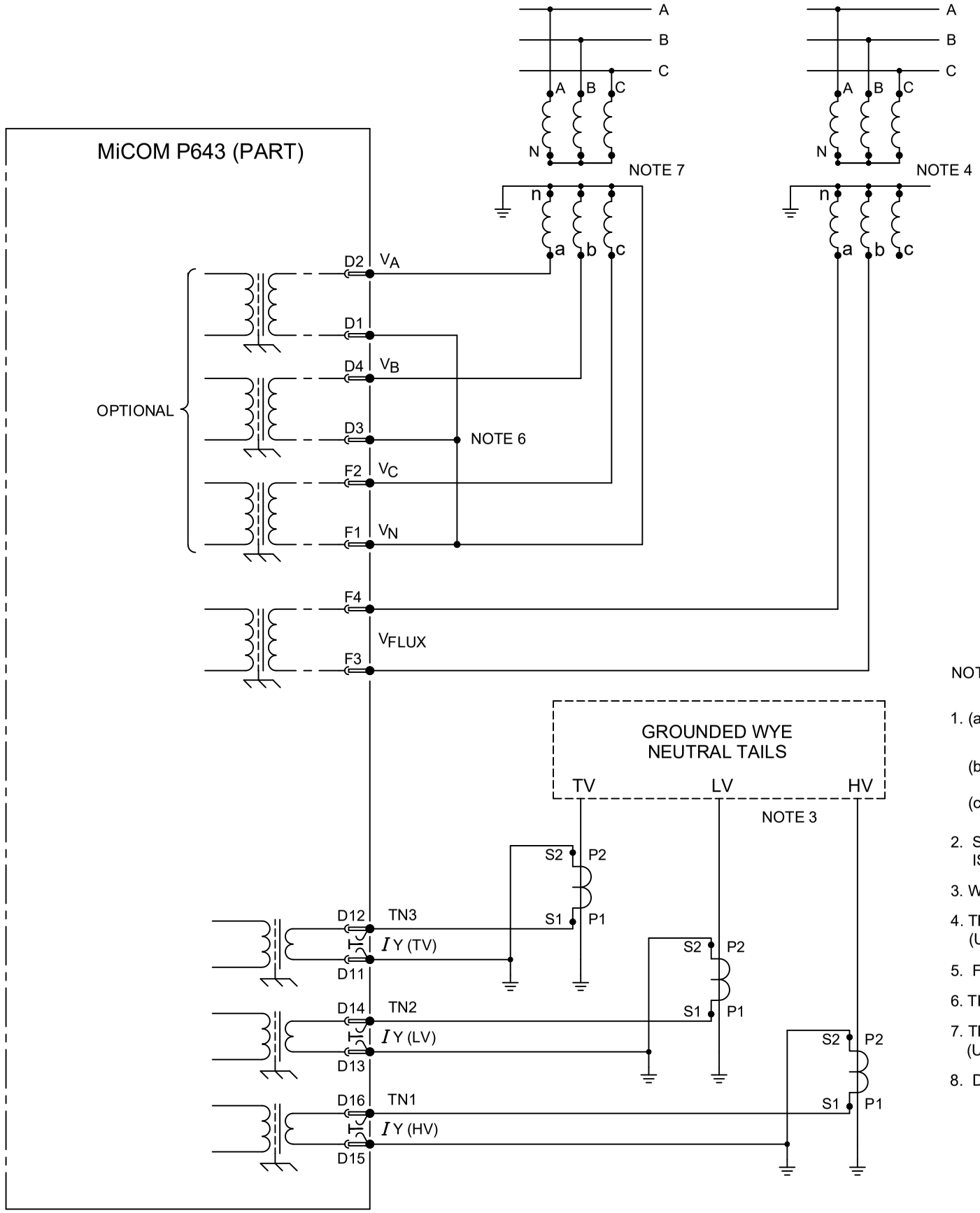
NEXT STAGE :-

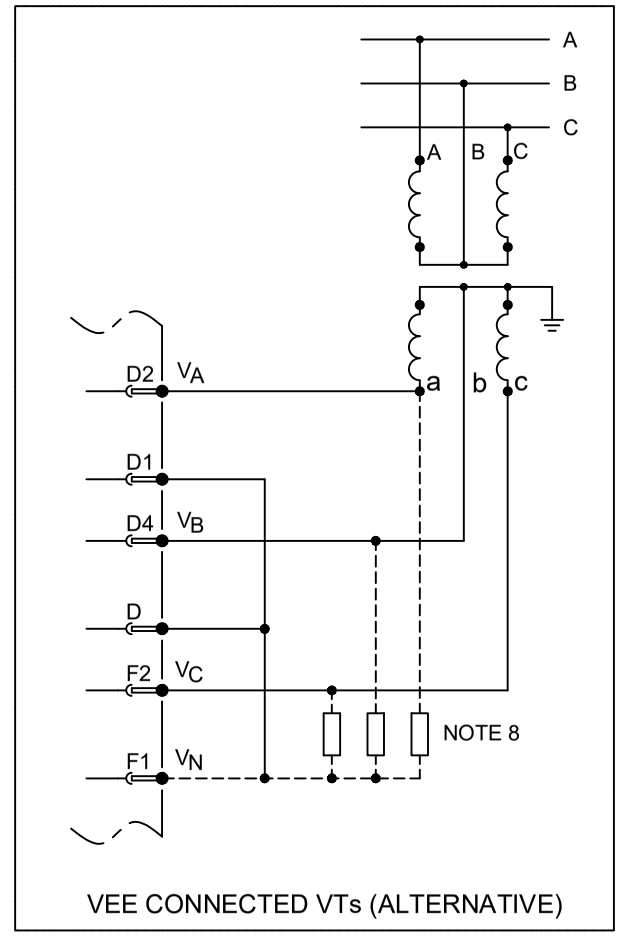


SEE SHEET 2 FOR NOTES



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS		
Date: 27/06/2023	Name: S WOOTTON		Drg No: 10P64342	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

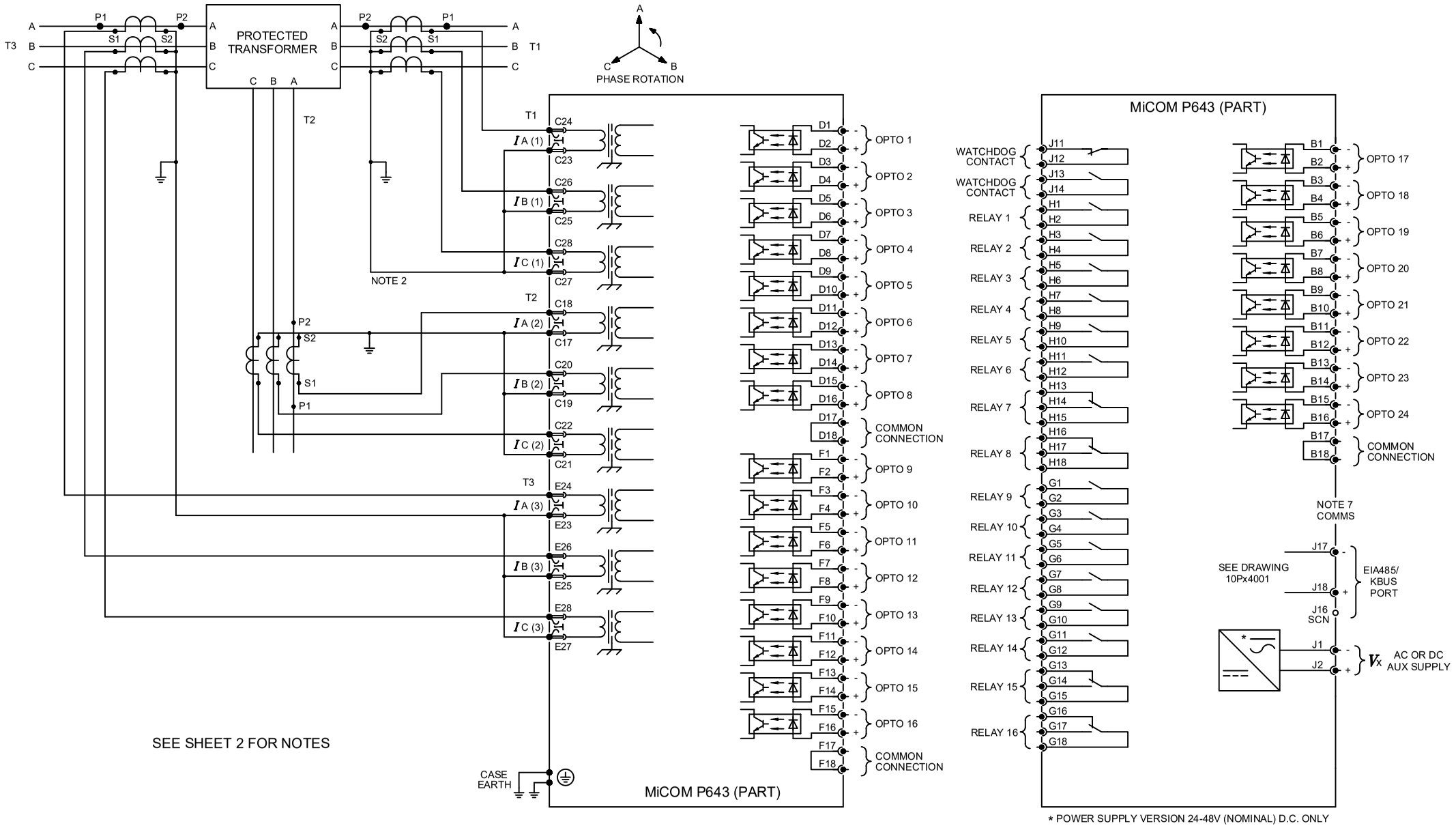




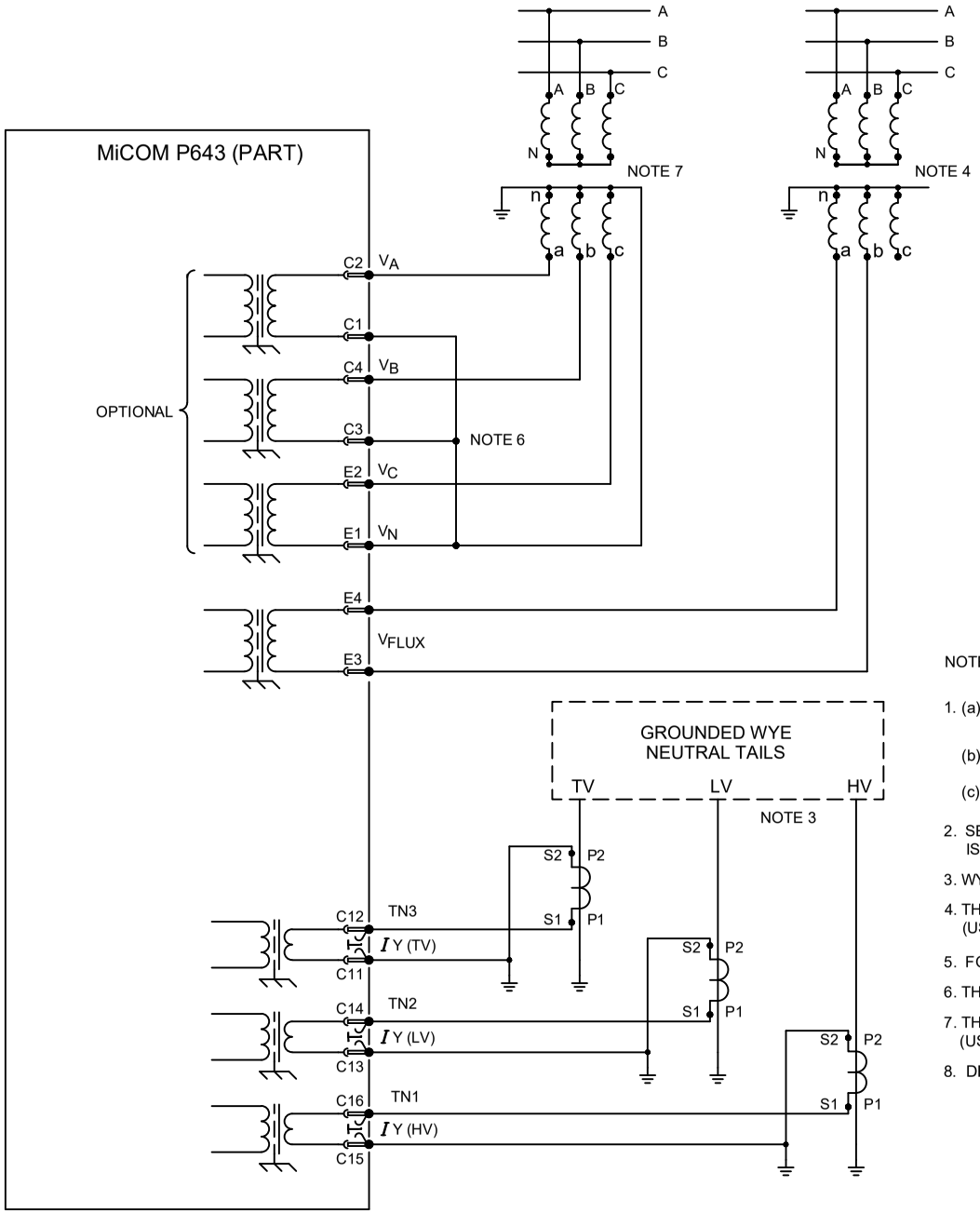
NOTES:

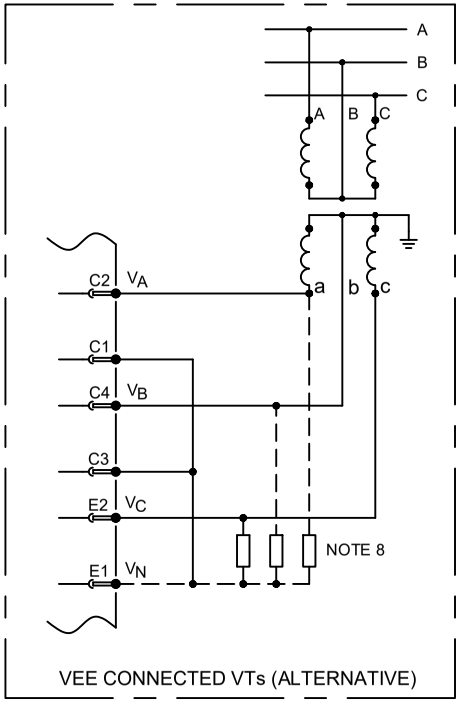
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF WITH 4 POLE VT INPUTS (20I/20O)) 80TE		
Date: 27/06/2023	Name: S WOOTTON		Drg No: 10P64342	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: H	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/O & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64304	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

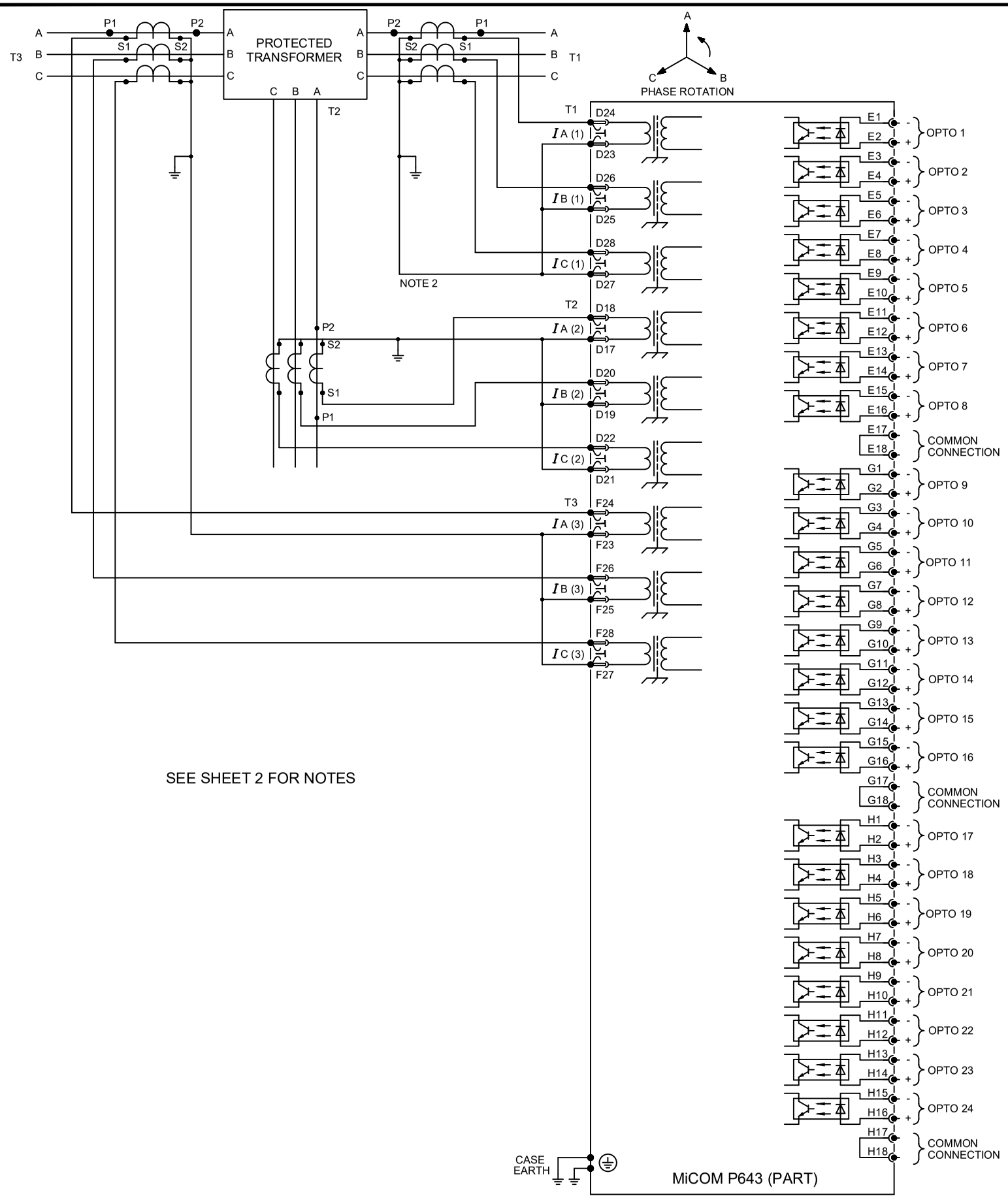




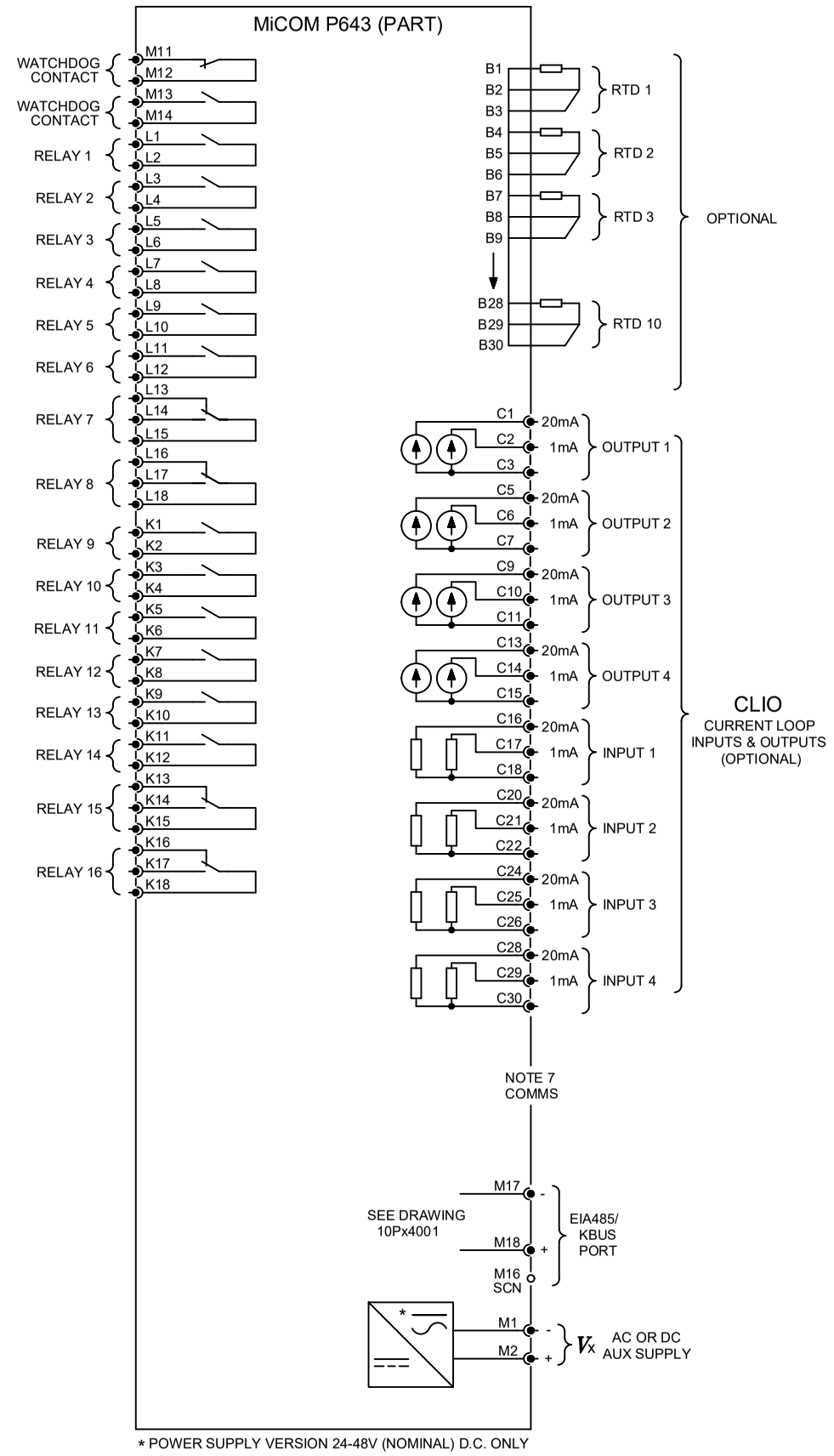
NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

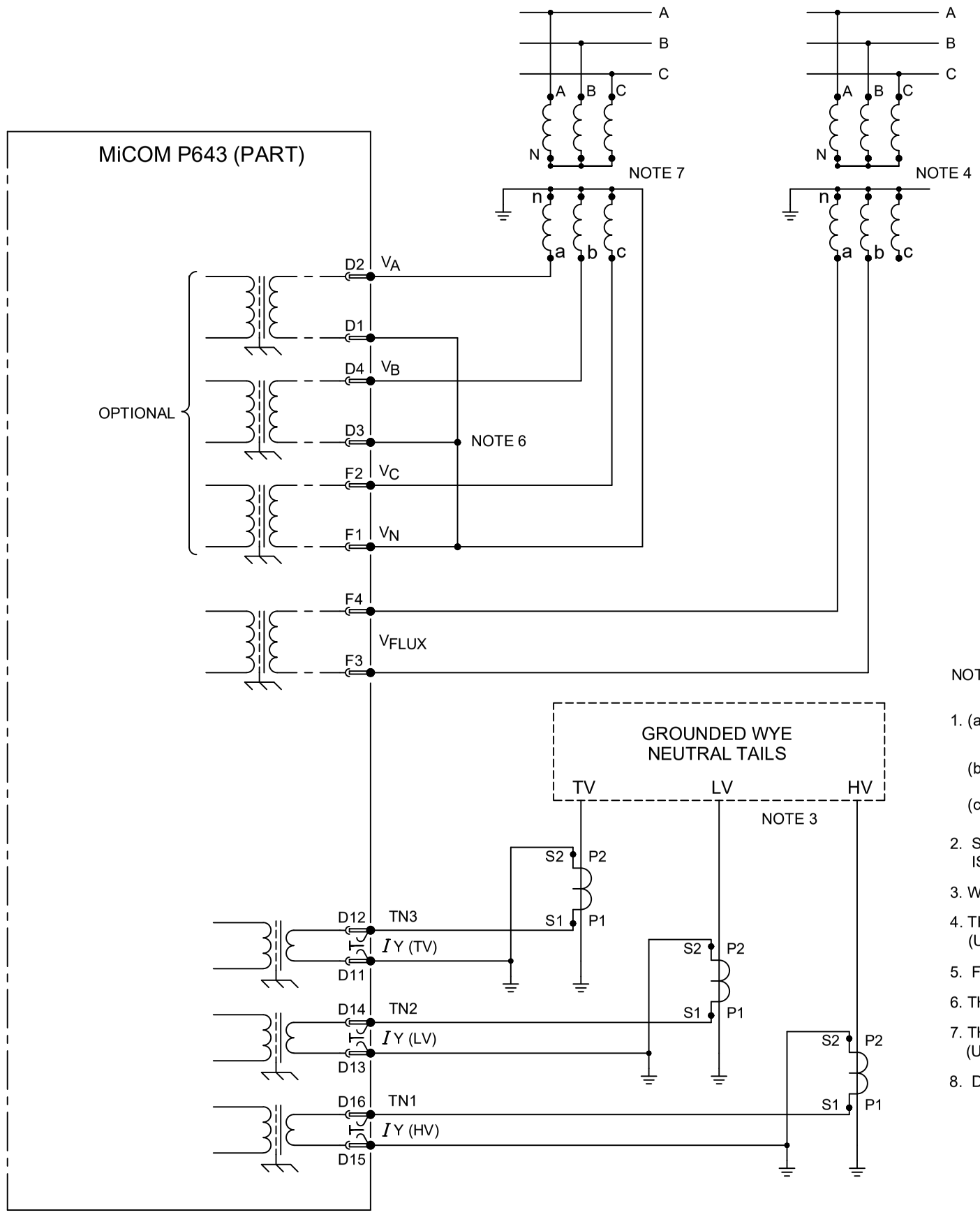
Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 3 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/O & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64304	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

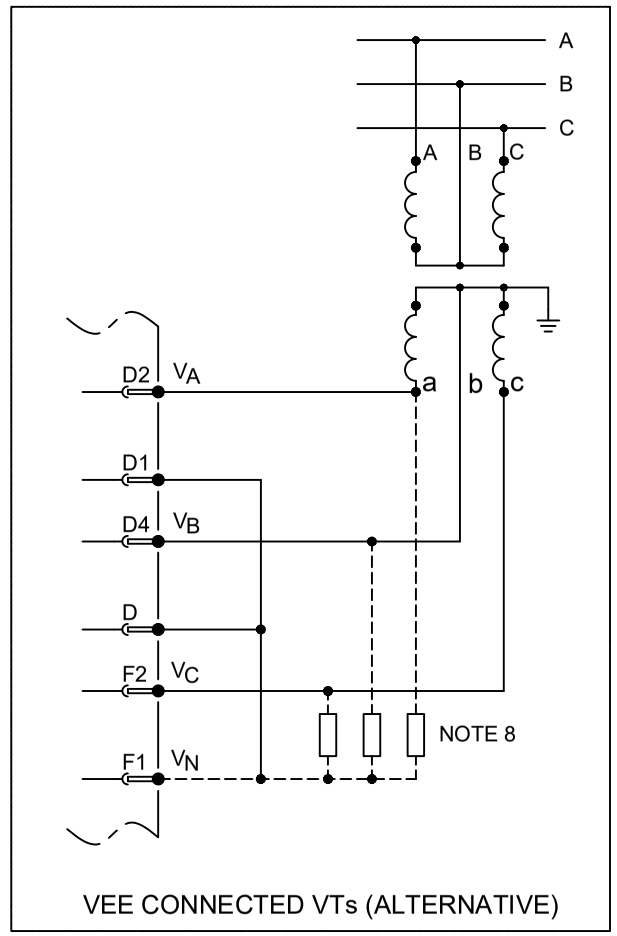


SEE SHEET 2 FOR NOTES



Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 06/07/2023	Name: S WOOTTON		Drg No: **10P64362**	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
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5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (24I/16O) 80TE	
Date: 06/07/2023	Name: S WOOTTON		Drg No: 10P64362	Sht: 2
Date:	Chkd: S SWAIN			Next Sht: -

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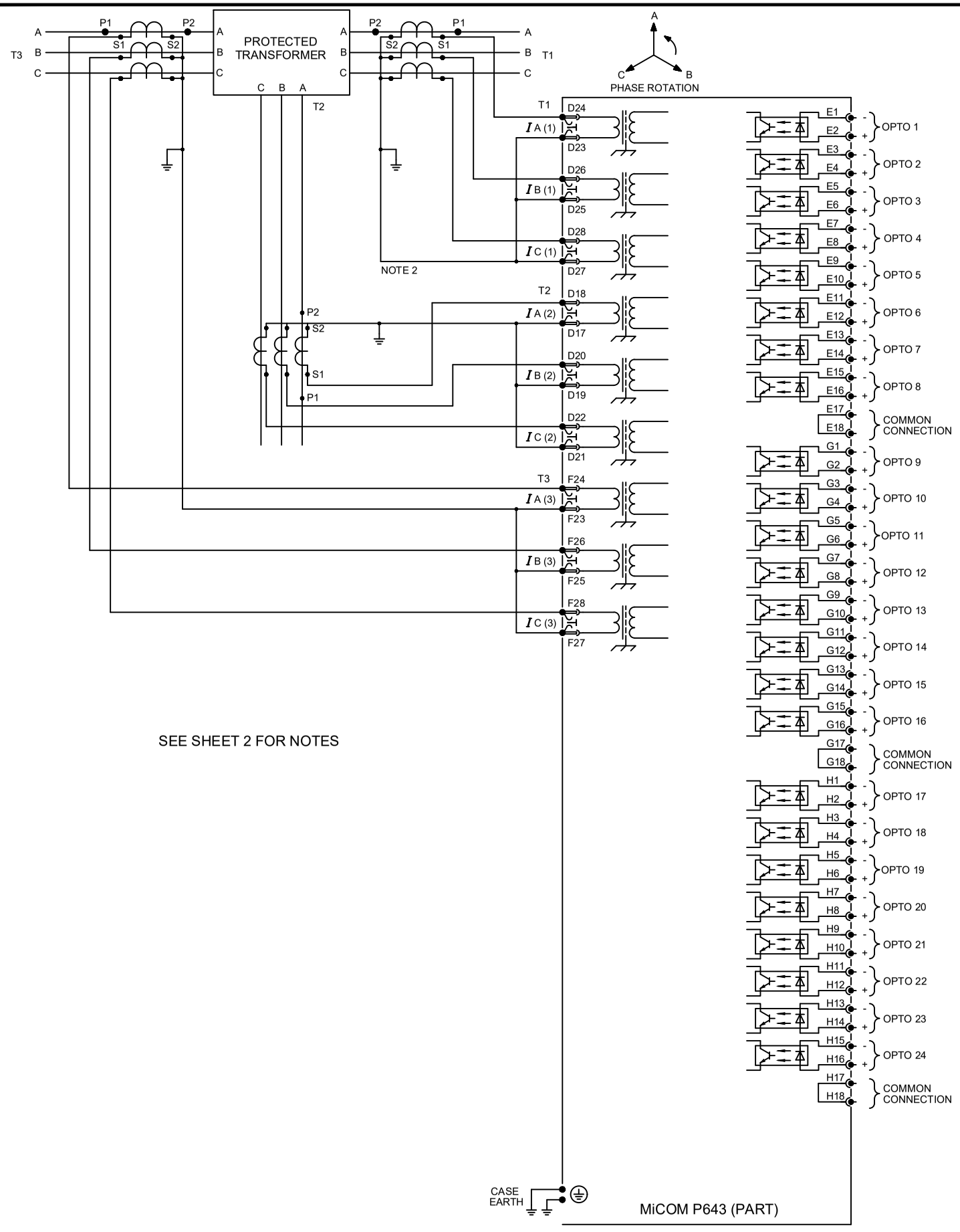
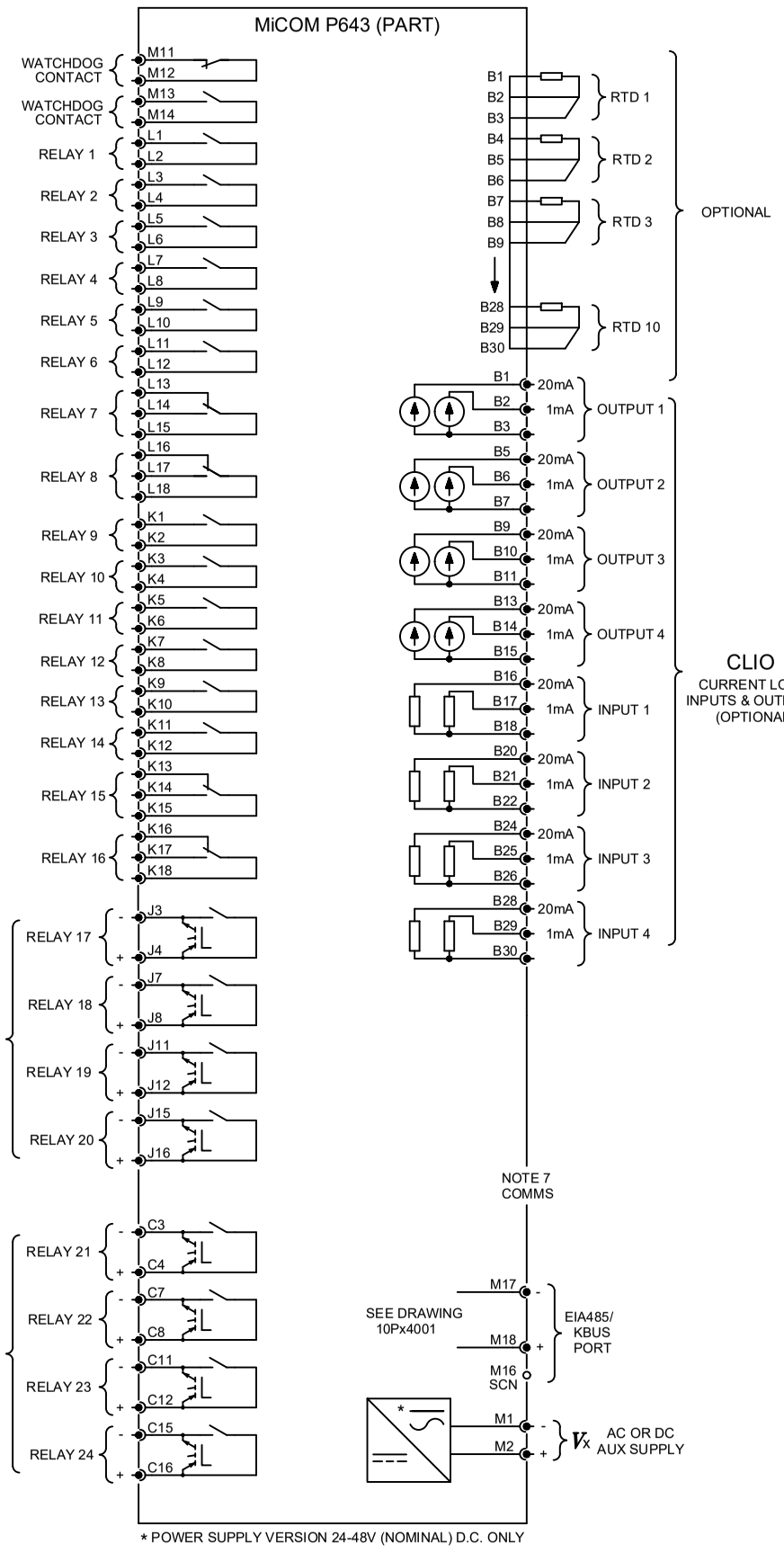
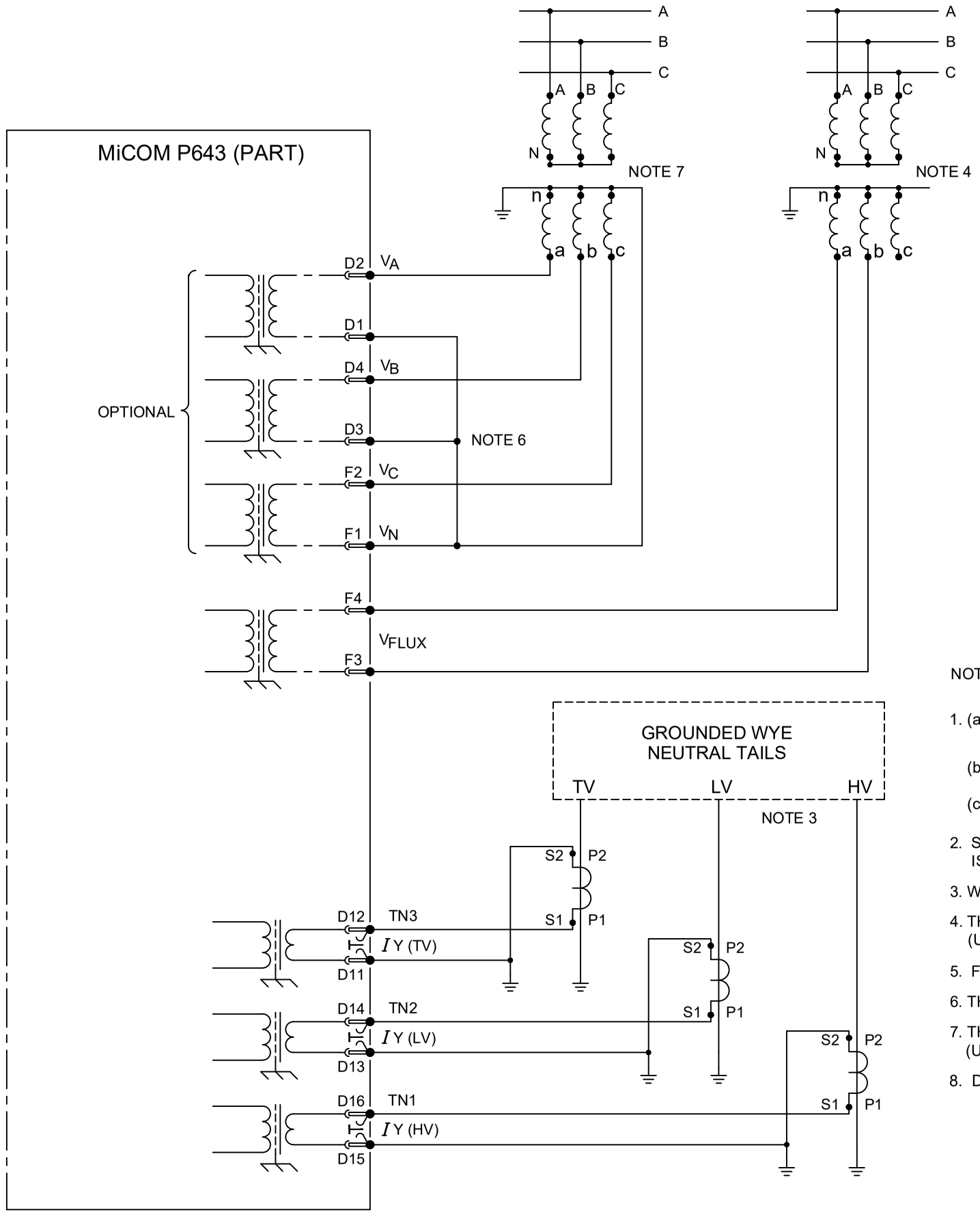
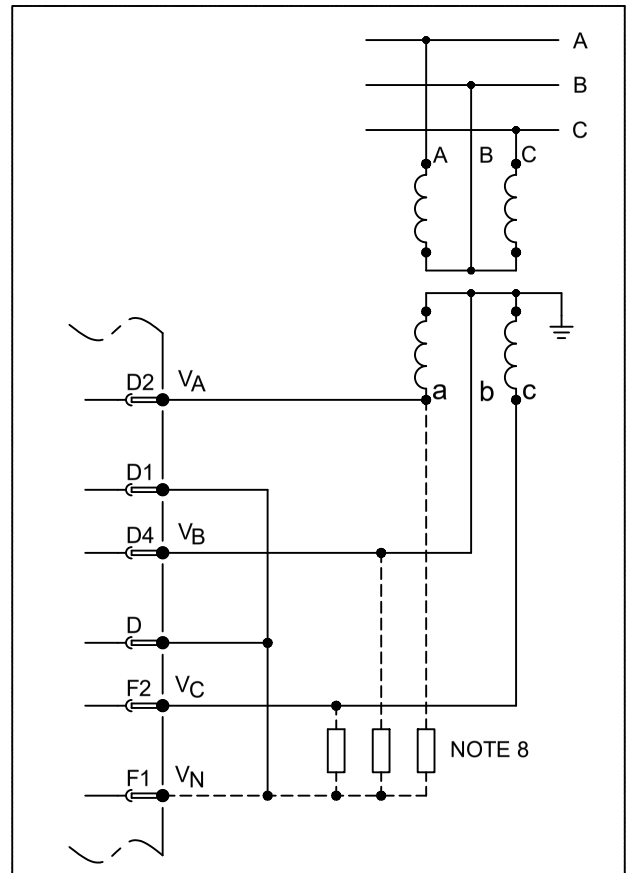


SEE SHEET 2 FOR NOTES



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (24I/16O + 8 HB RELAYS) 80TE		
Date: 24/07/2023	Name: S WOOTTON		Drg No: 10P64363	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
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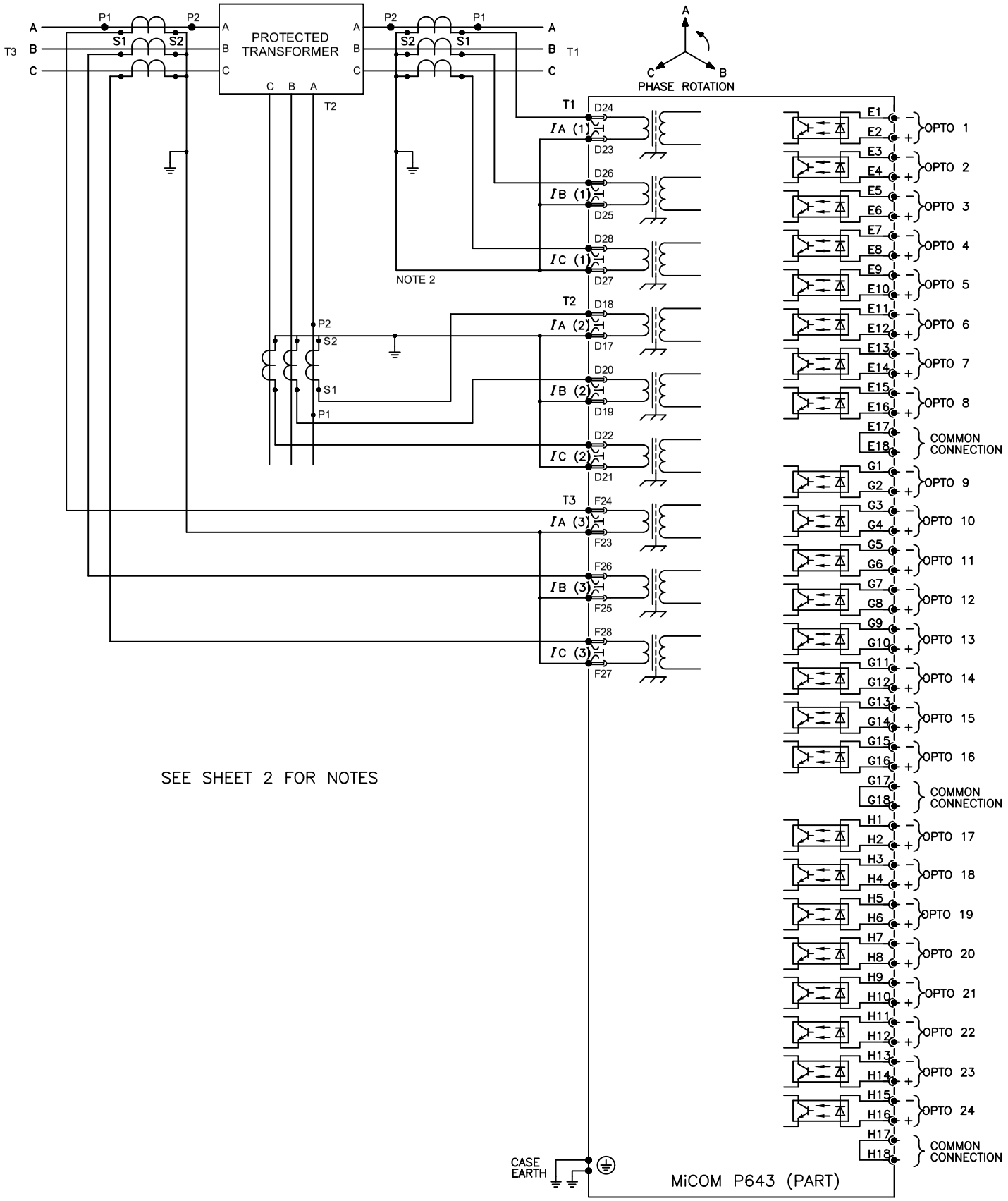
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

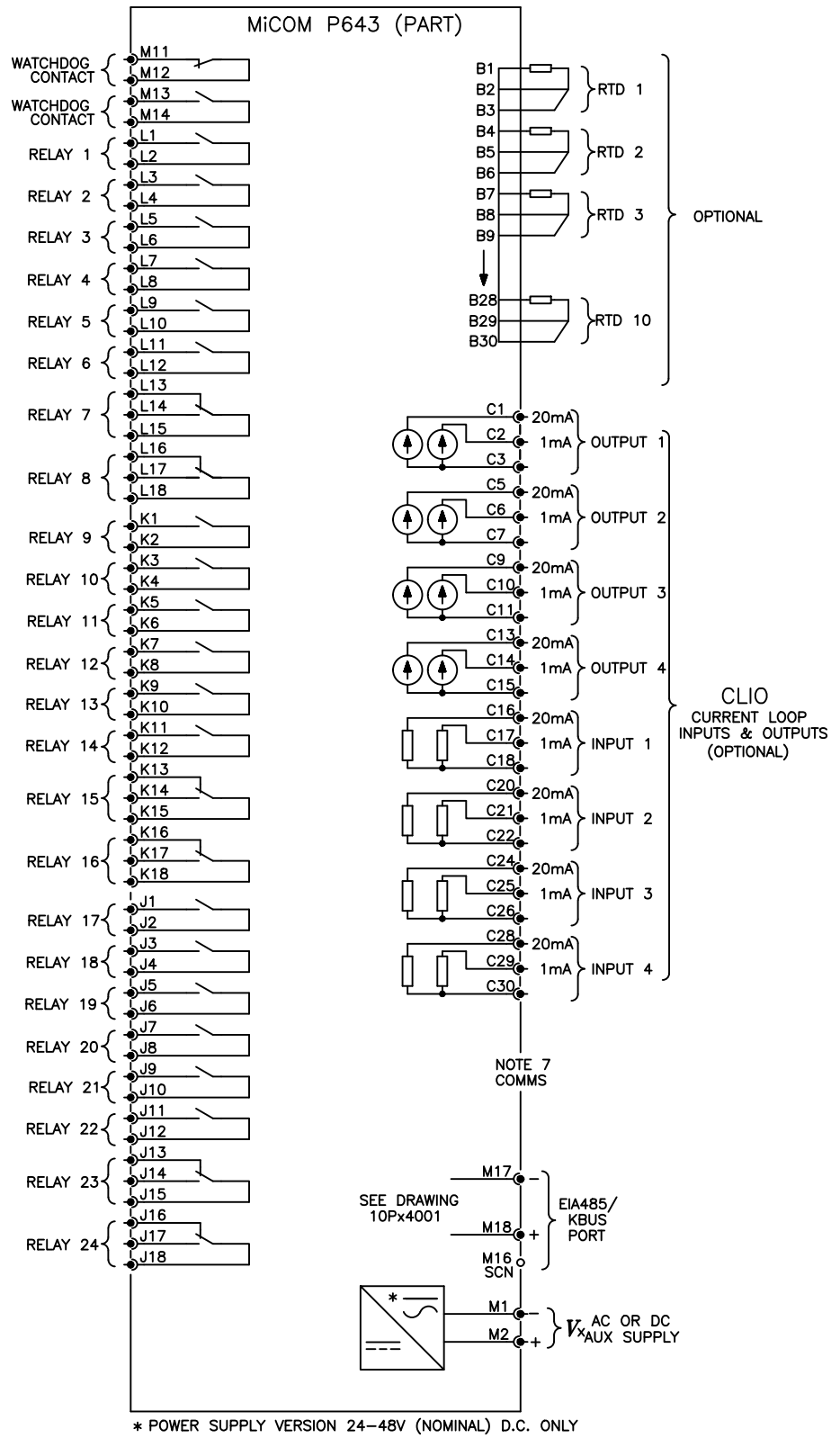
Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (24I/16O + 8 HB RELAYS) 80TE		
Date: 24/07/2023	Name: S WOOTTON		Drg No: 10P64363	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

FINISH :-

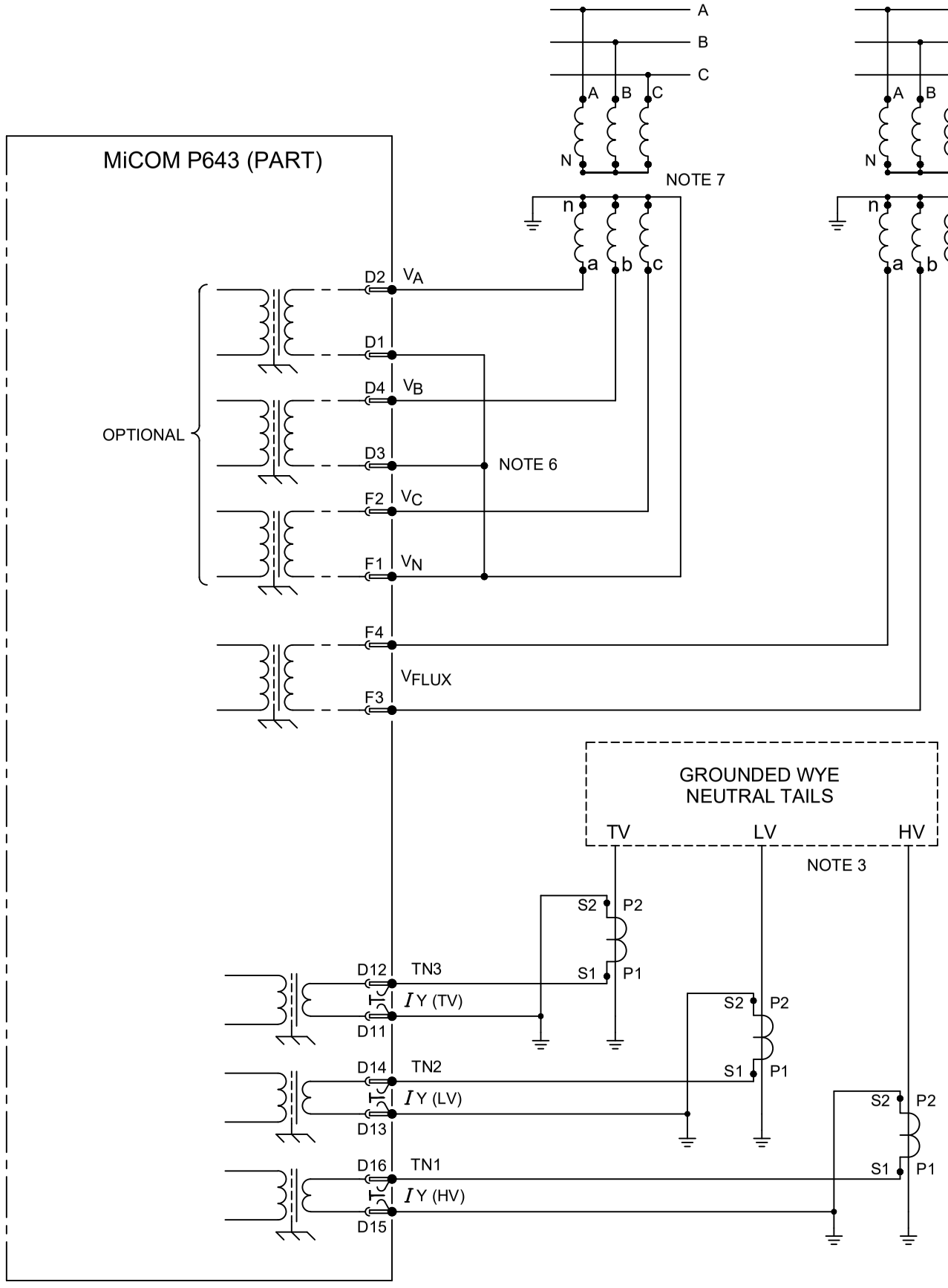
NEXT STAGE :-

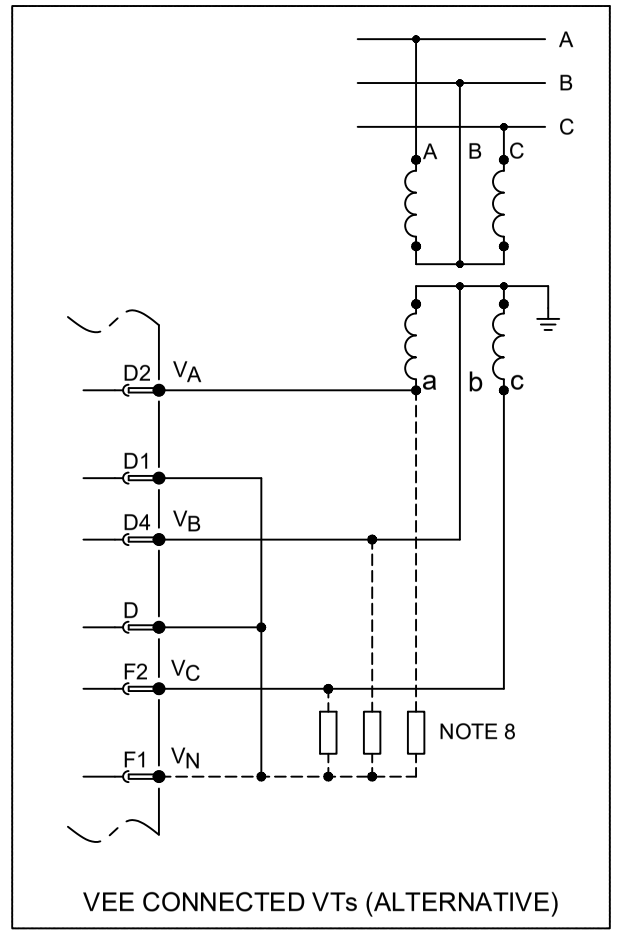


SEE SHEET 2 FOR NOTES



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24 I/P & 24 O/P) 80TE		
Date: 15/03/2023	Name: S WOOTTON		Drg No: 10P64352	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
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6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24 I/P & 24 O/P) 80TE	
Date: 20/04/2023	Name: S WOOTTON		Drg No: 10P64352	Sht: 2
Date:	Chkd:			Next Sht: -

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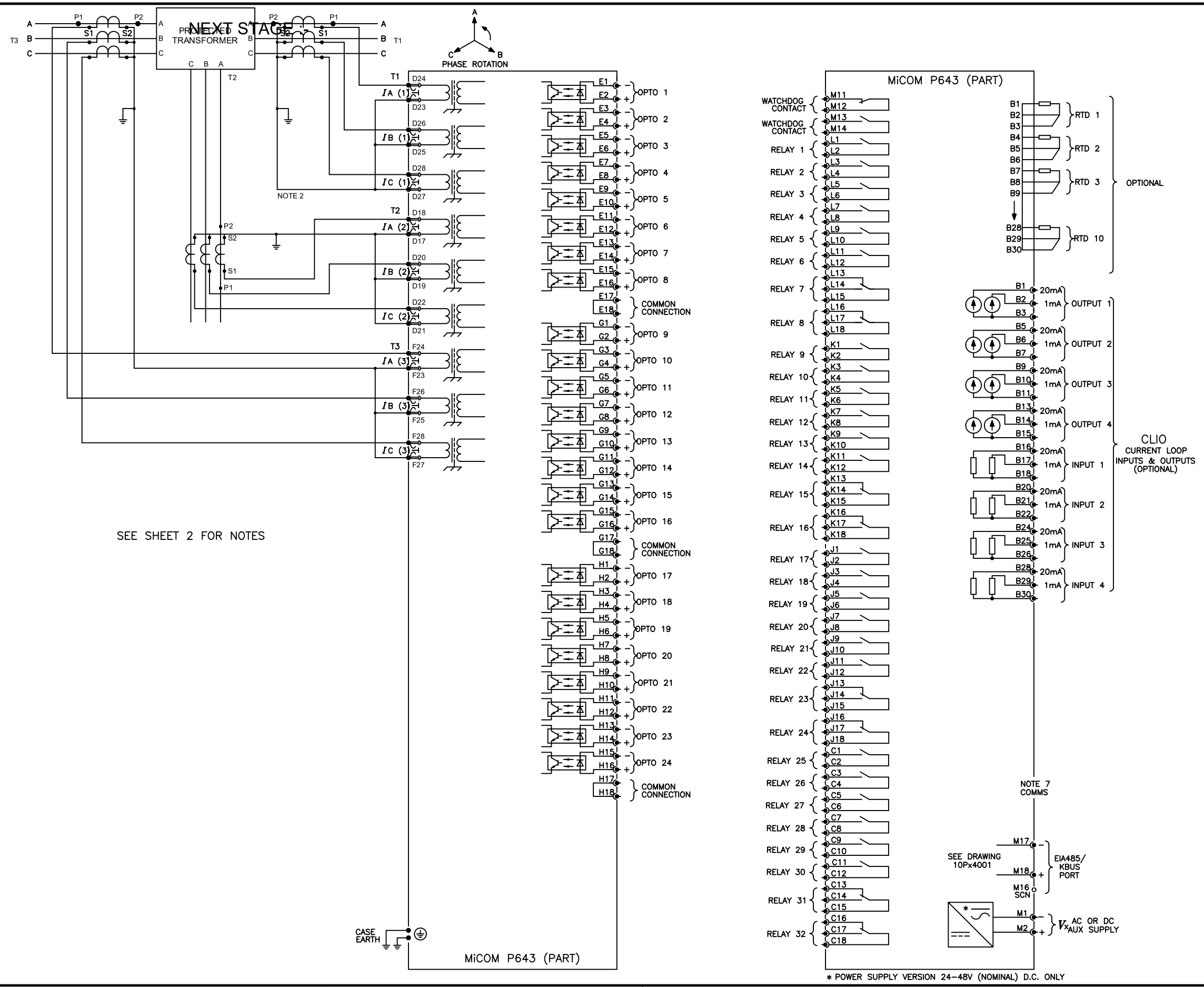
FINISH :-

NEXT STAGE



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title:	EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24 I/P & 32 O/P) 80TE	
Date: 15/08/2023	Name: S WOOTTON		Drg No:	10P64353	Sht: 1
Date:	Chkd:				Next Sht: 2

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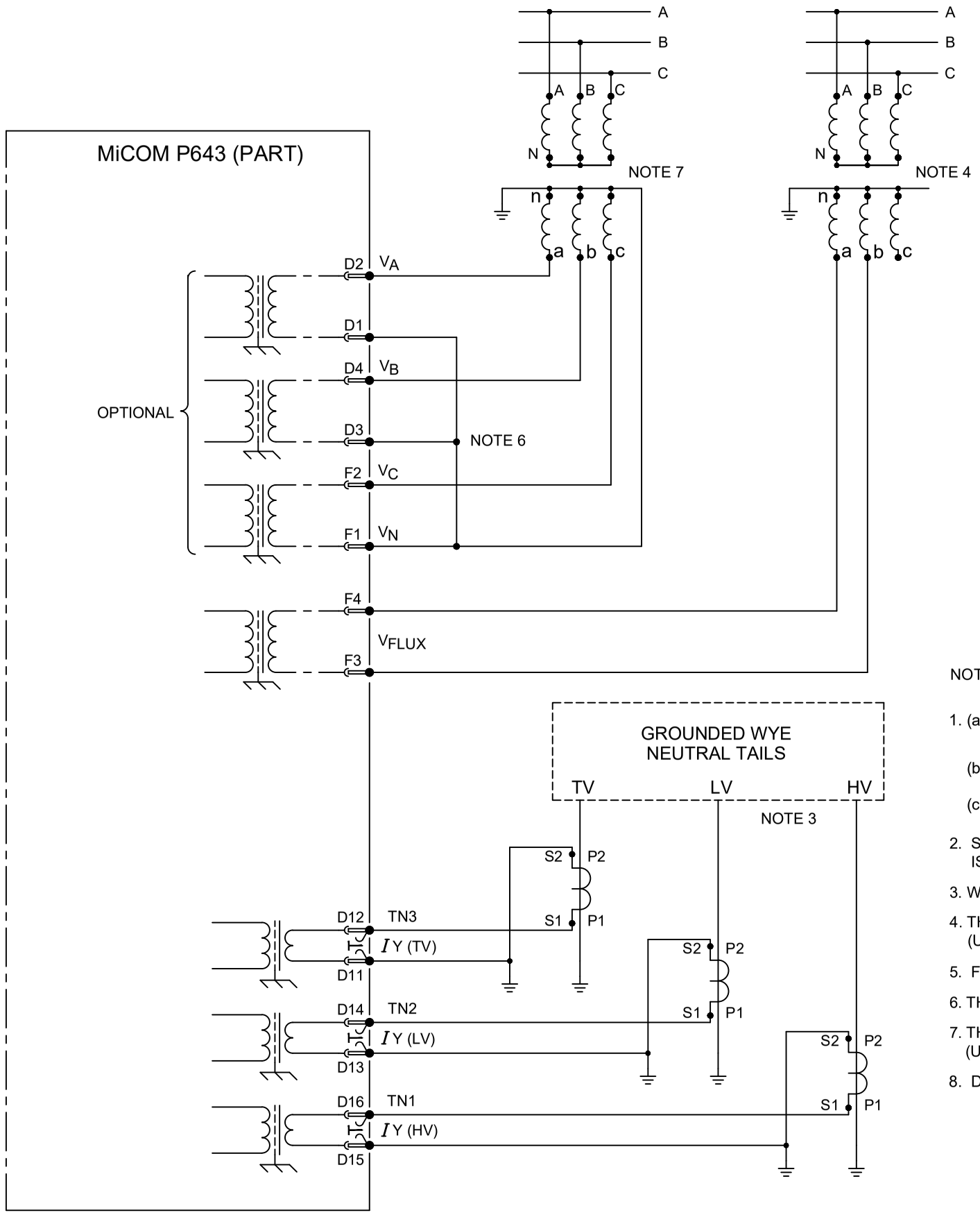
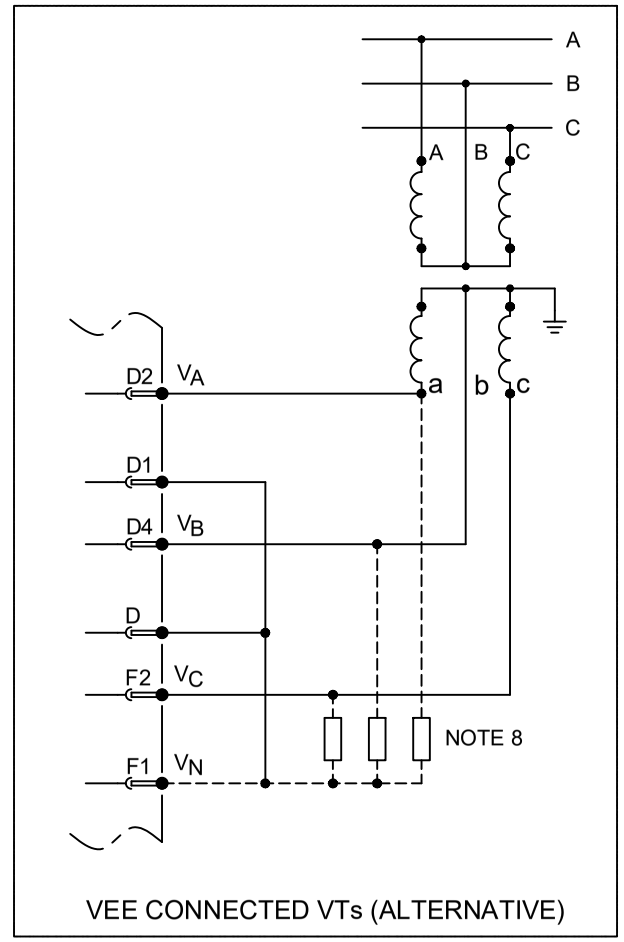
ST16 1WT, UK.





VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

   (b) TERMINAL.

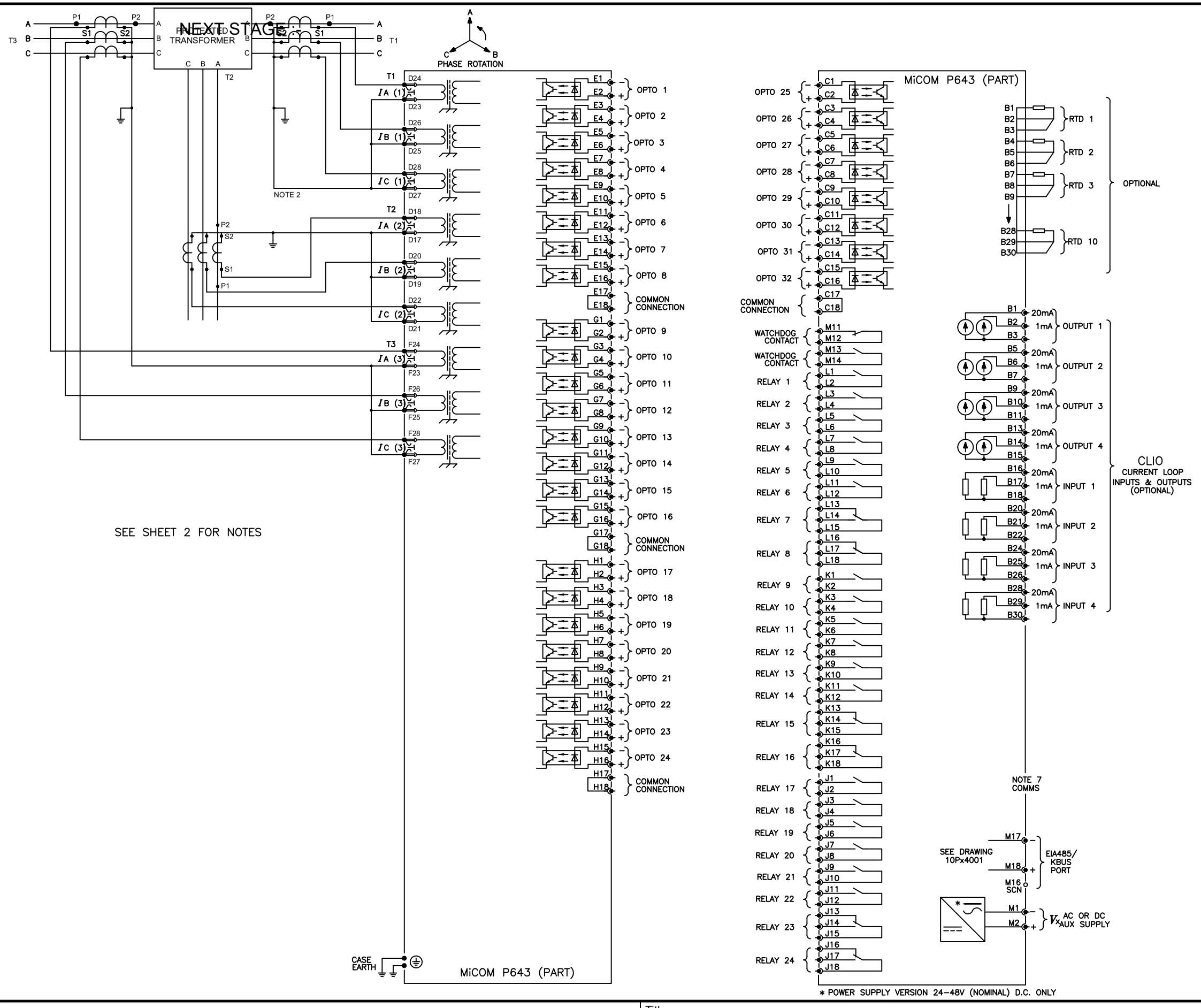
   (c) PIN TERMINAL (P.C.B. TYPE)

2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24 I/P & 32 O/P) 80TE		
Date: 21/04/2023	Name: S WOOTTON		Drg No: 10P64353	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	

FINISH :-

NEXT STAGE :-



Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/24O) 80TE		
Date: 14/08/2023	Name: S WOOTTON		Drg No: 10P64374	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

FINISH :-

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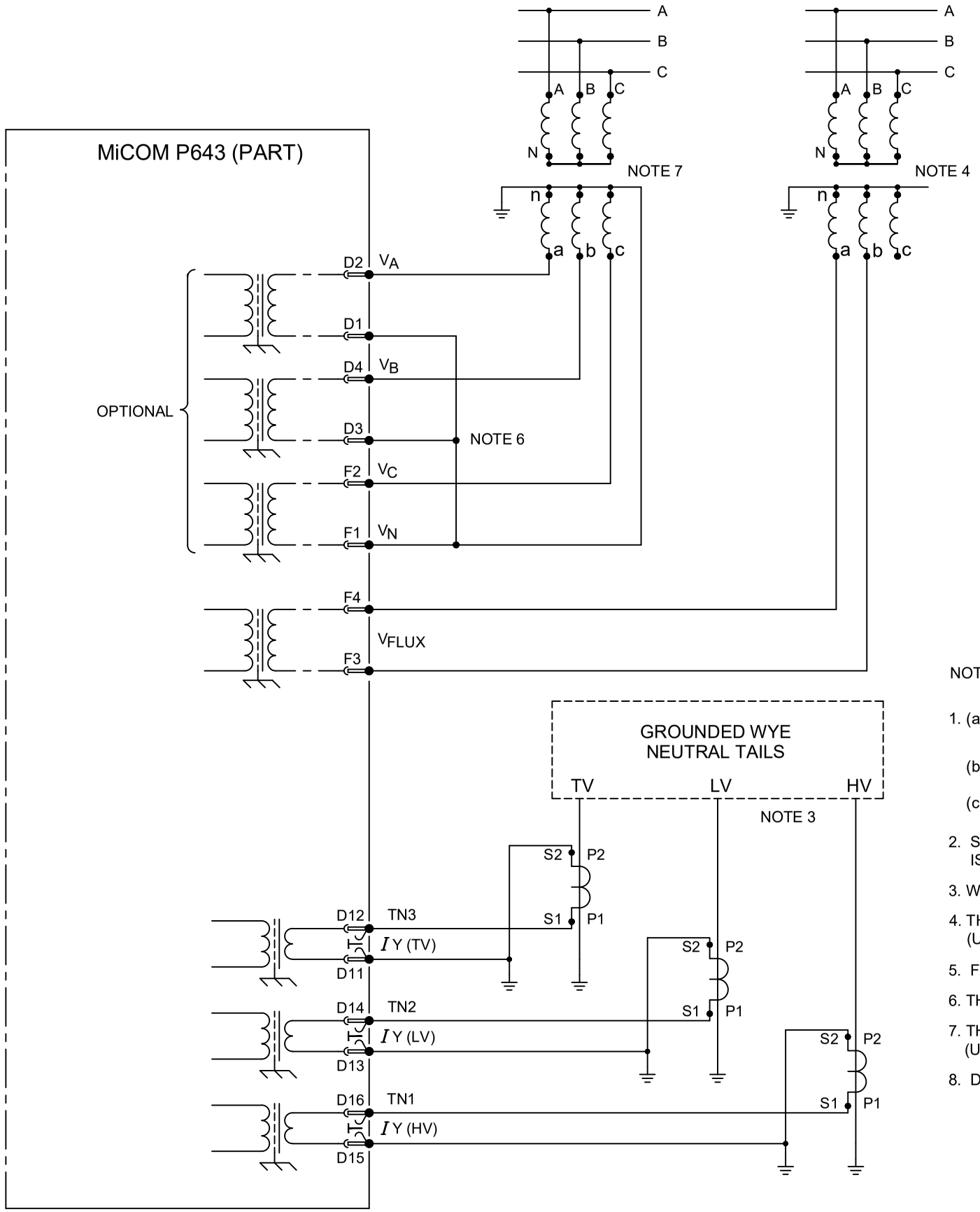
MiCOM P643 (PART)
A
B
C
N
NOTE 7
n
a
b
c
D2
VA
D1
D4
VB
OPTIONAL
D3
NOTE 6
F2
VC
F1
VN
F4
VFLUX
F3
GROUNDED WYE
NEUTRAL TAILS
TV
LV
HV
NOTE 3
S2
P2
S1
P1
D12
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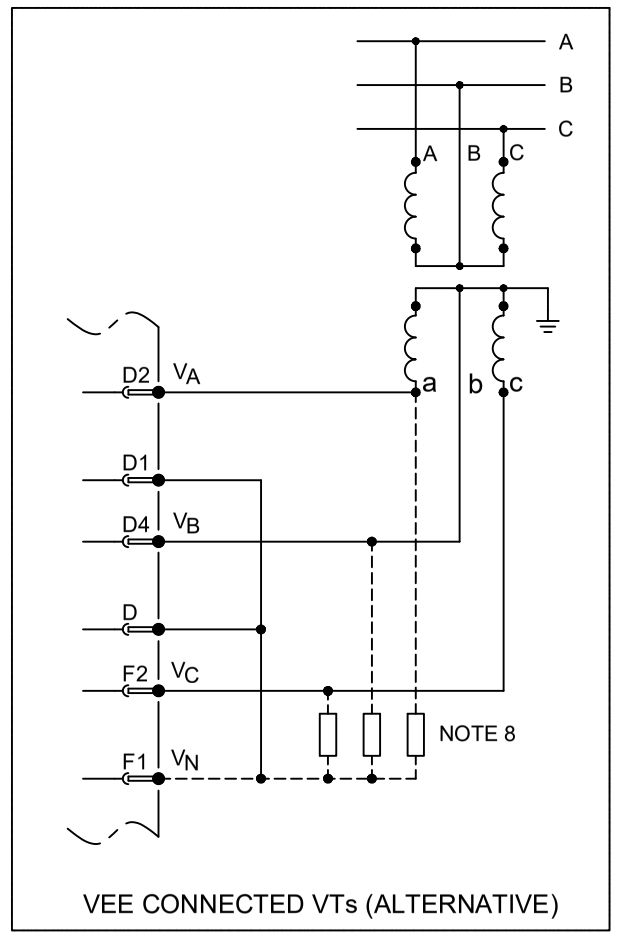
D11
D14
TN2
IY (LV)
D13
D16
TN1
IY (HV)
D15
NOTE 4



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/24O) 80TE	
Date: 14/08/2023	Name: S WOOTTON		Drg No: 10P64374	Sht: 2
Date:	Chkd:			Next Sht: -

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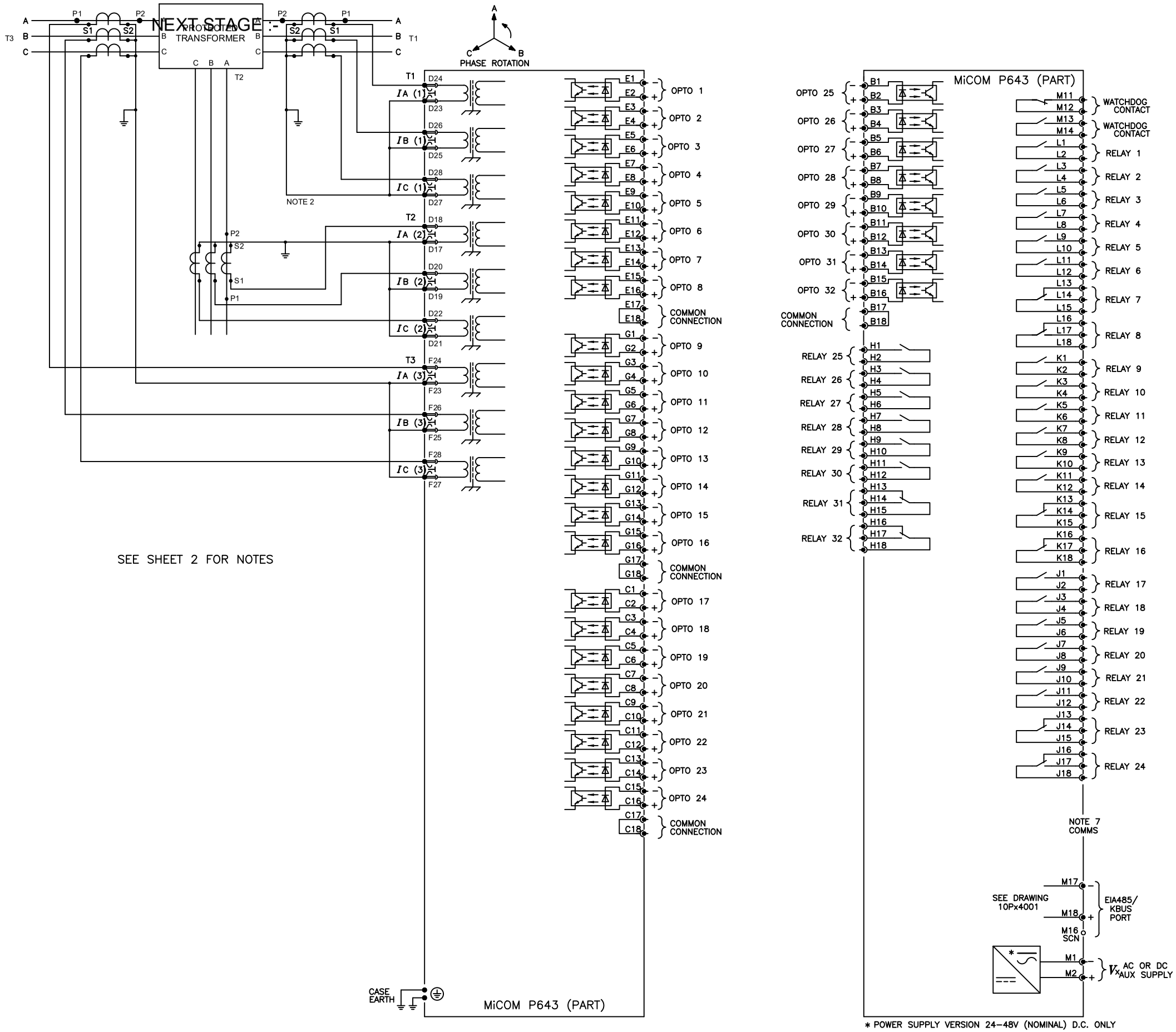

SEE SHEET 2 FOR NOTES

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/32O) 80TE	
Date: 14/08/2023	Name: S WOOTTON		Drg No: 10P64377	Sht: 1
Date:	Chkd:			Next Sht: 2

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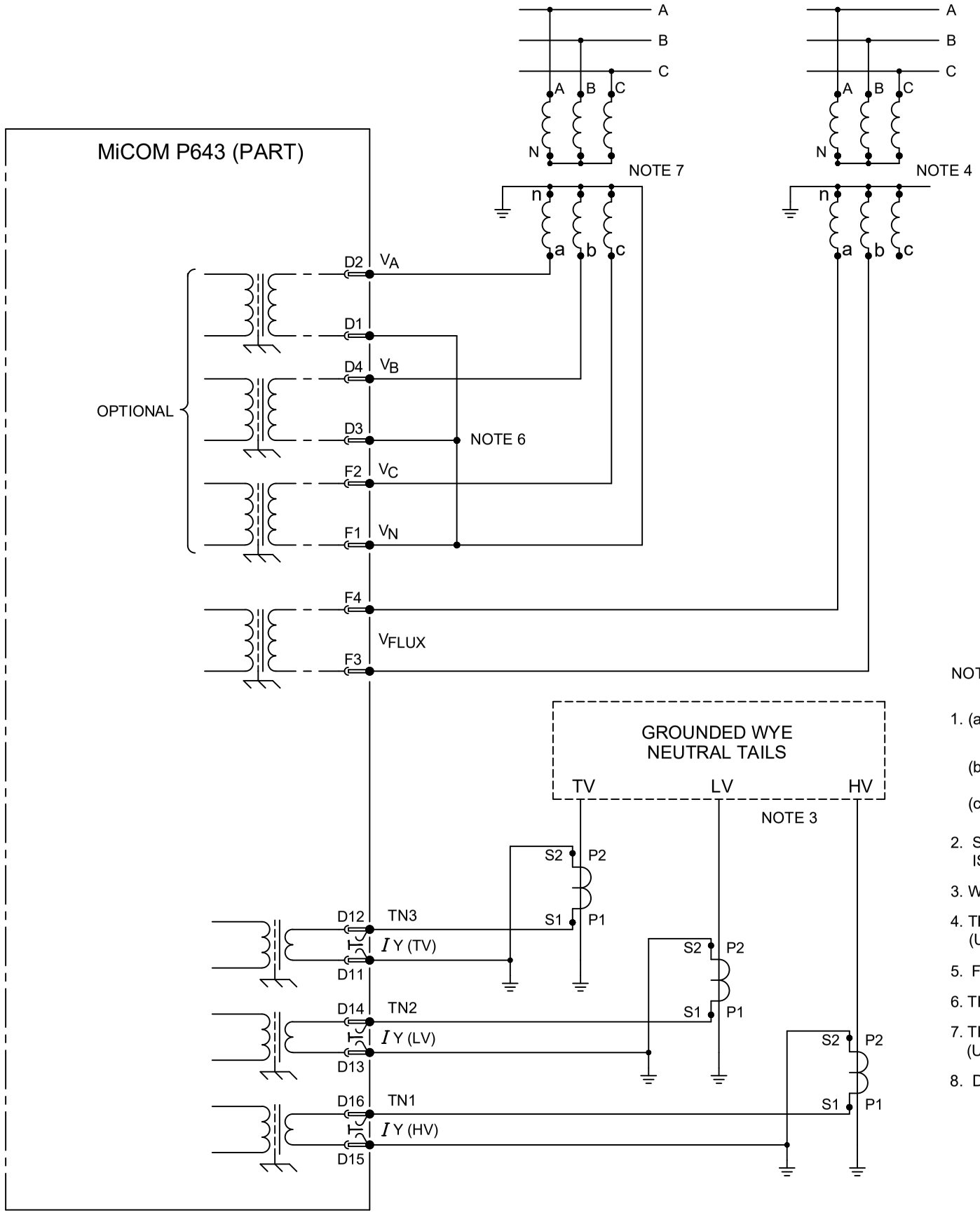

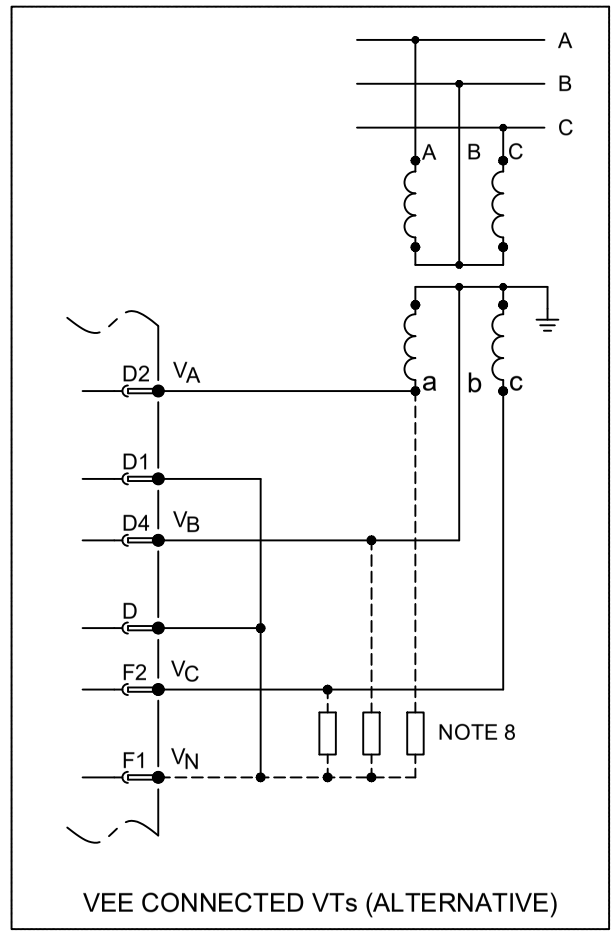

VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/32O) 80TE	
Date: 14/08/2023	Name: S WOOTTON		Drg No: 10P64377	Sht: 2
Date:	Chkd:			Next Sht: -

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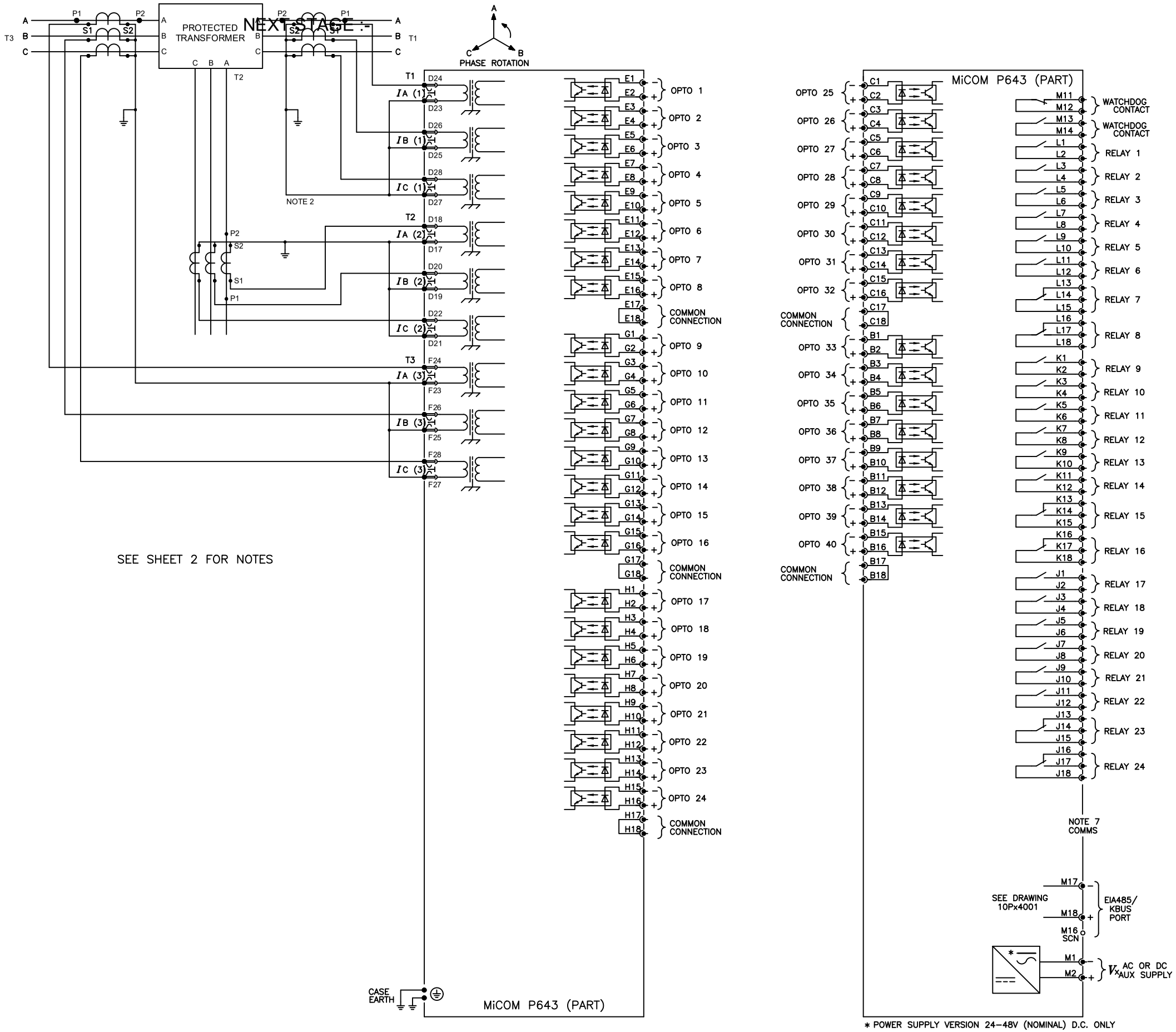
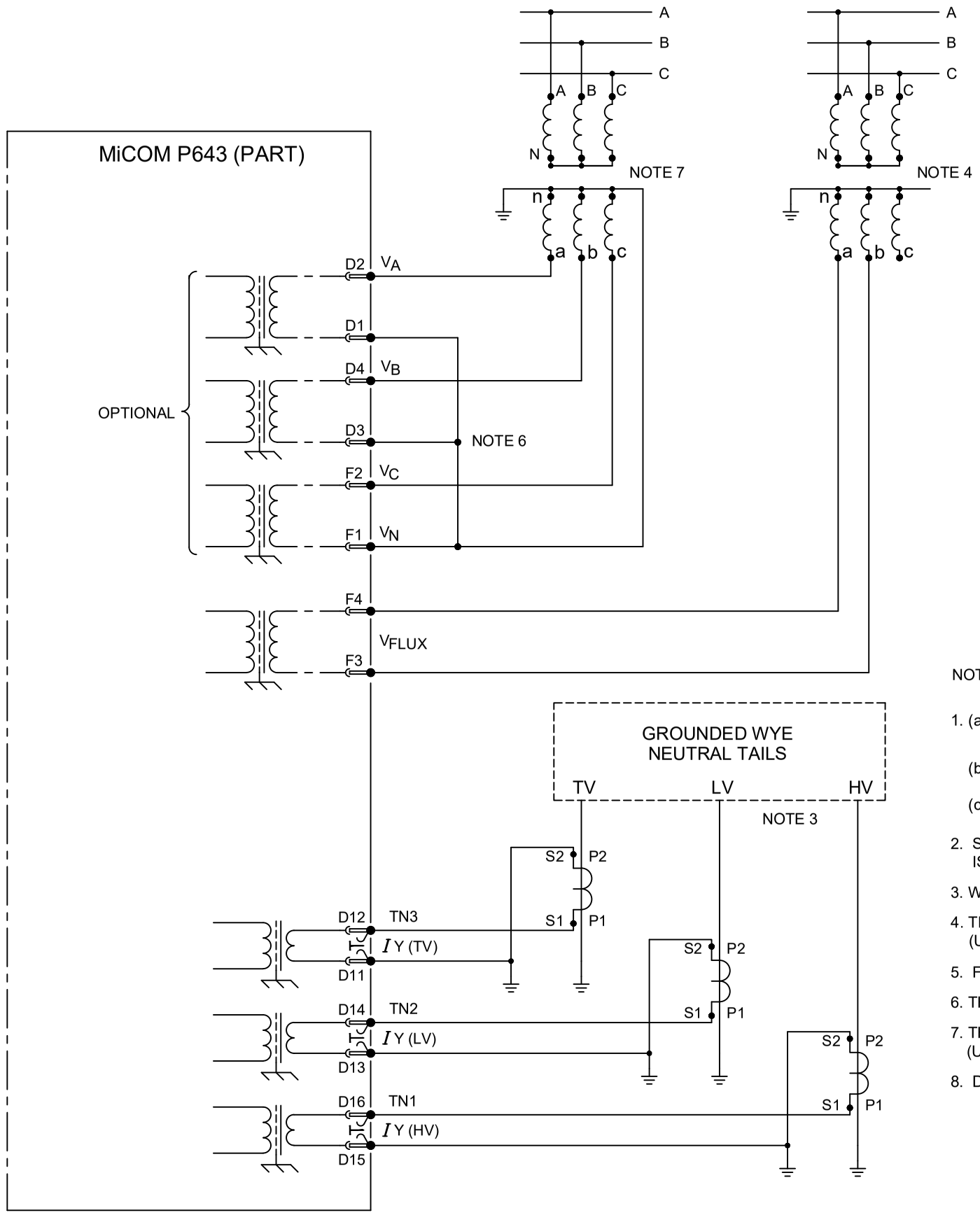
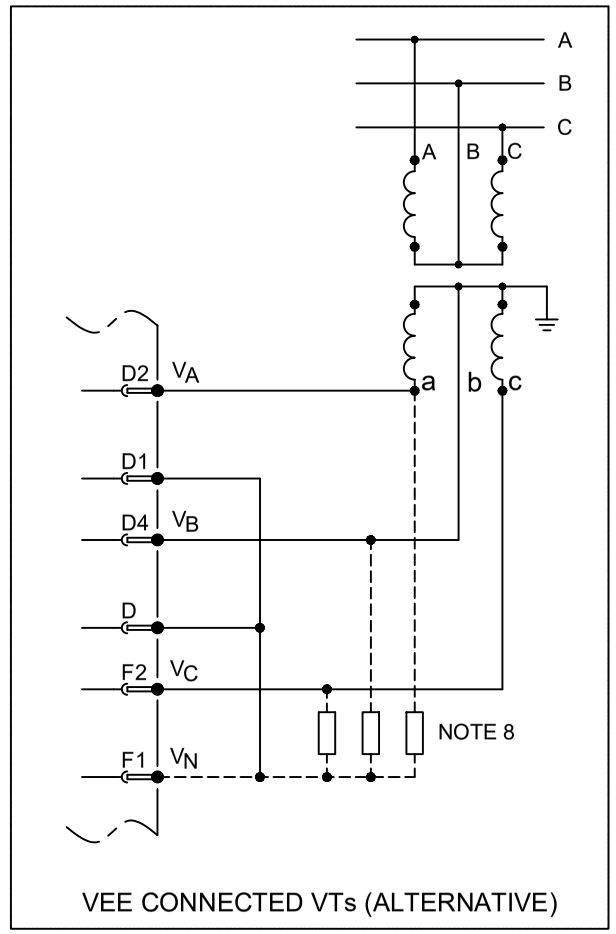


SEE SHEET 2 FOR NOTES

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (40I/24O) 80TE		
Date: 16/03/2023	Name: S WOOTTON		Drg No: 10P64355	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





VEE CONNECTED VTs (ALTERNATIVE)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (40I/24O) 80TE	
Date: 24/04/2023	Name: S WOOTTON		Drg No: 10P64355	Sht: 2
Date:	Chkd:			Next Sht: -

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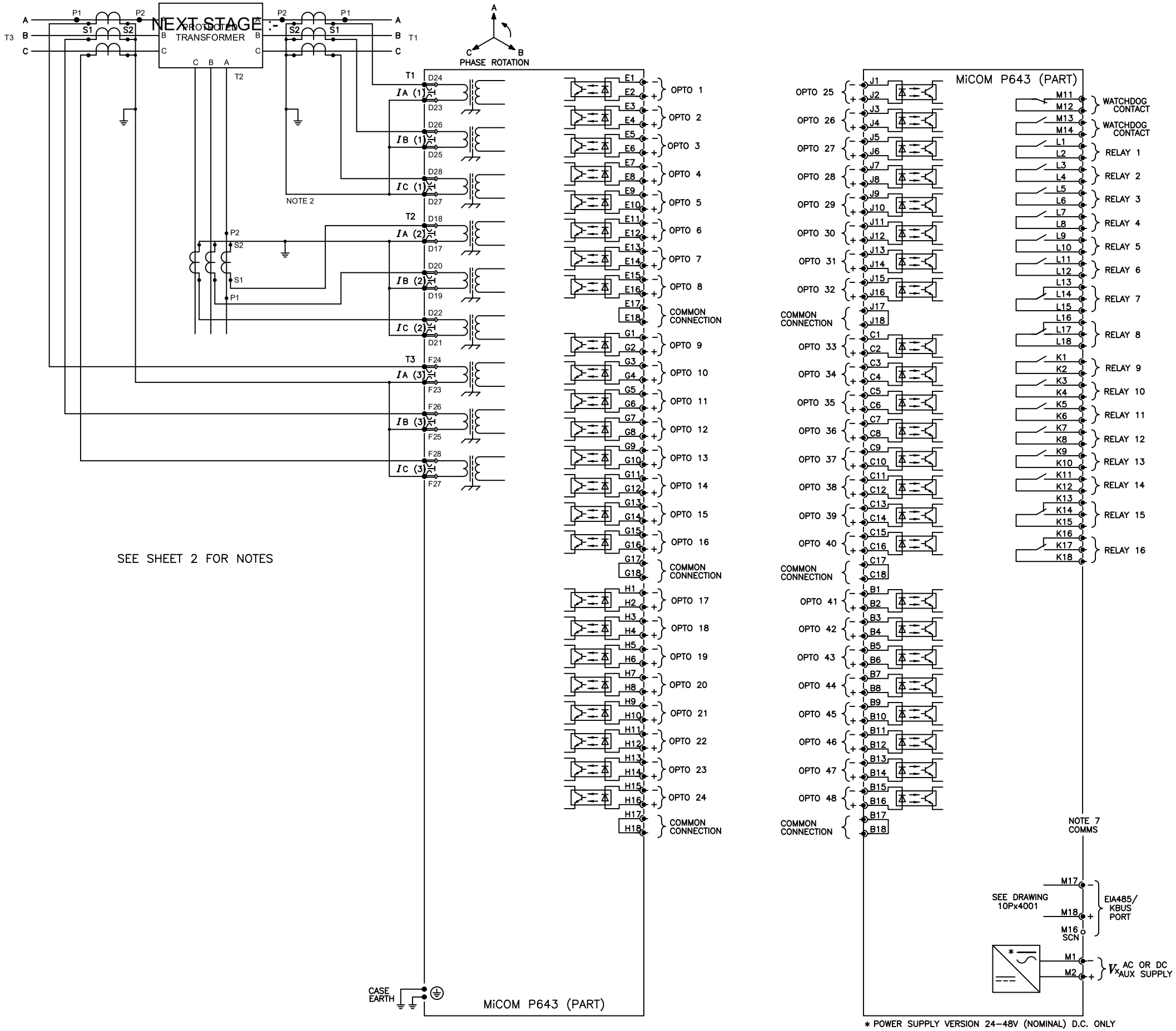
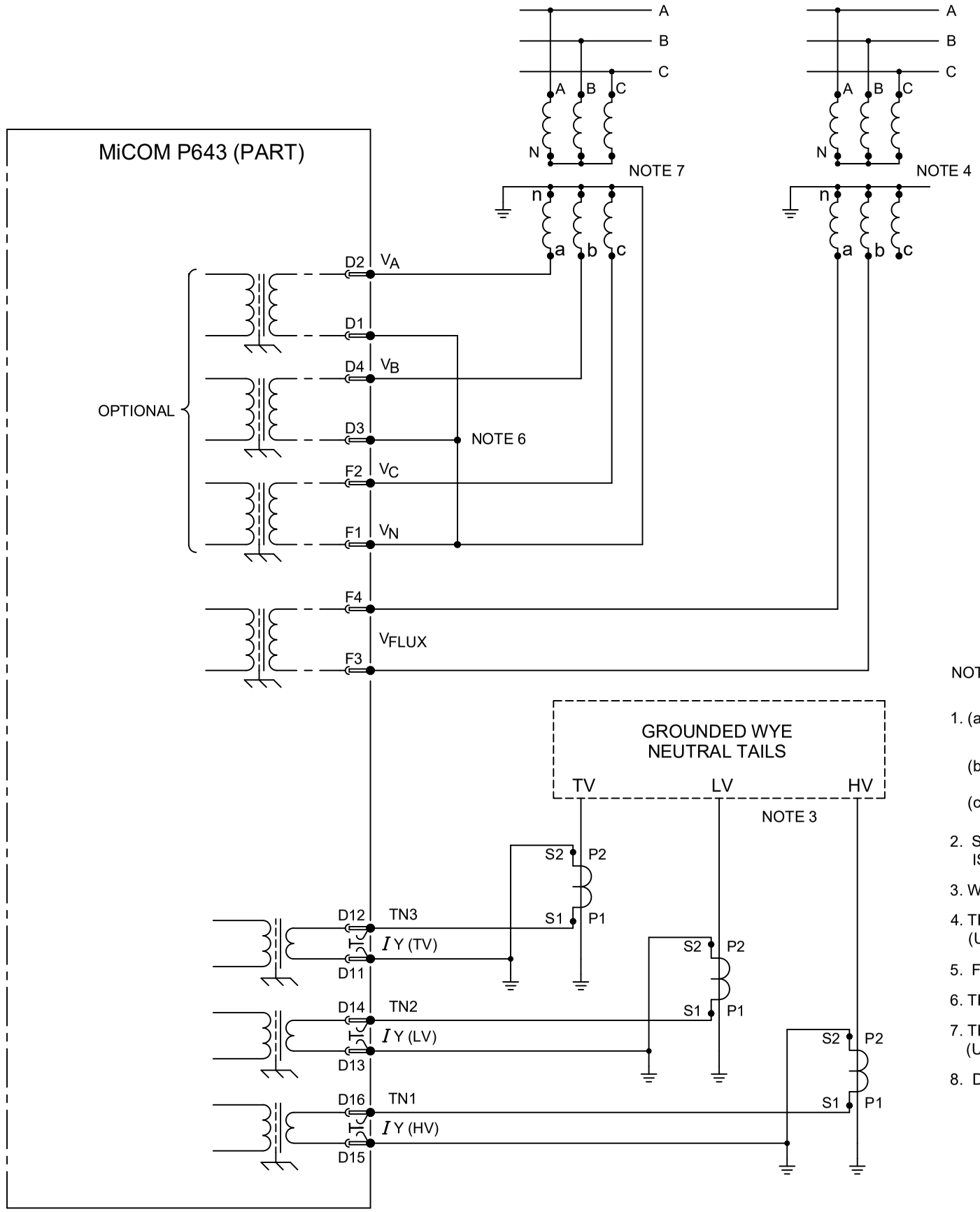
FINISH :-

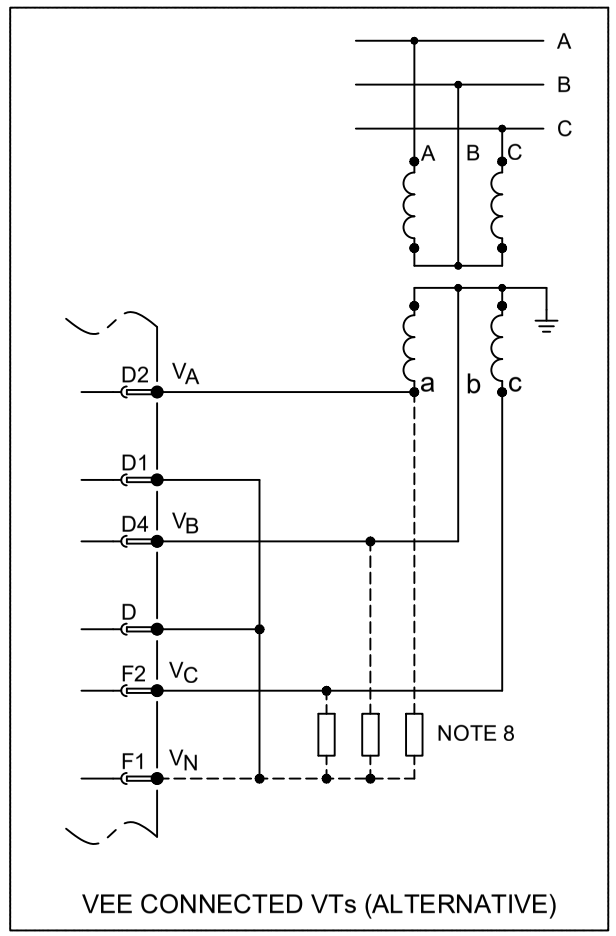
NEXT STAGE :-



SEE SHEET 2 FOR NOTES

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (48I/16O) 80TE		
Date: 16/03/2023	Name: S WOOTTON		Drg No: 10P64356	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 3 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (48I/16O) 80TE	
Date: 24/04/2023	Name: S WOOTTON		Drg No: 10P64356	Sht: 2
Date:	Chkd:			Next Sht: -

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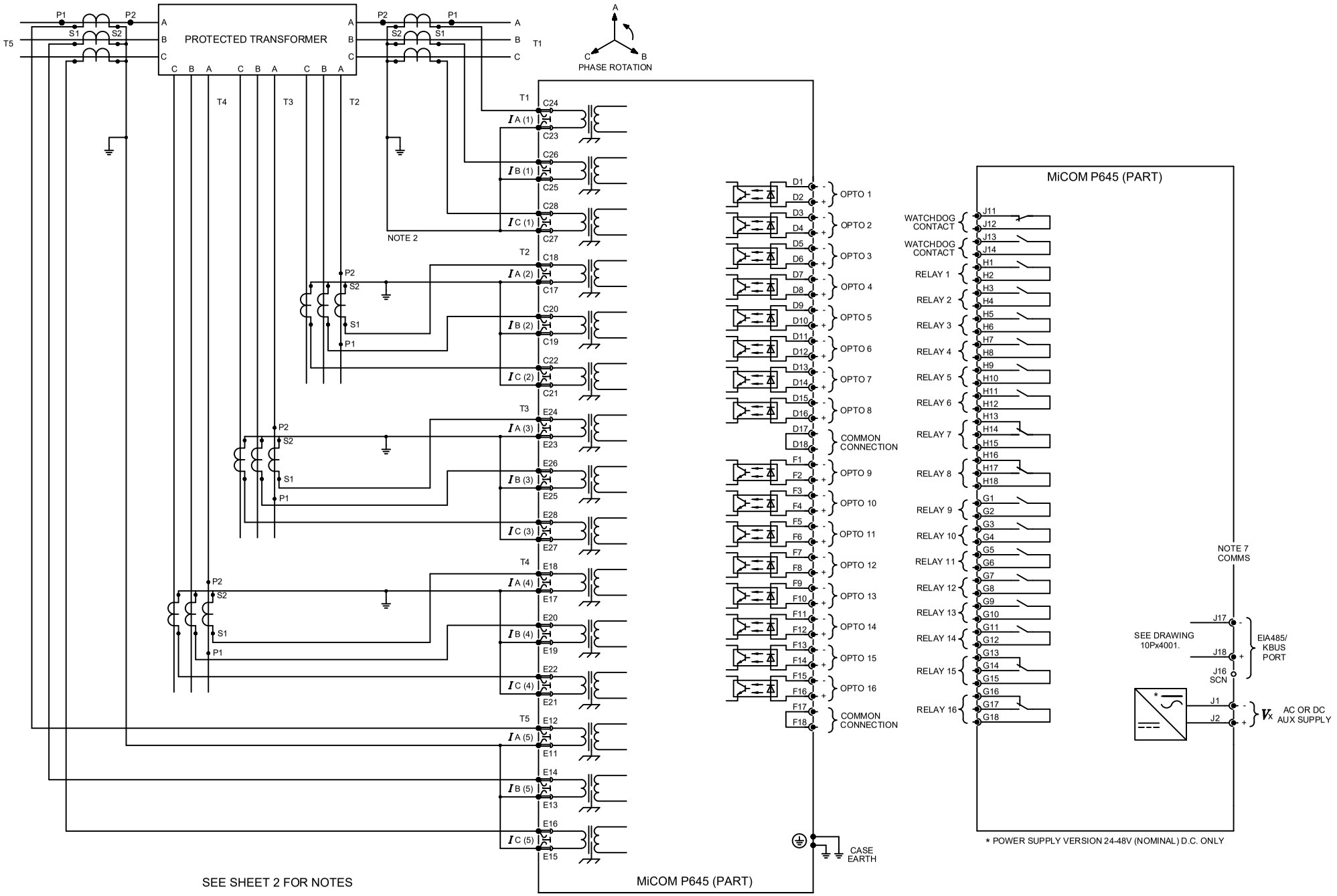
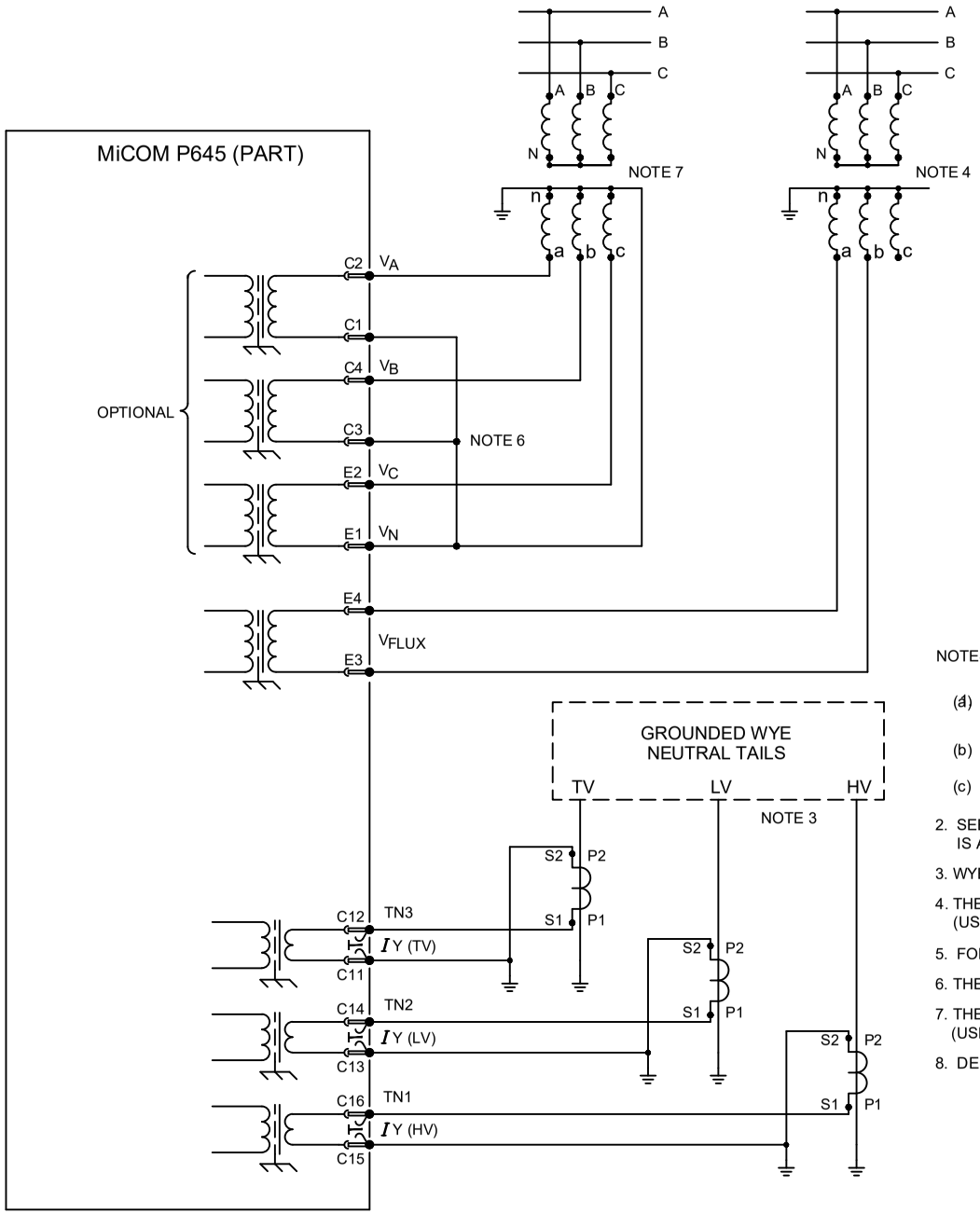
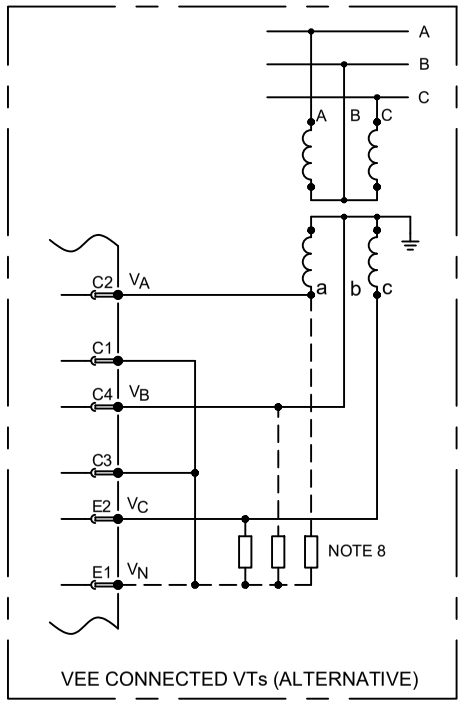


Issue: F	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64501	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

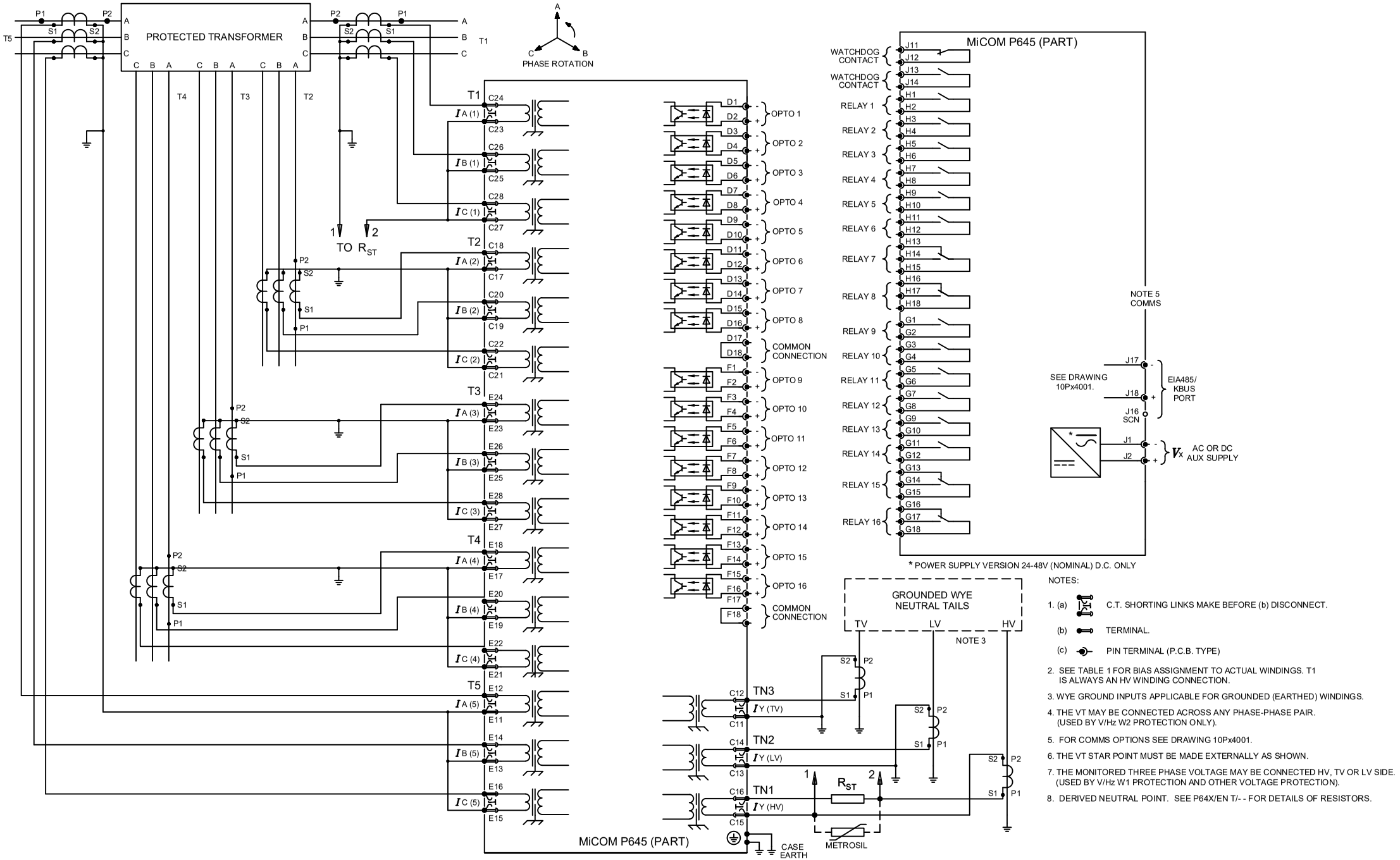
(a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

(b) TERMINAL.

(c) PIN TERMINAL (P.C.B. TYPE)

2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: K	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64501	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: H	Revision: CID006234 Outlines updated to GE Format		Title: EXT CONN DIAG:HIGH Z REF FOR 5 BIAS I/P TRANSFORMER DIFF. SAME PRINCIPAL APPLIES TO WIRE HIGH Z REF FOR T2,T3,T4,T5	
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64501	Sht: 3
Date:	Chkd:			Next Sht: -

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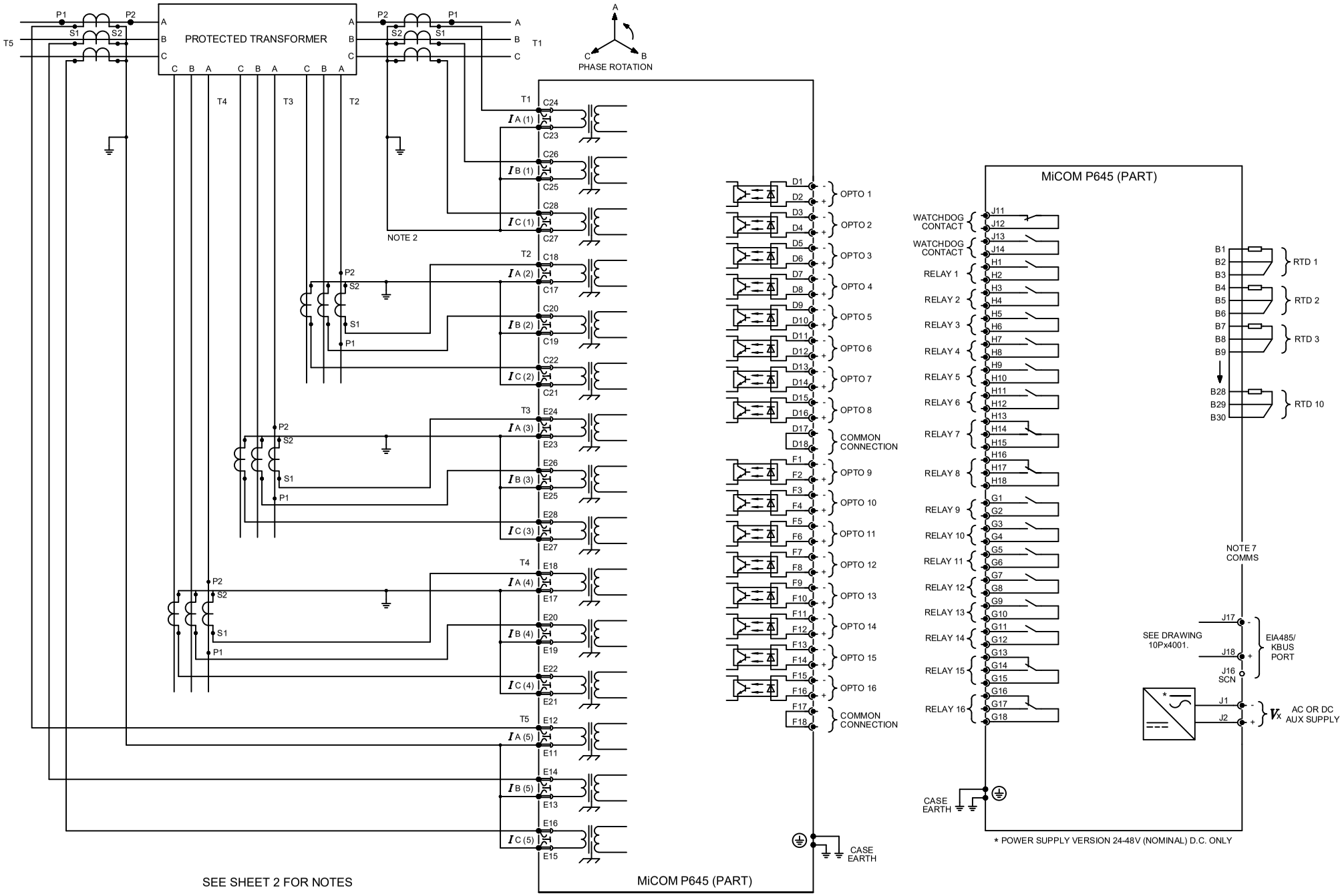
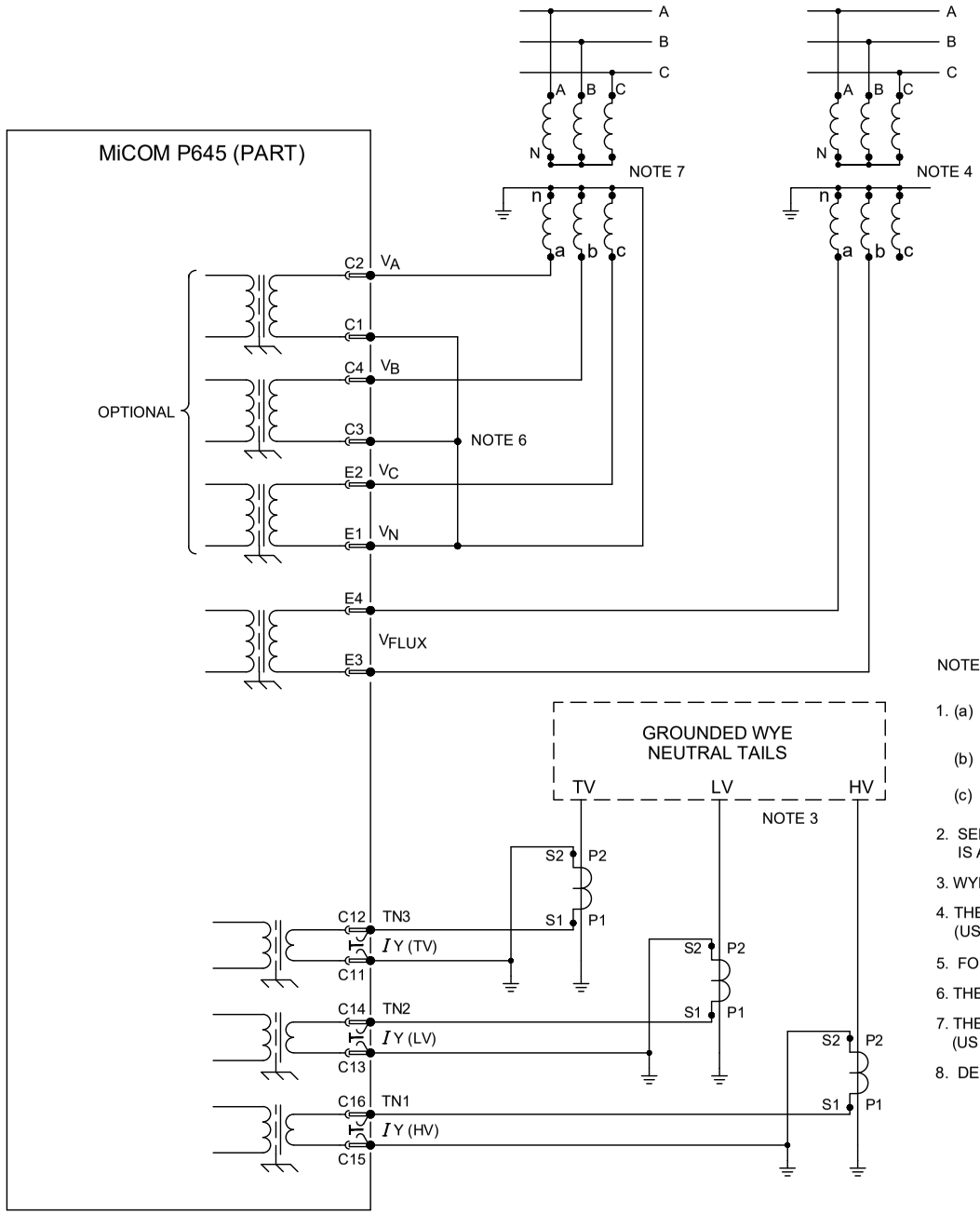
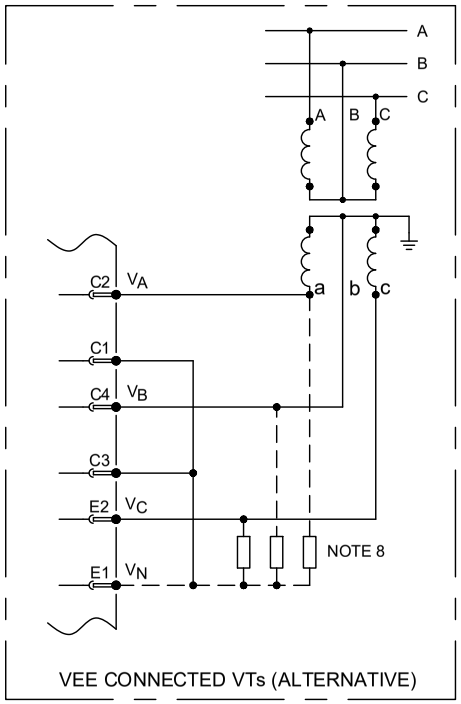


Issue: F	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P + RTD) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64502	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

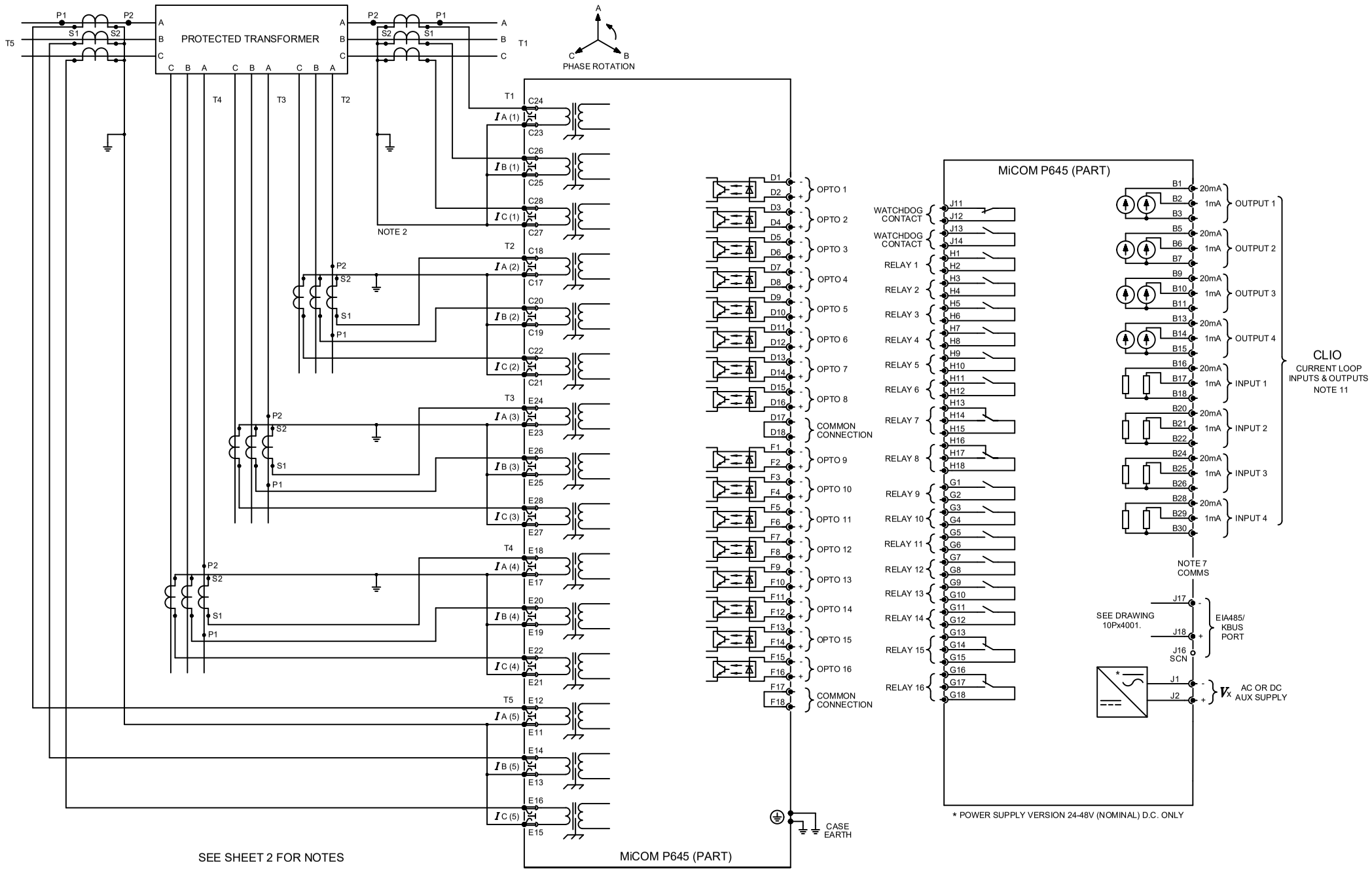




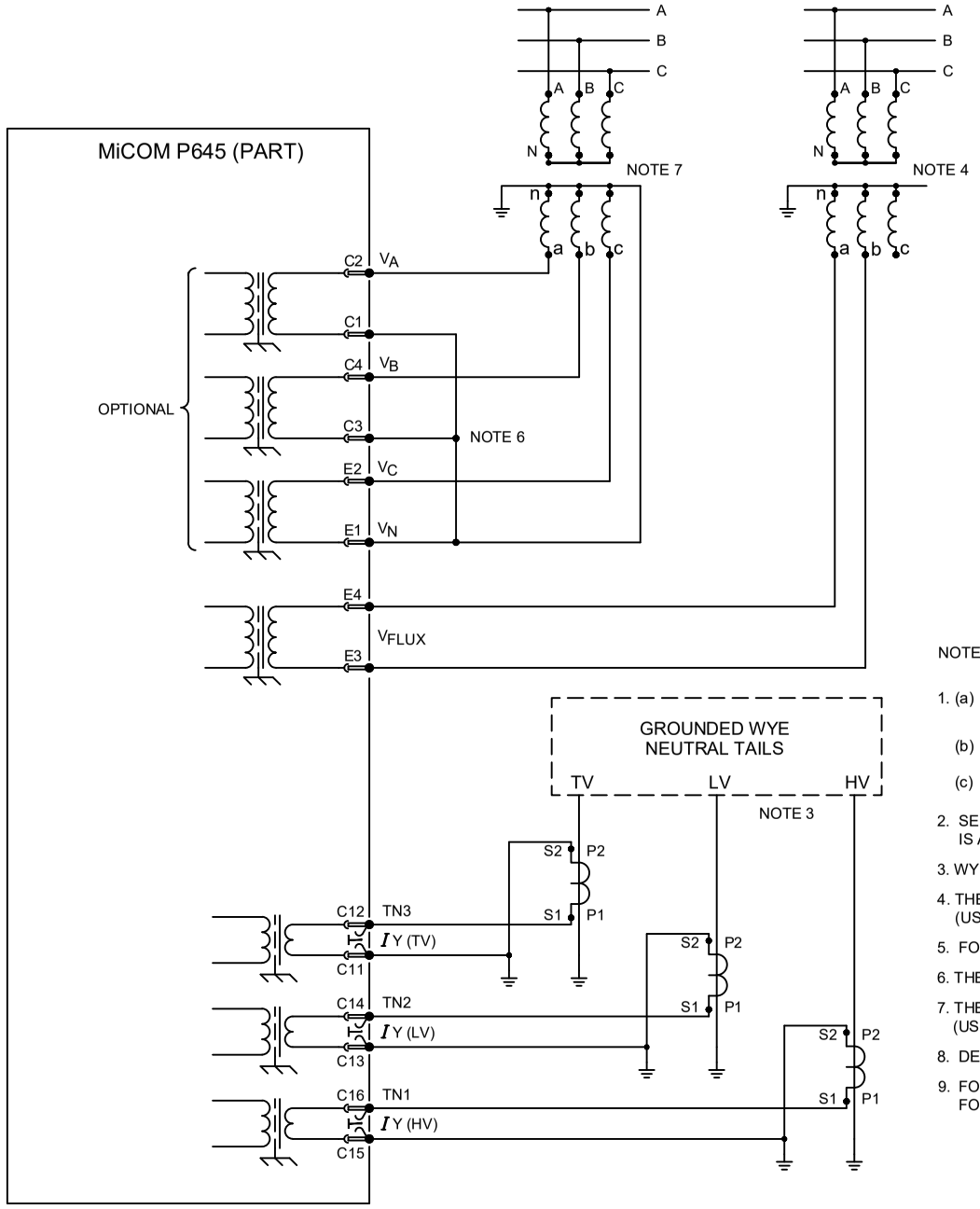
NOTES:

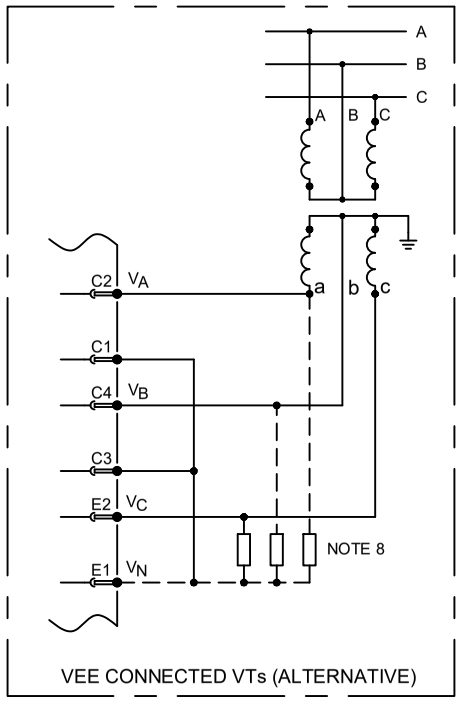
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P + RTD) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64502	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: F	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P + CLIO) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64503	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

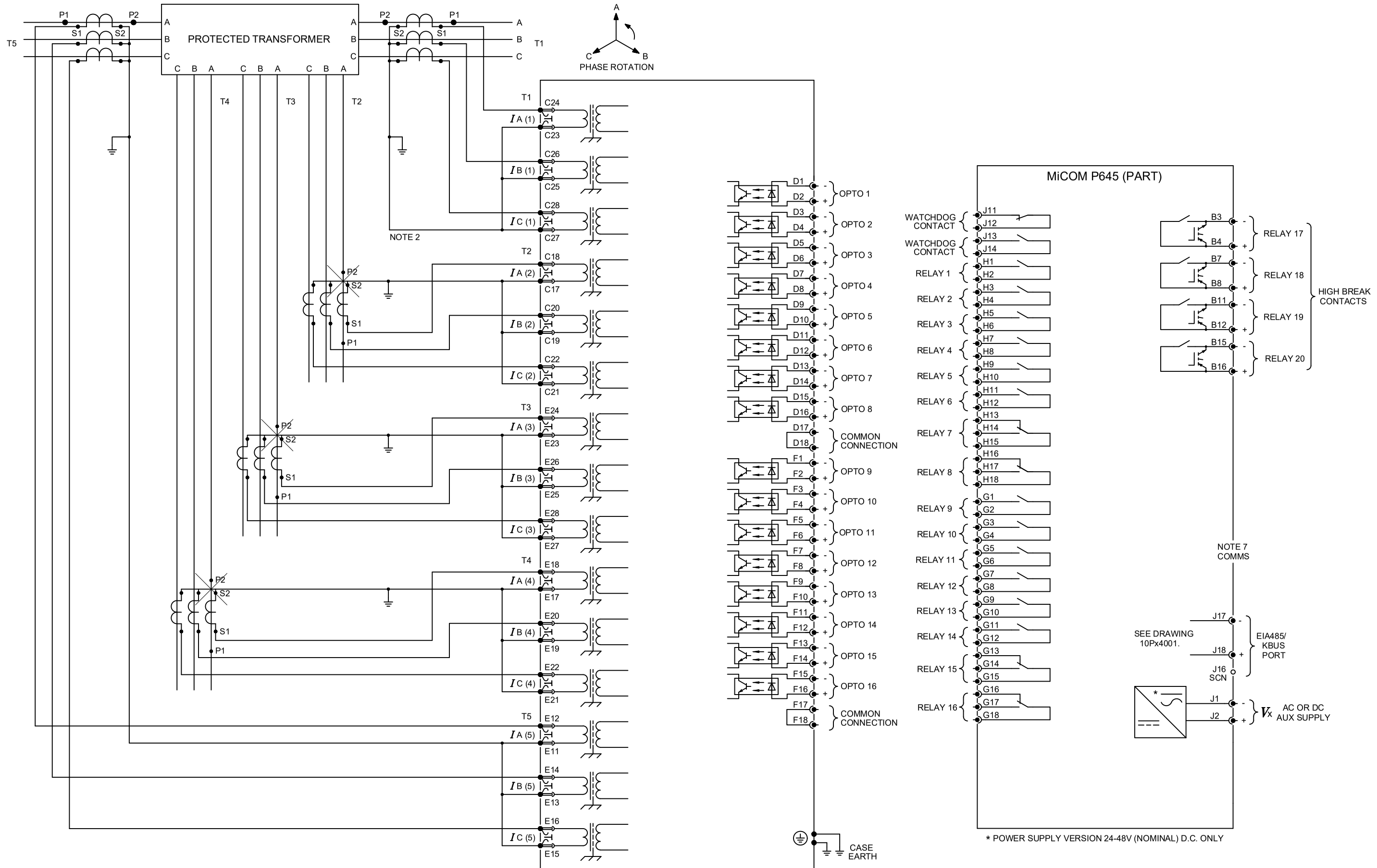




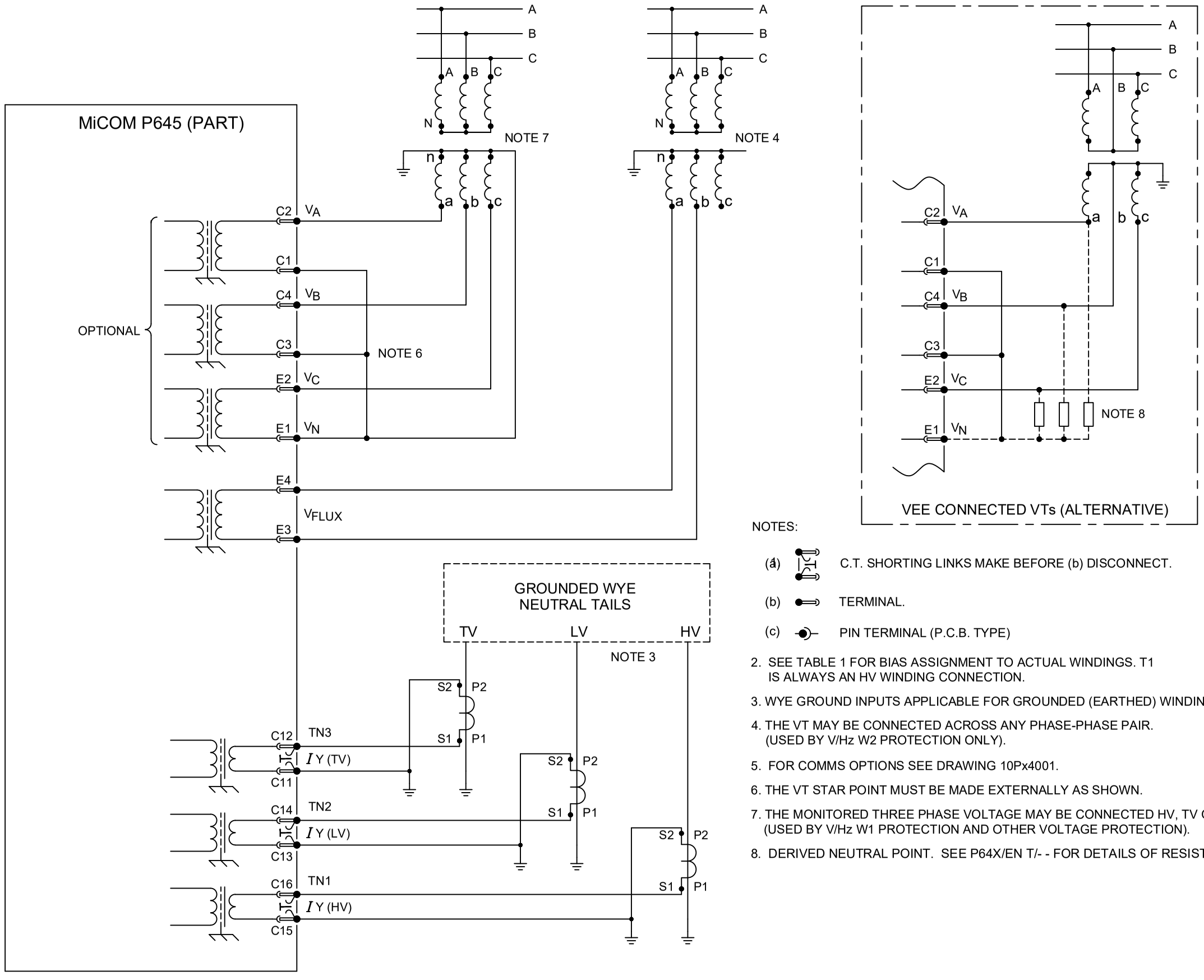
NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 16 O/P + CLIO) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64503	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/16O + 4 HB RELAYS) 60TE	
Date: 07/09/2023	Name: S WOOTTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64528	Sht: 1 Next Sht: 2
Date:	Chkd:			GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.



NOTES:

(a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

(b) TERMINAL.

(c) PIN TERMINAL (P.C.B. TYPE)

2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/16O + 4 HB RELAYS) 60TE	
Date: 07/09/2023	Name: S WOOTTON		Drg No: 10P64528	Sht: 2
Date:	Chkd:			Next Sht: -

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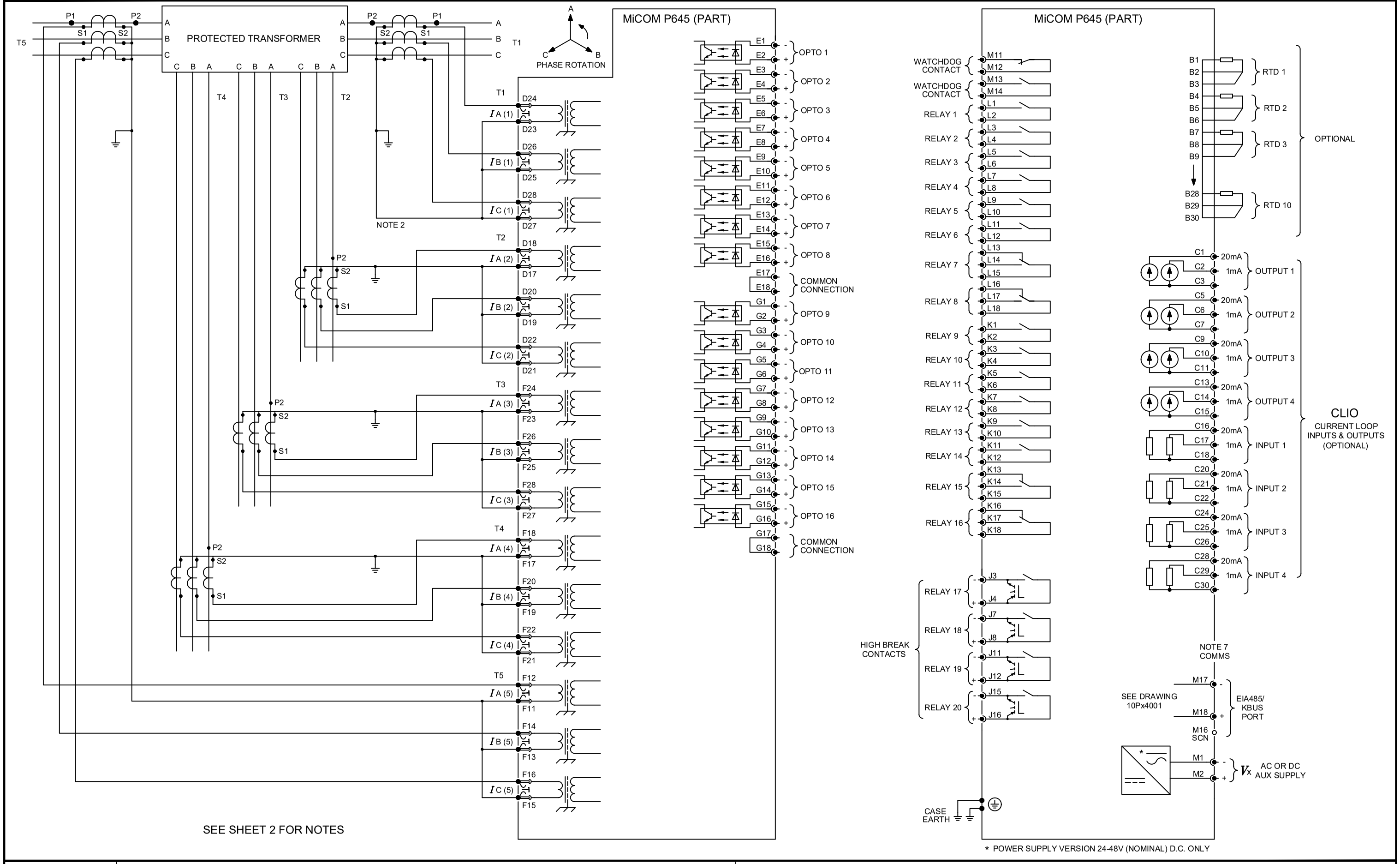
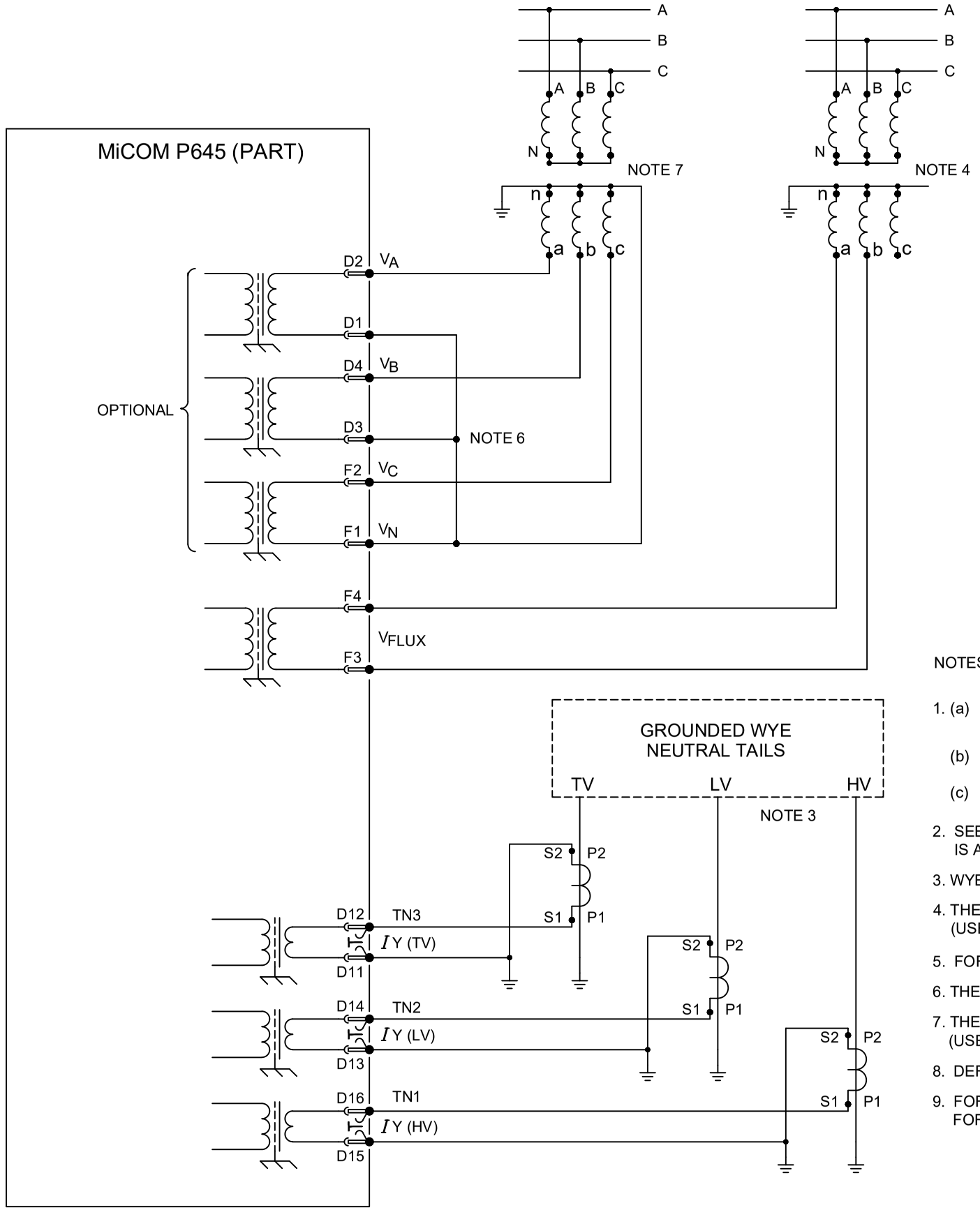
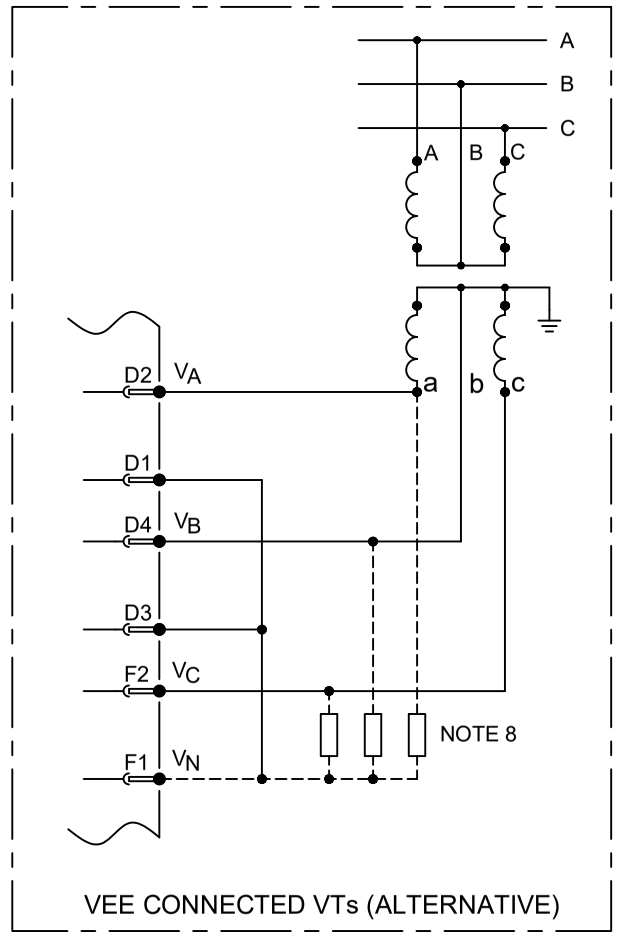


Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 19/09/2023	Name: S WOOTTON		Drg No: 10P64538	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF WITH 4 POLE VT INPUTS (16I/20O) 80TE	
Date: 18/09/2023	Name: S WOOTTON		Drg No: 10P64538	Sht: 2
Date:	Chkd:			Next Sht: -

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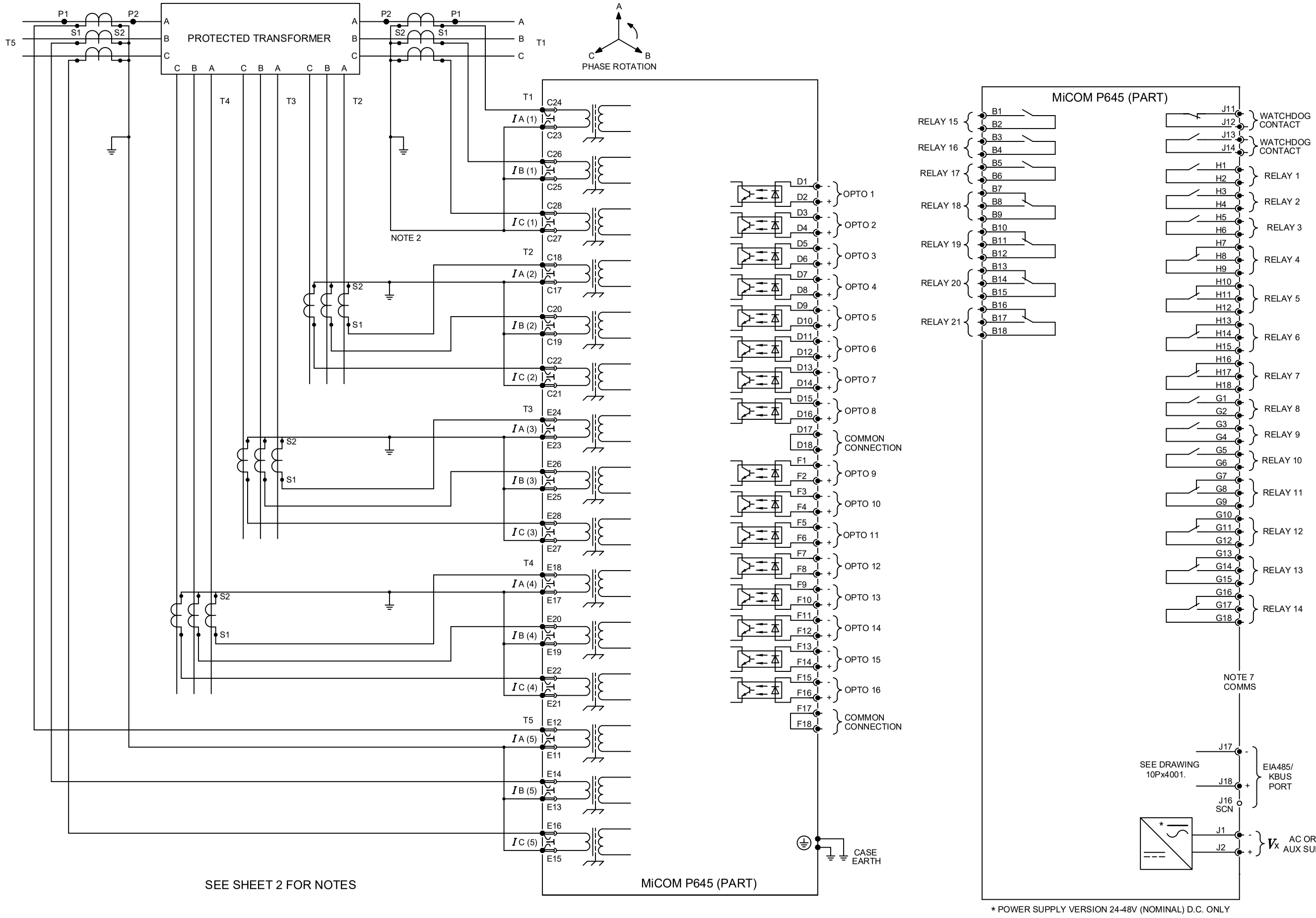
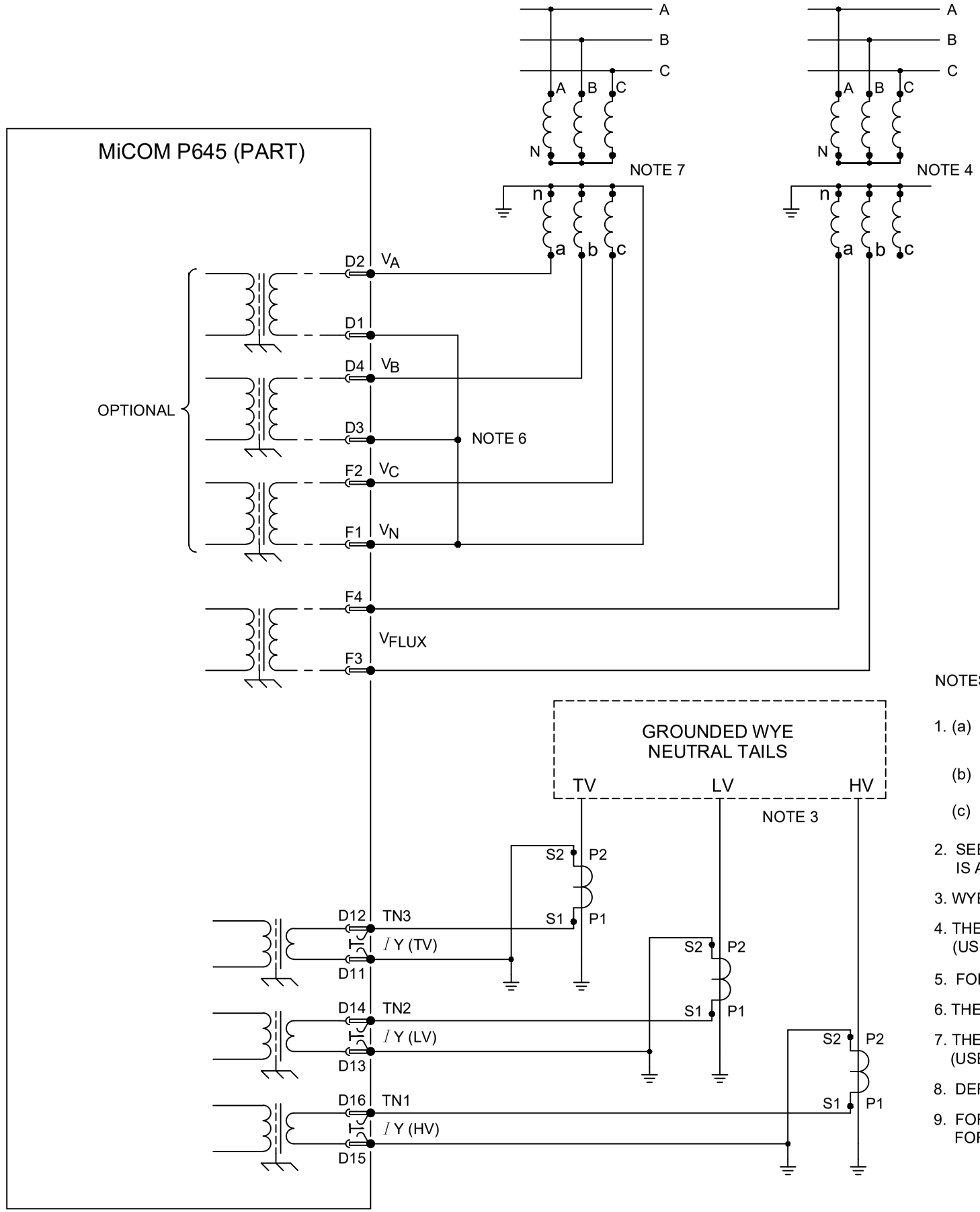
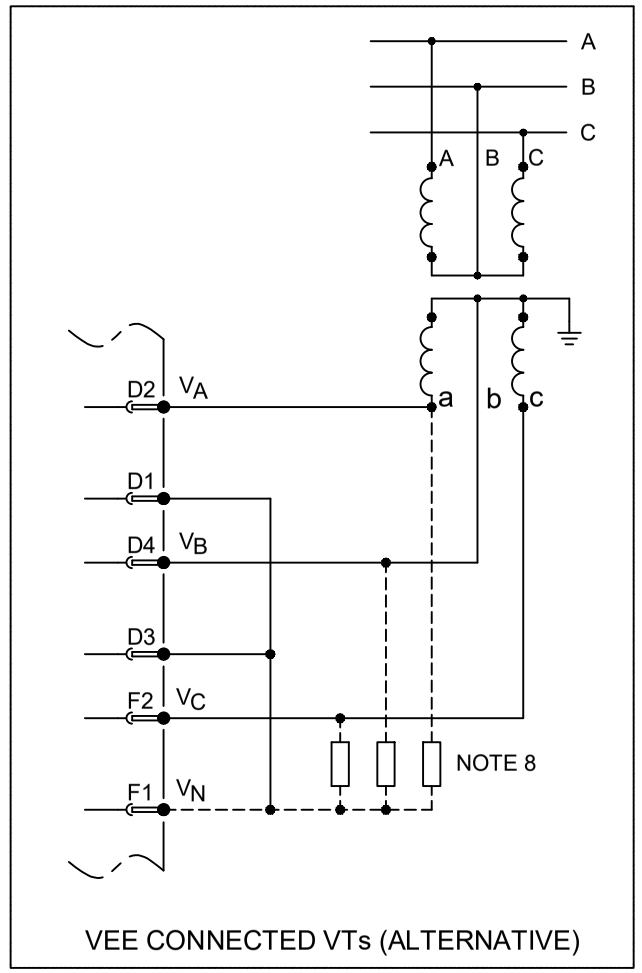


Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (16I/21O) 60TE	
Date: 07/09/2023	Name: S WOOTTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64529	Sht: 1 Next Sht: 2
Date:	Chkd:			GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (16I/16O) 60TE	
Date: 07/09/2023	Name: S WOOTTON		Drg No: 10P64529	Sht: 2
Date:	Chkd:			Next Sht: -

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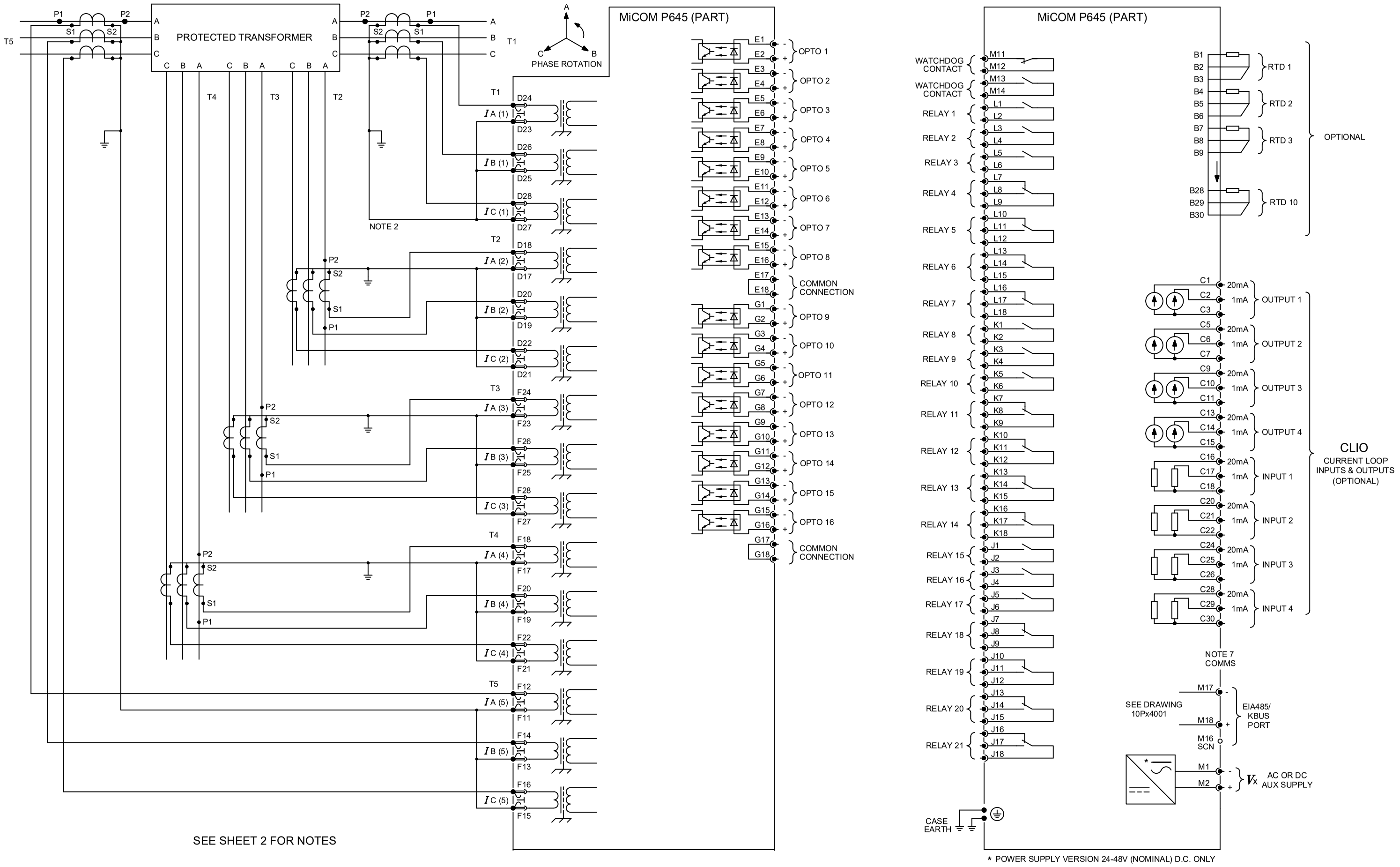
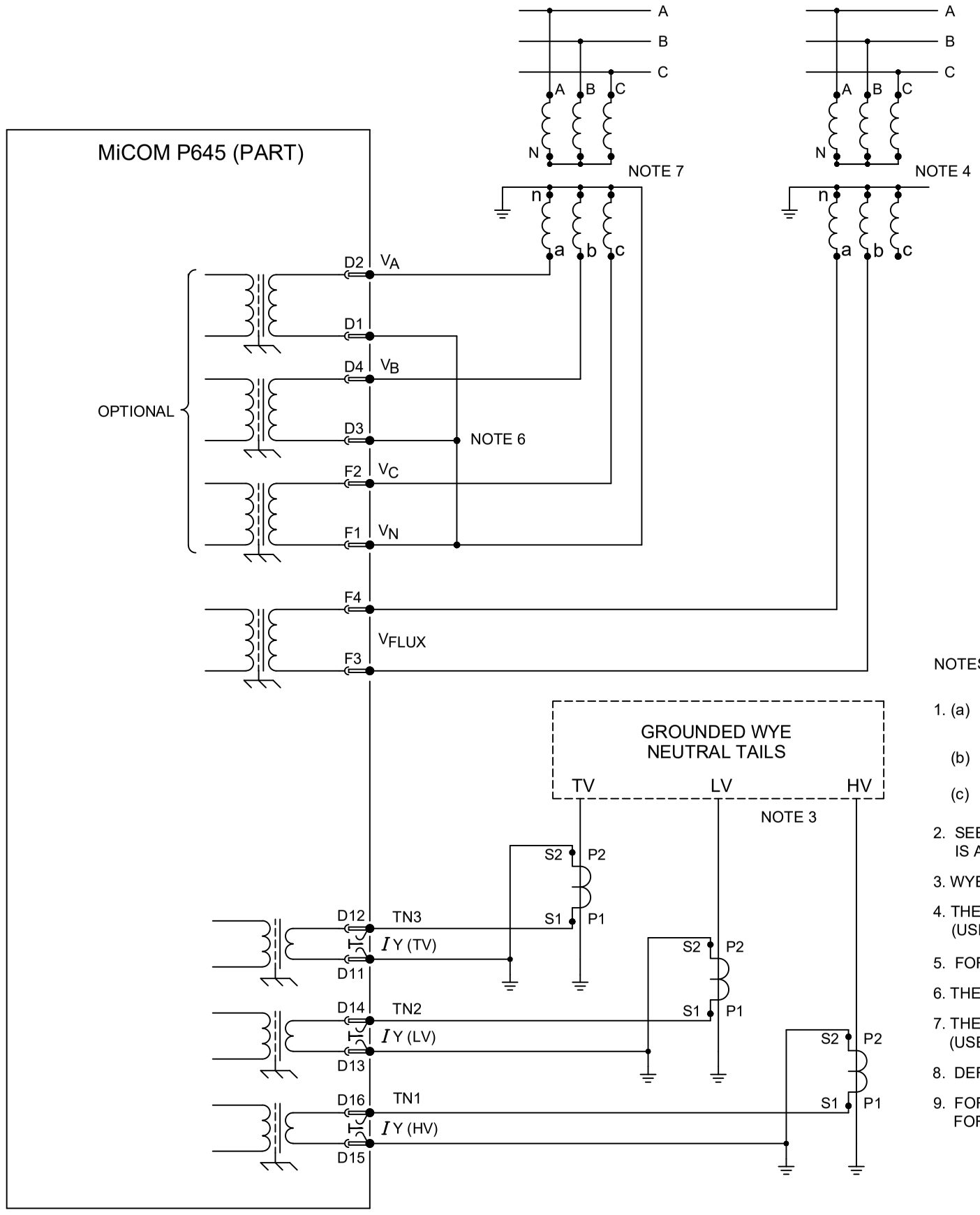
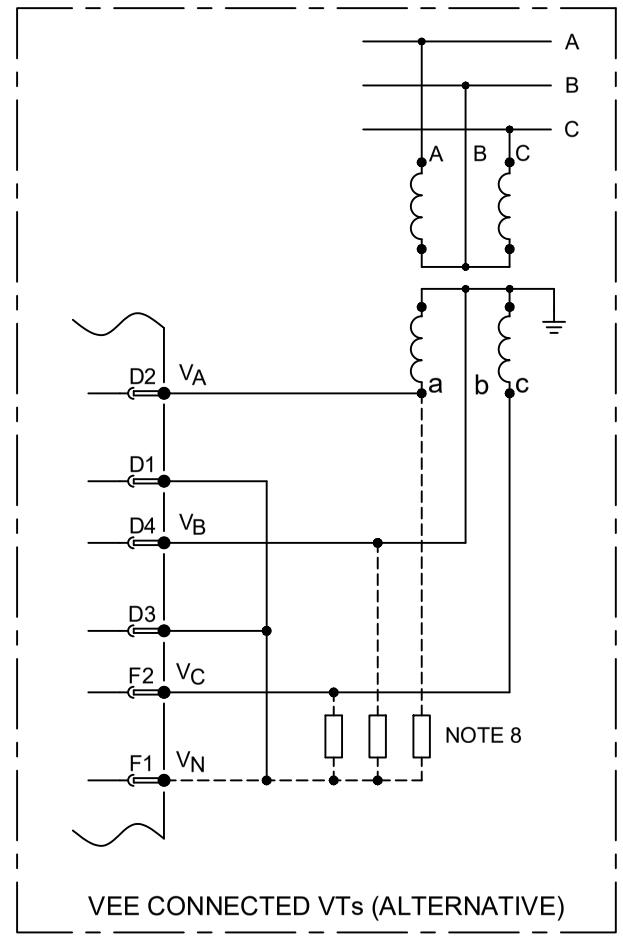


Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFERENTIAL. WITH 4 POLE VT INPUTS 80TE		
Date: 19/09/2023	Name: S WOOTTON		Drg No: 10P64542	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

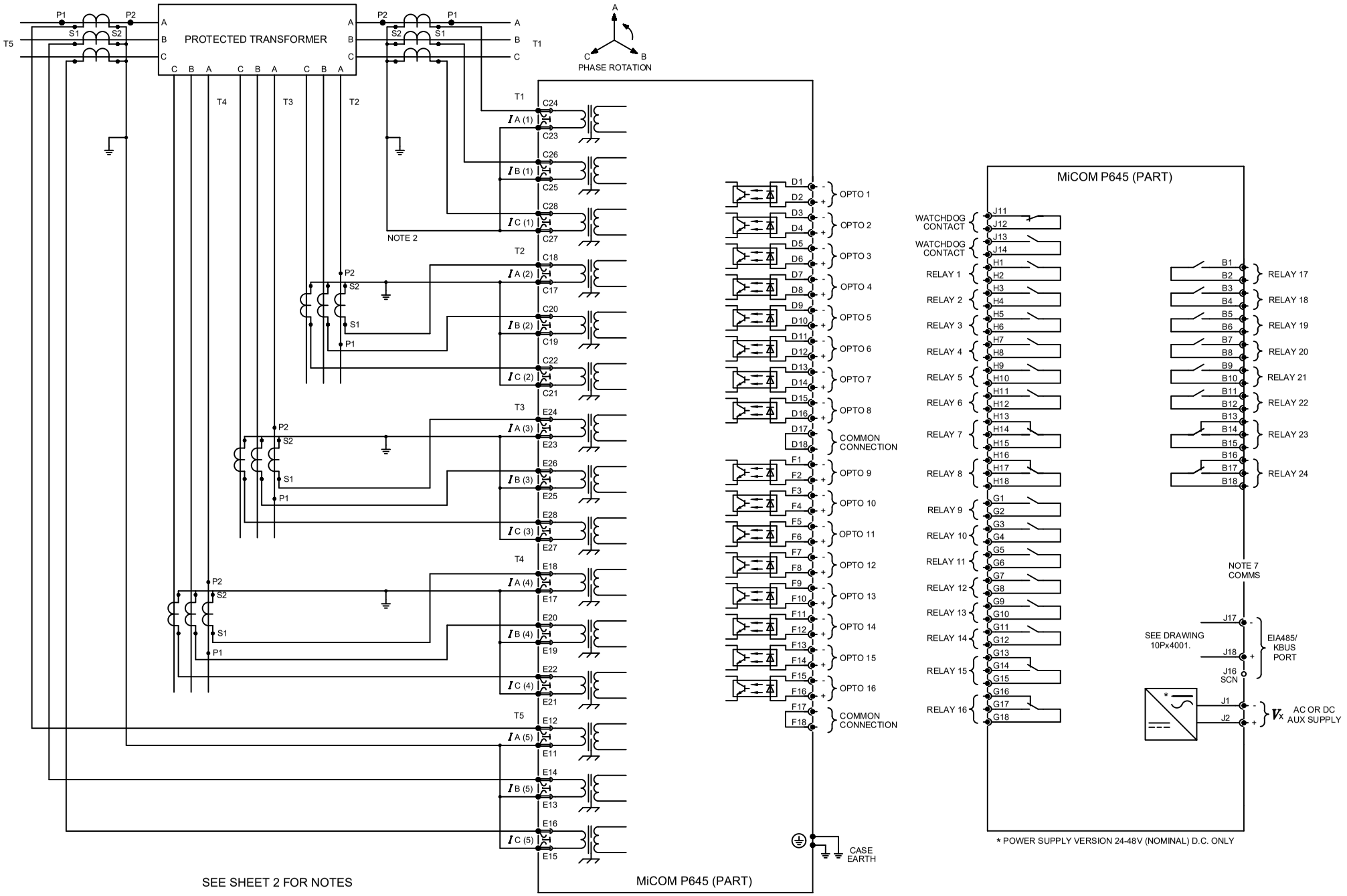




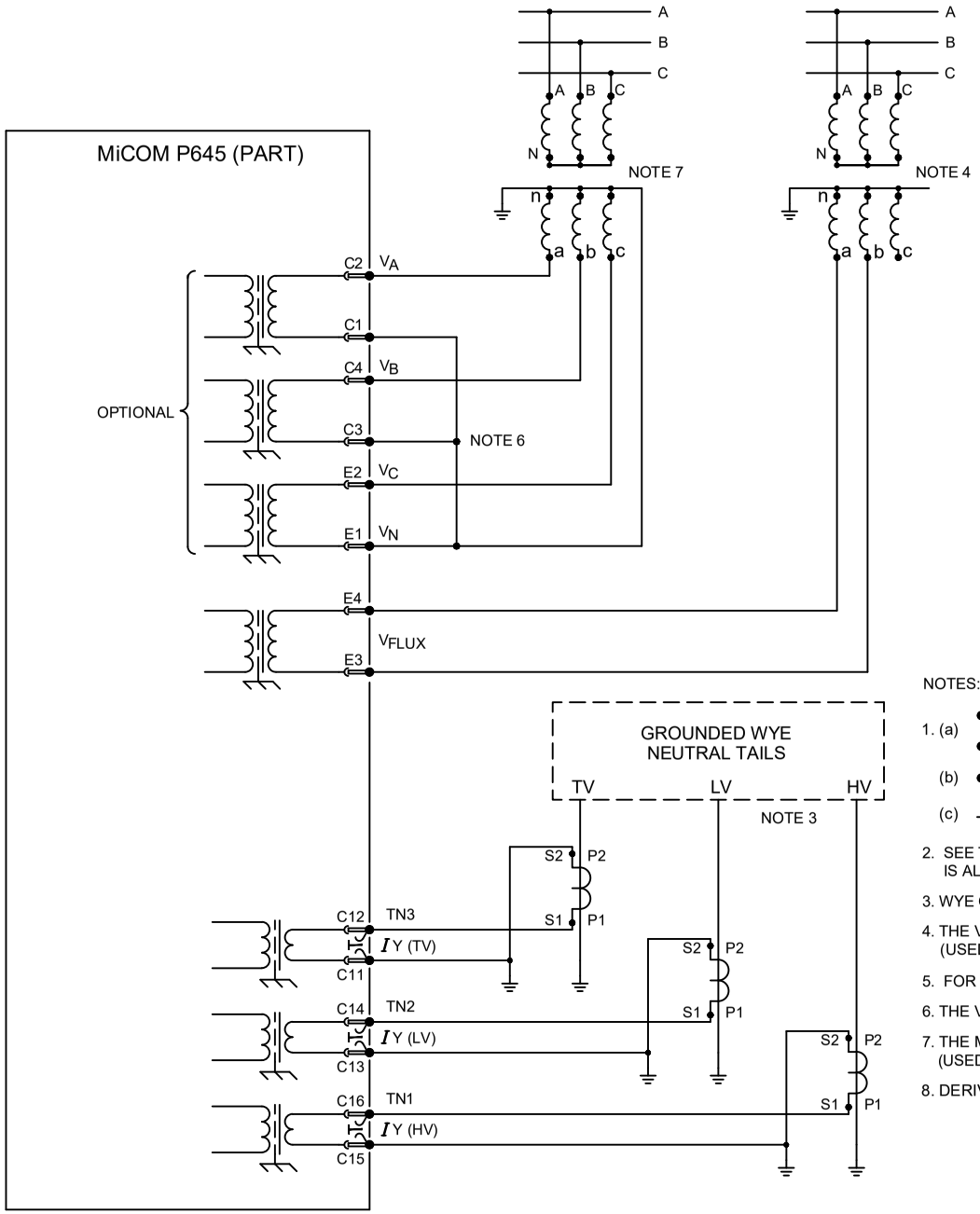
NOTES:

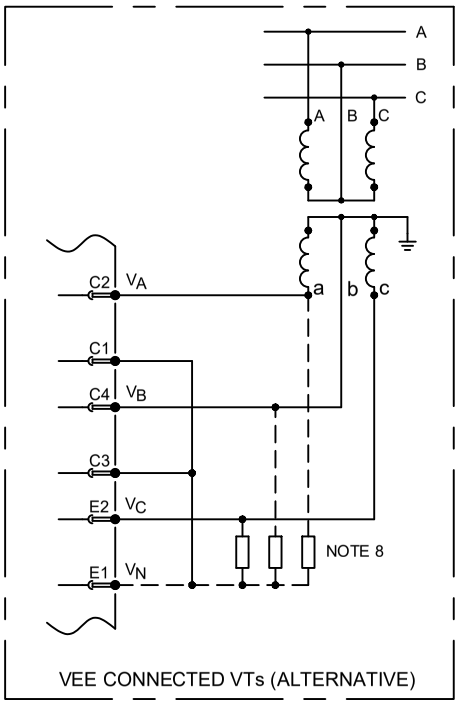
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/21O) 80TE		
Date: 19/09/2023	Name: S WOOTTON		Drg No: 10P64542	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: F	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 24 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64505	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

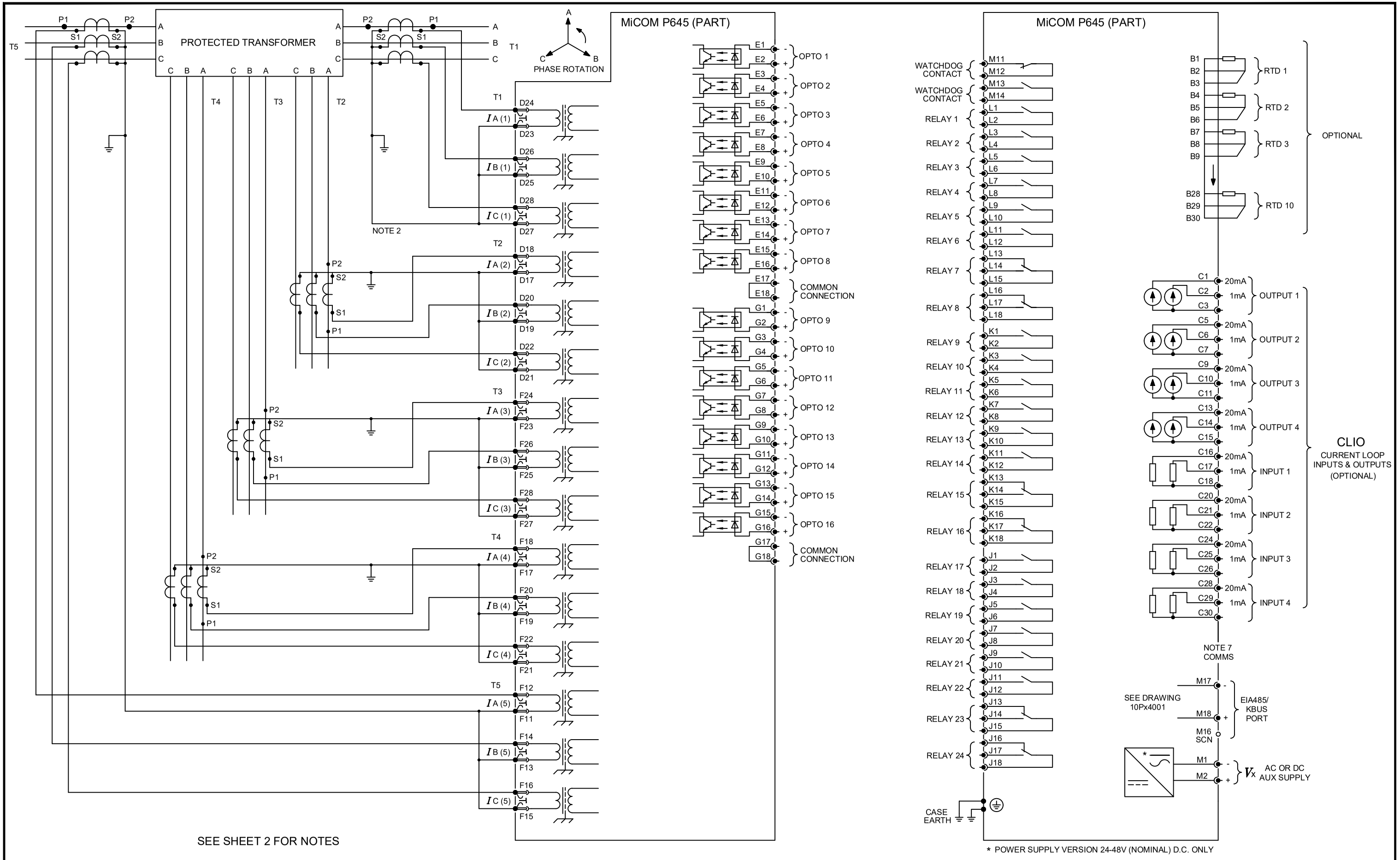




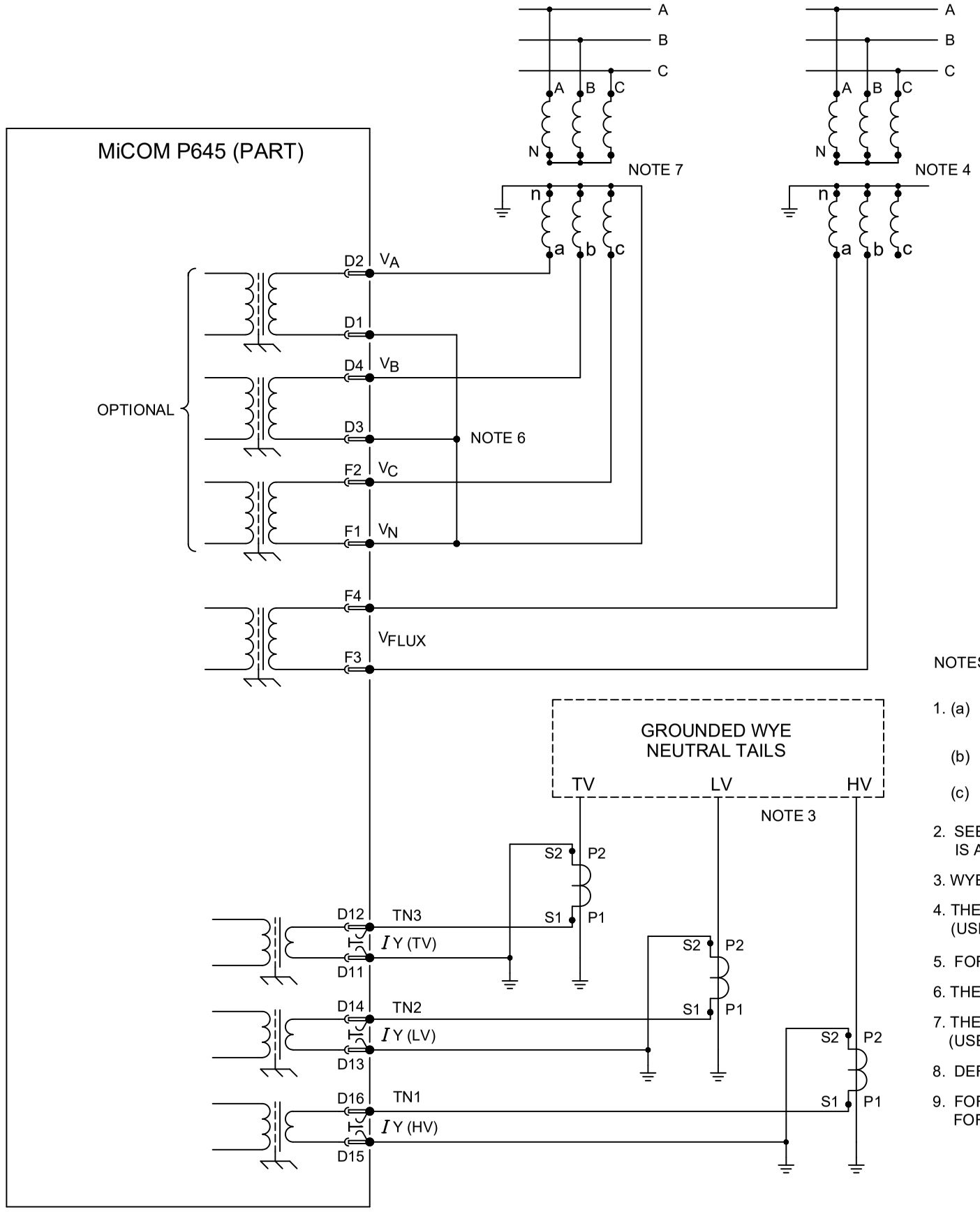
NOTES:

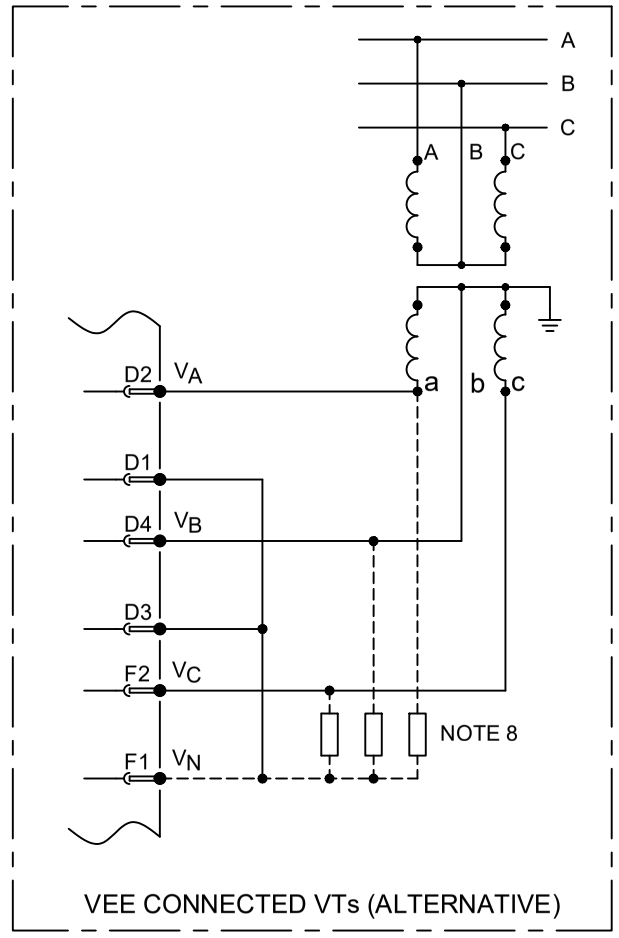
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS.T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (16 I/P & 24 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON	GE PROPRIETARY AND CONFIDENTIAL INFORMATION This document is the property of General Electric Company ("GE") and contains proprietary information of GE. This document is loaned on the express condition that neither it nor the information contained therein shall be disclosed to others without the express written consent of GE, and that the information shall be used by the recipient only as approved expressly by GE. This document shall be returned to GE upon its request. This document may be subject to certain restrictions under U.S. export control laws and regulations.© General Electric Company, GE CONFIDENTIAL UNPUBLISHED WORK.	Drg No: 10P64505	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS 80TE		
Date: 19/09/2023	Name: S WOOTTON		Drg No: 10P64546	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (16I/24O) 80TE	
Date: 19/09/2023	Name: S WOOTTON		Drg No: 10P64546	Sht: 2
Date:	Chkd:			Next Sht: -

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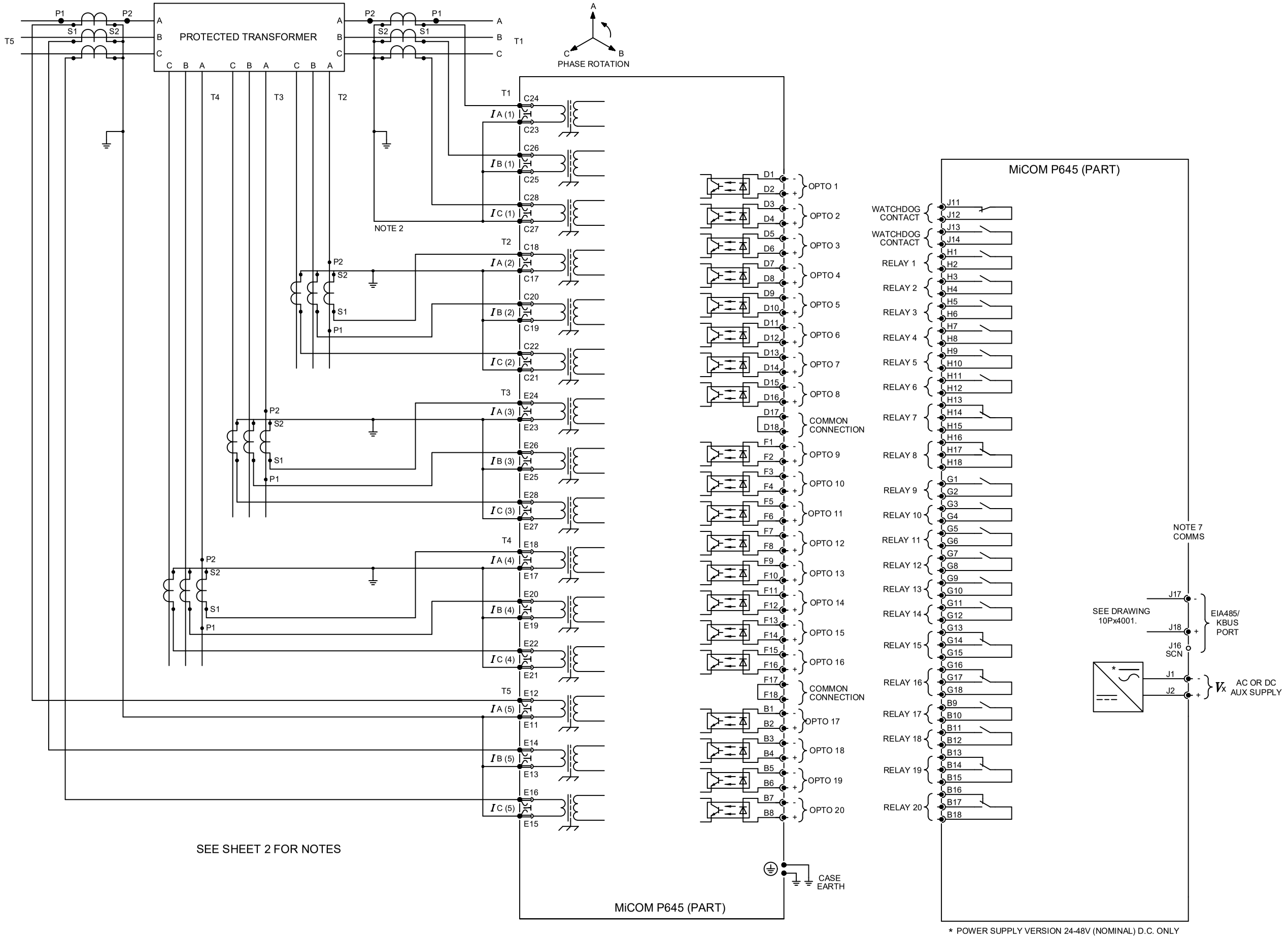

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (20I/20O) 60TE	
Date: 07/09/2023	Name: S WOOTTON		Drg No: **10P64530**	Sht: 1
Date:	Chkd:			Next Sht: 2

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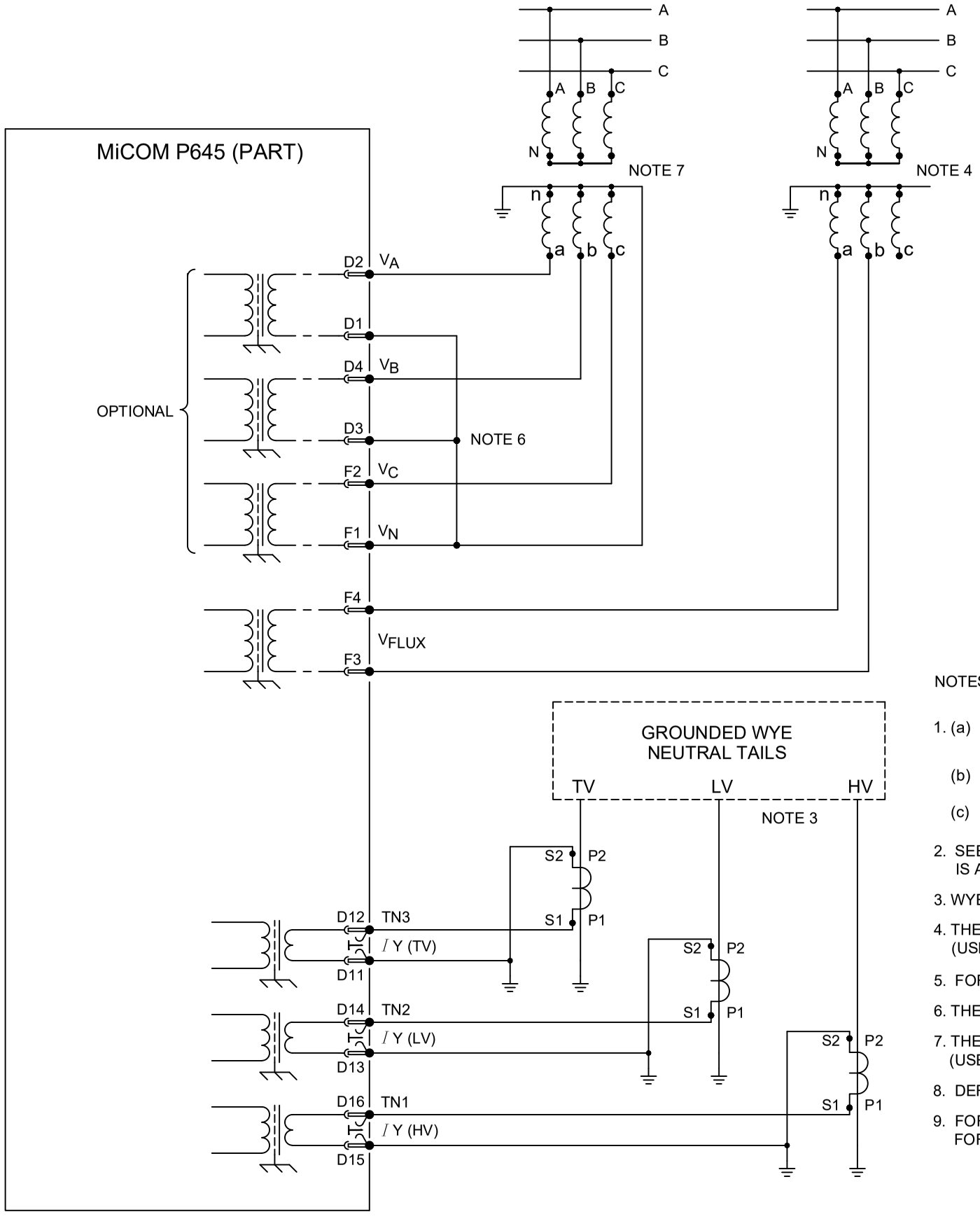
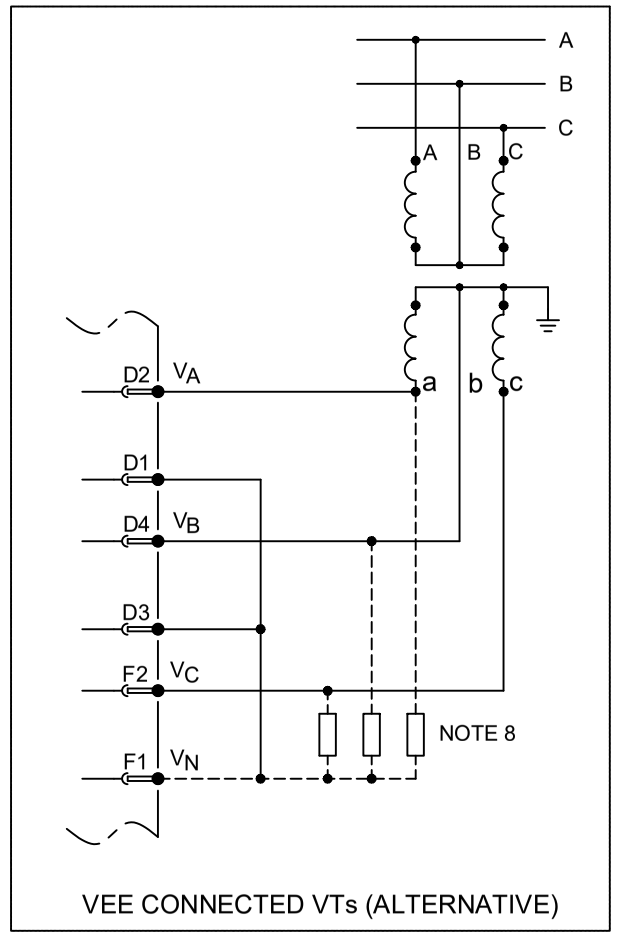
ST16 1WT, UK.





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (20I/20O) 60TE	
Date: 11/10/2023	Name: S WOOTTON		Drg No: 10P64530	Sht: 2
Date:	Chkd:			Next Sht: -

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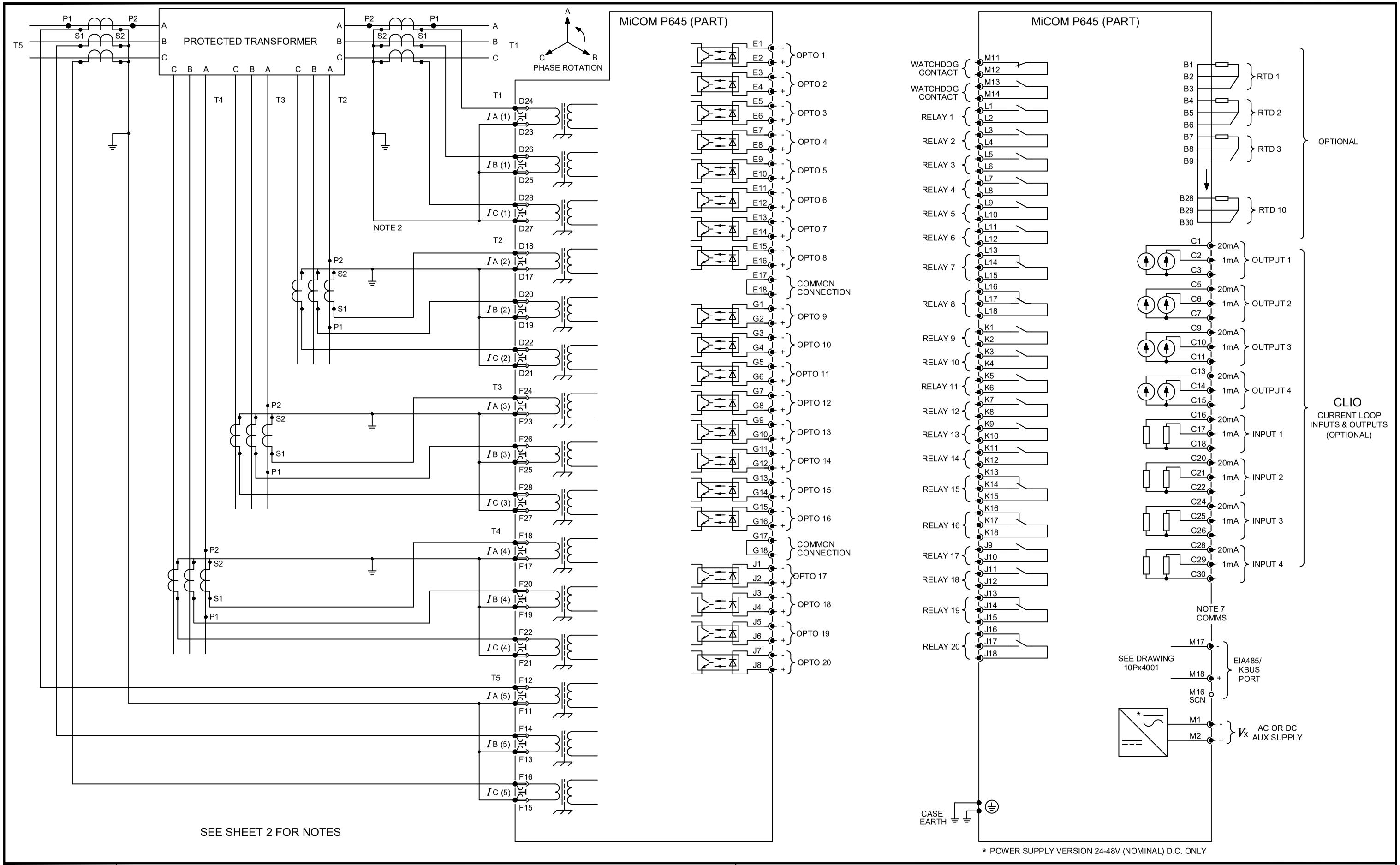
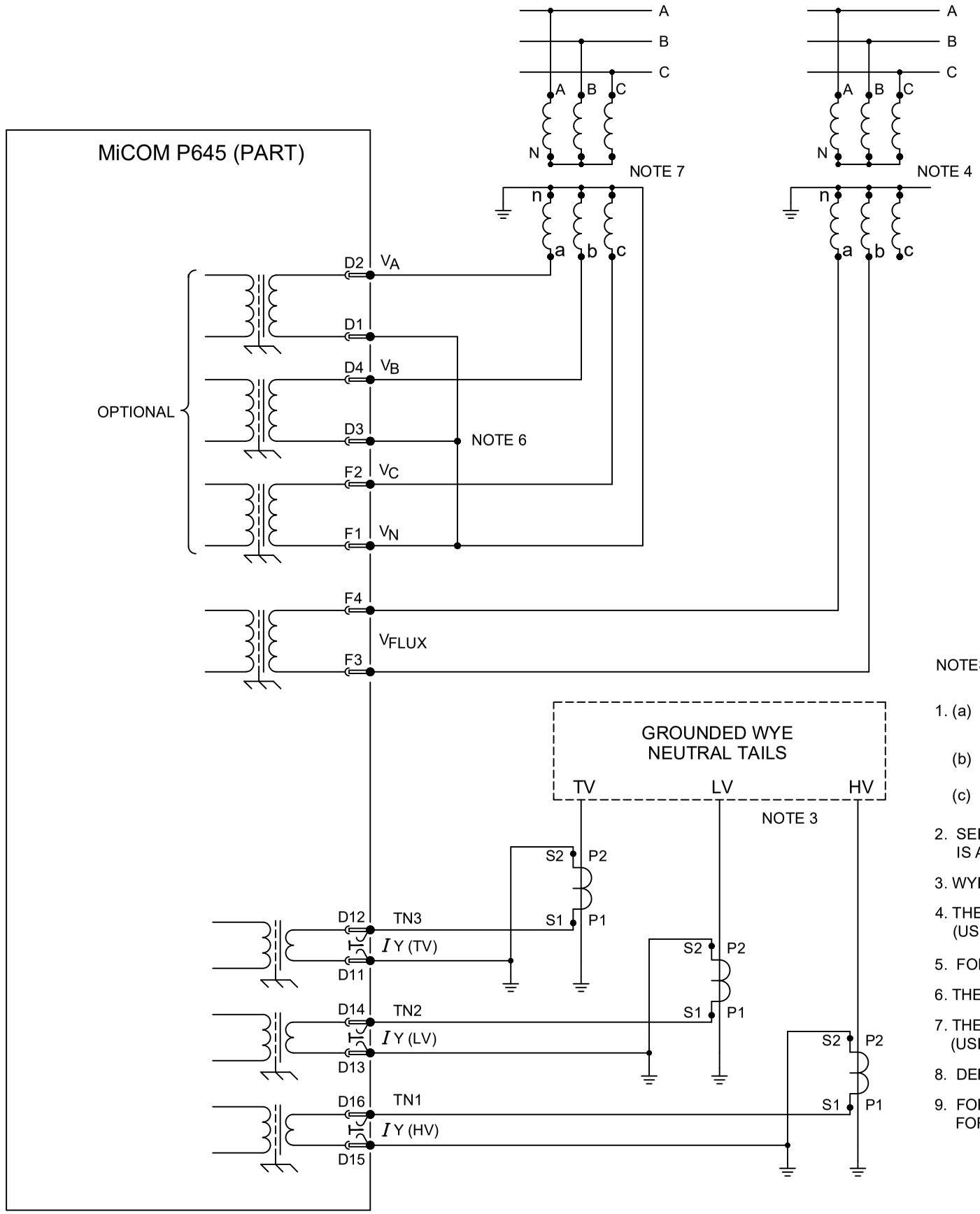
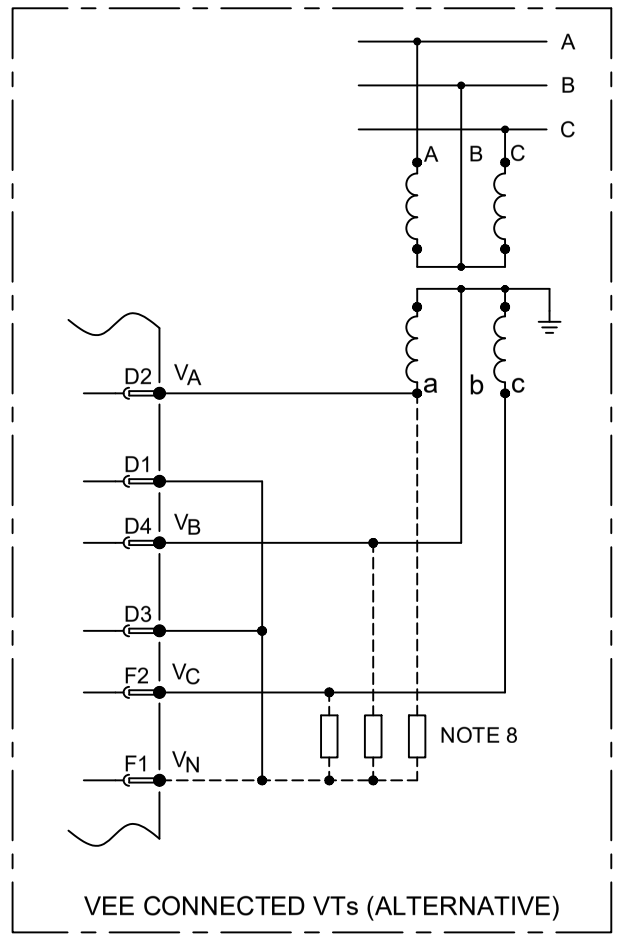


Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 20/09/2023	Name: S WOOTTON		Drg No: 10P64550	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

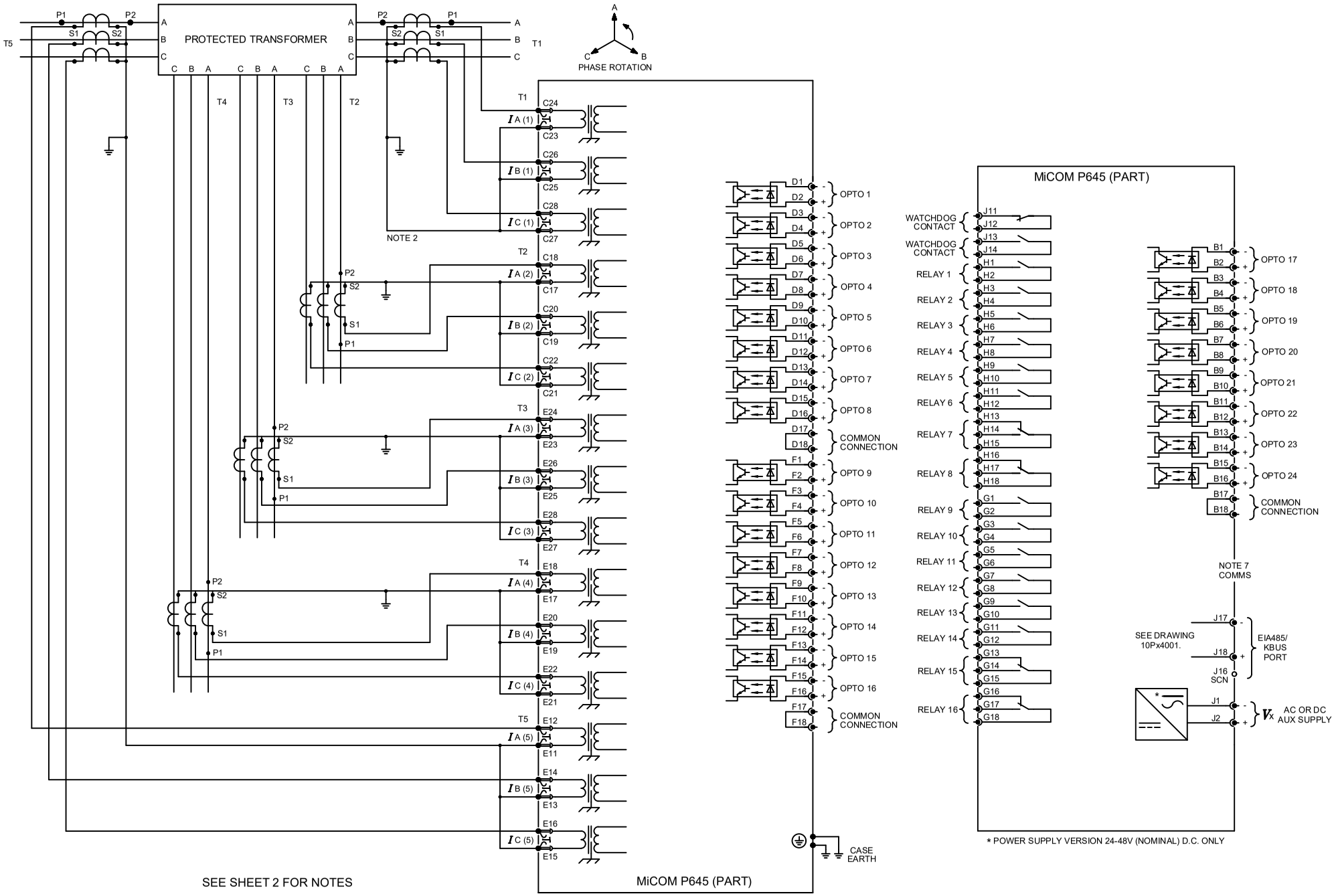




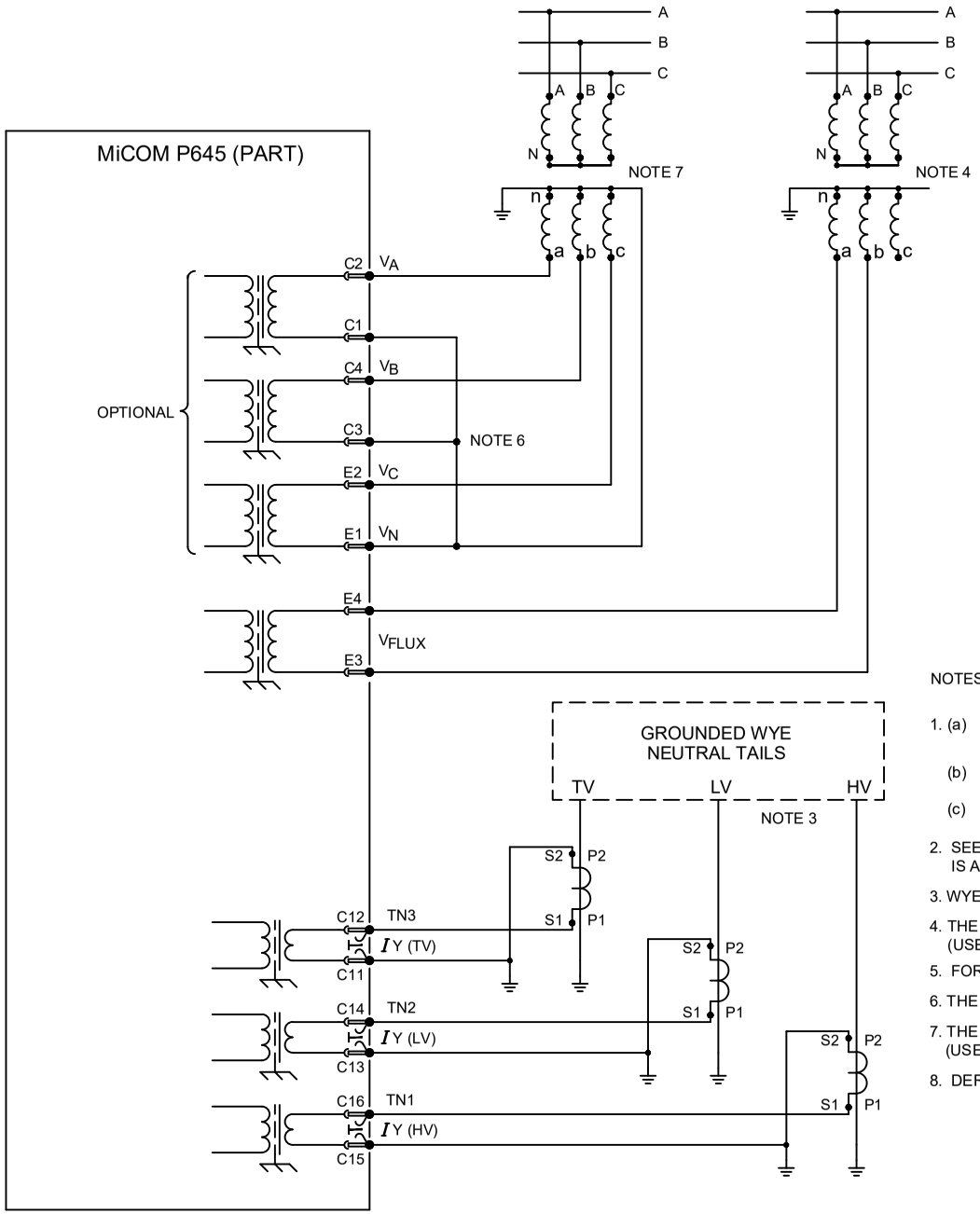
NOTES:

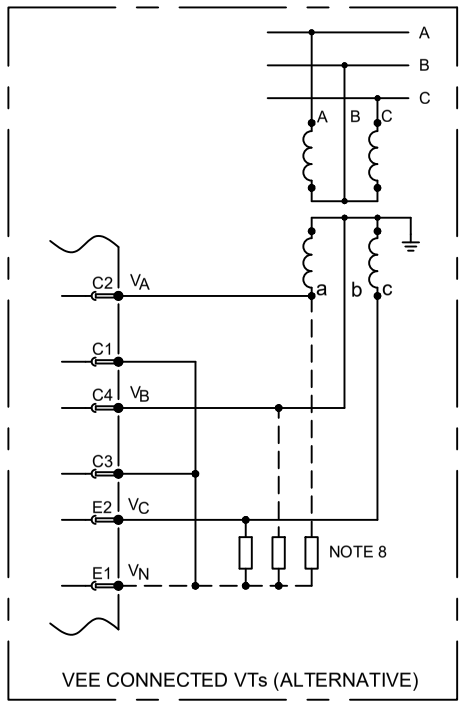
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (20I/20O) 80TE		
Date: 20/09/2023	Name: S WOOTTON		Drg No: 10P64550	Sht: 2	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: F	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/P & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64504	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

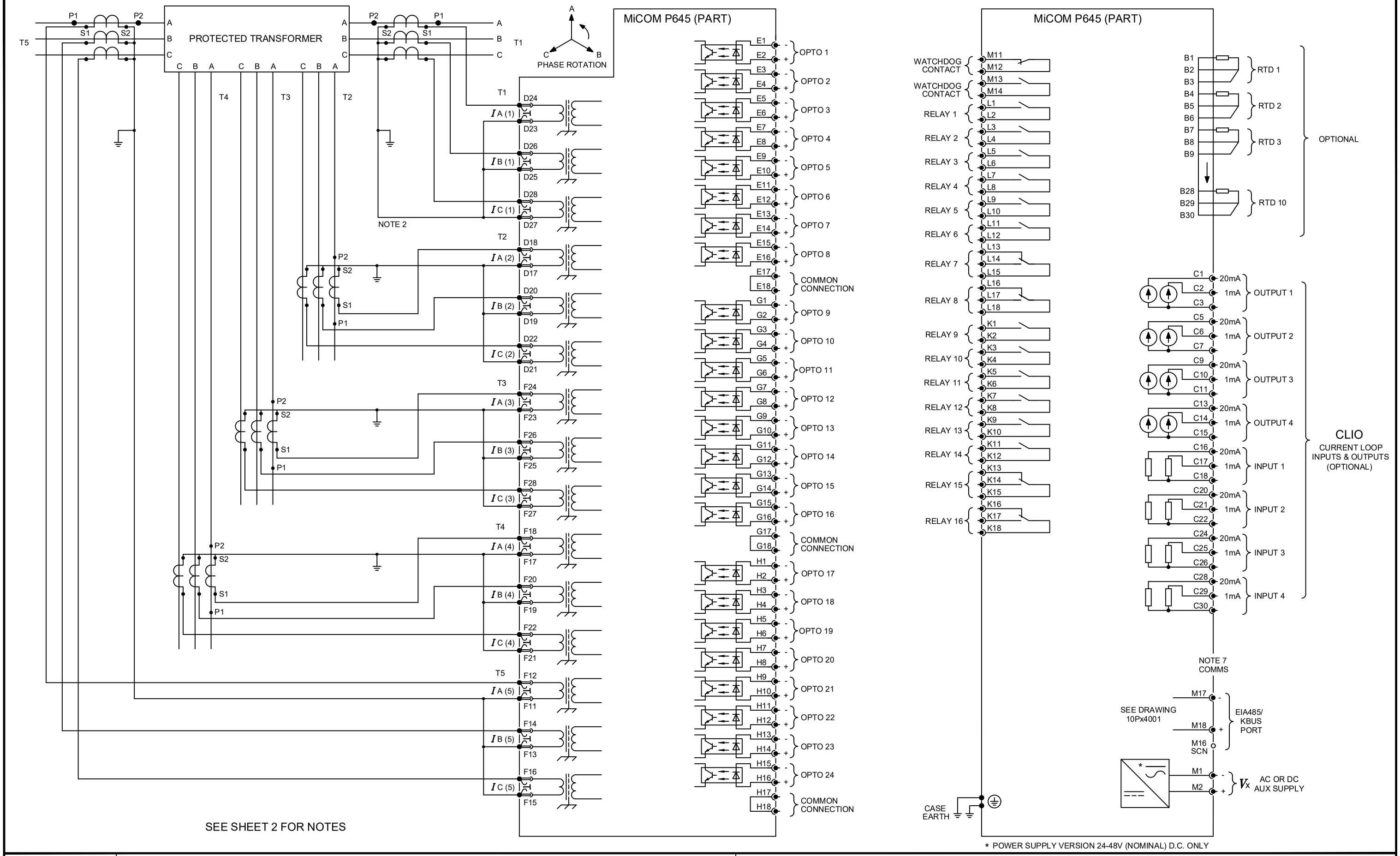




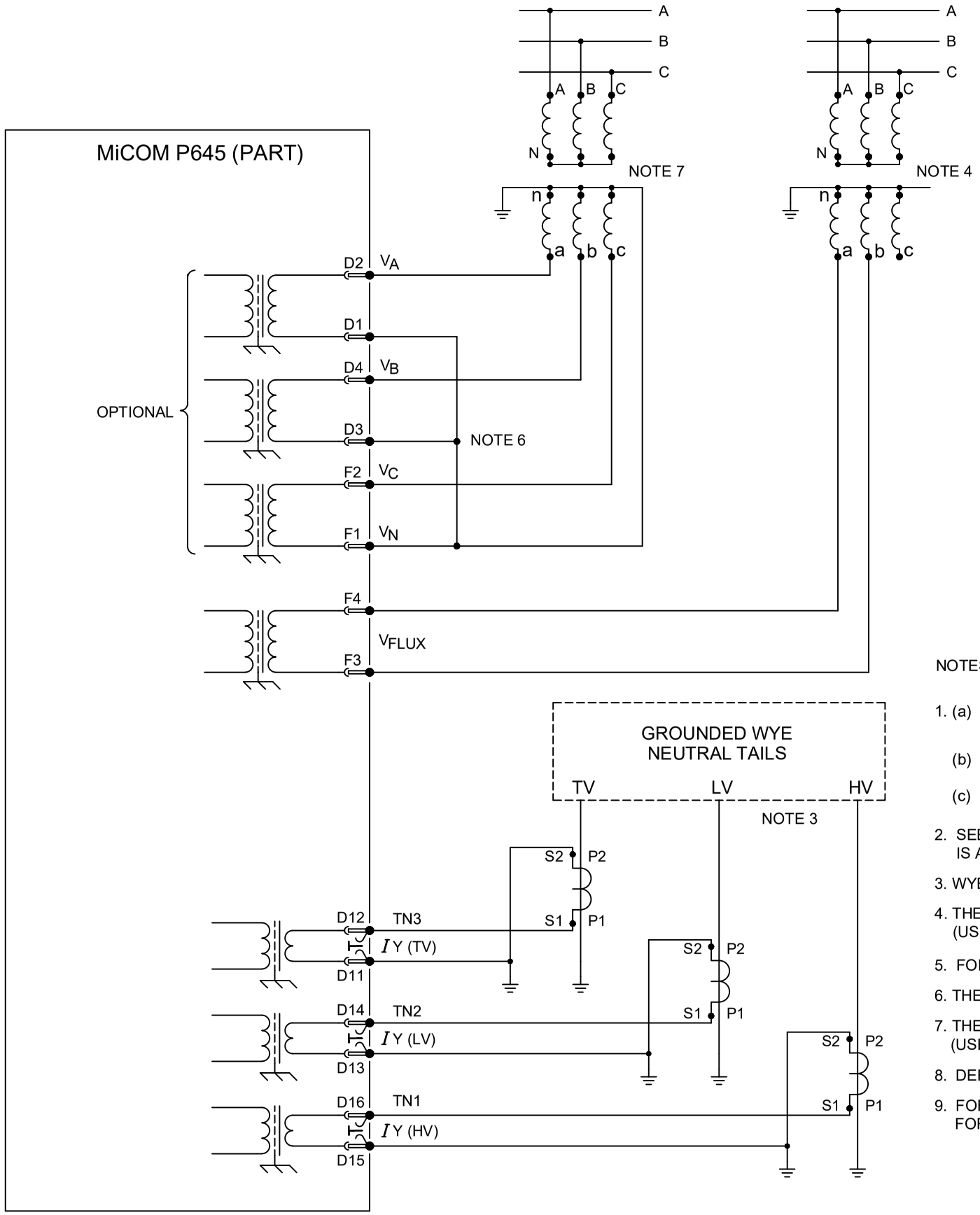
NOTES:

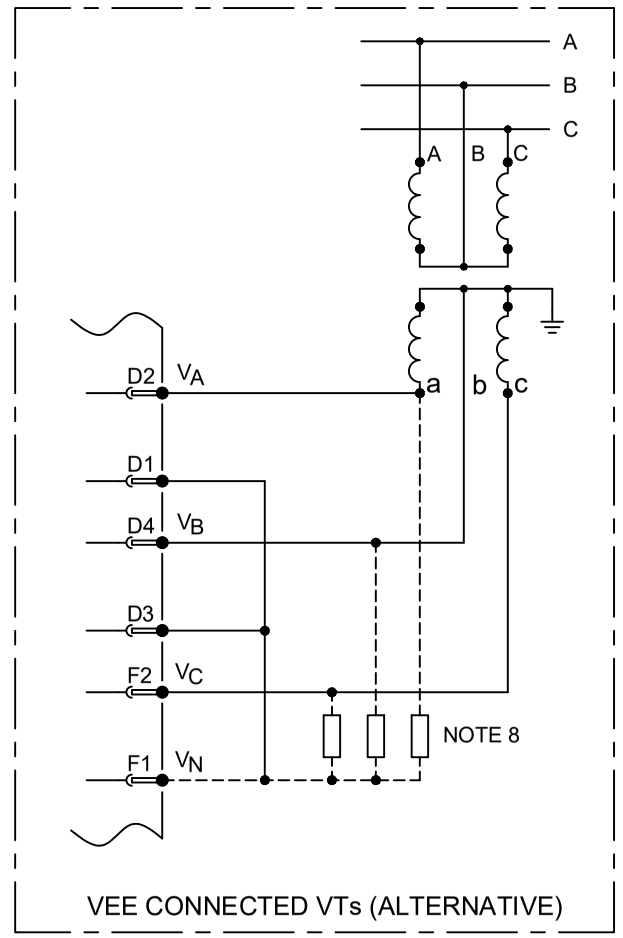
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. T1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

Issue: J	Revision: CID006234 Outlines updated to GE Format		Title: EXTERNAL CONNECTION DIAGRAM: 5 BIAS INPUT TRANSFORMER DIFFERENTIAL (24 I/P & 16 O/P) WITH 4 POLE VT INPUTS (60TE)		
Date: 4/30/2020	Name: S.J.BURTON		Drg No: 10P64504	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 26/09/2023	Name: S WOOTTON		Drg No: 10P64558	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	

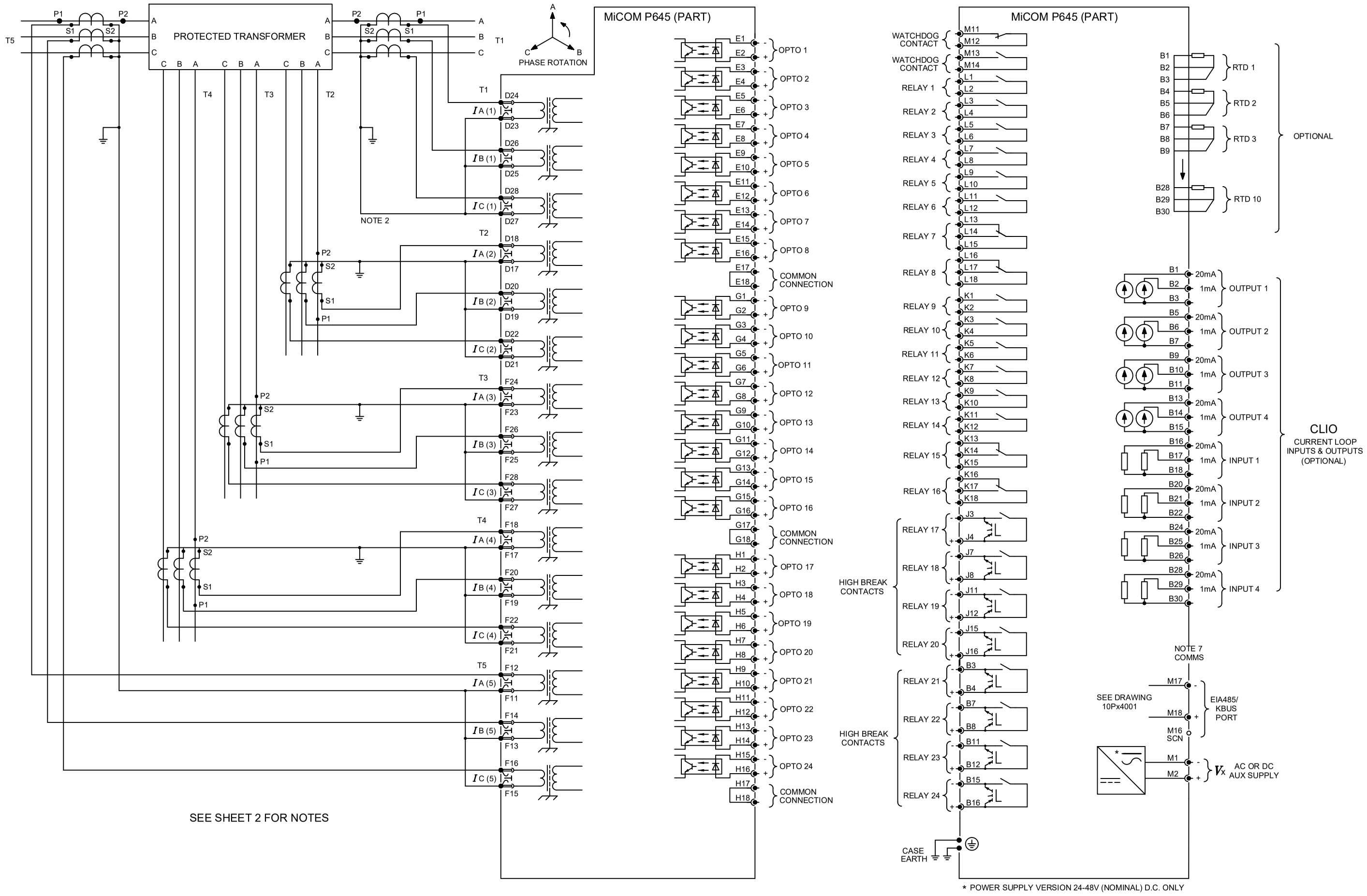




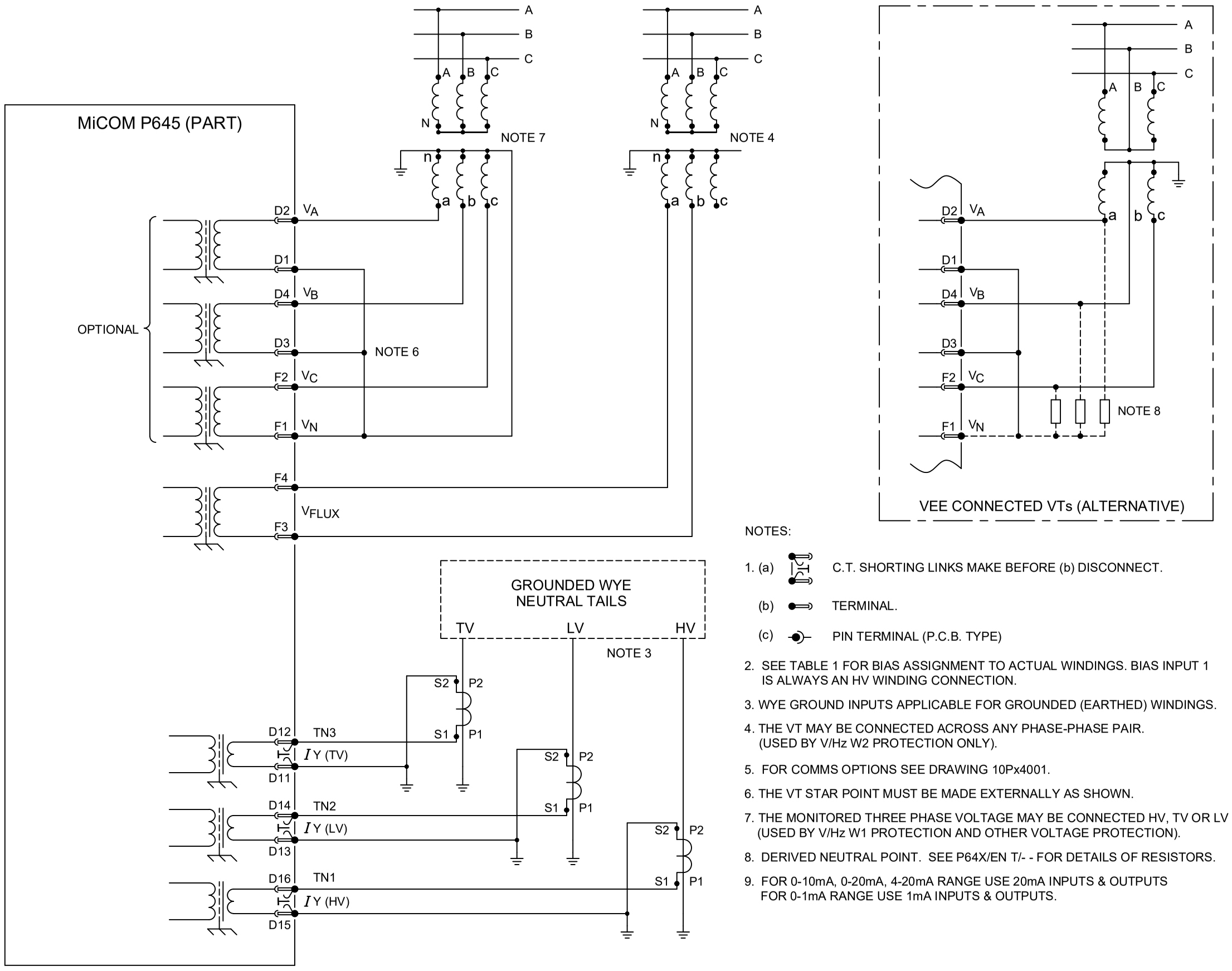
NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (24I/16O) 80TE		
Date: 26/09/2023	Name: S WOOTTON		Drg No: 10P64558	Sht: 2	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: -	



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24I/24O) 80TE		
Date: 26/09/2023	Name: S WOOTTON		Drg No: 10P64559	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	



NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24I/24O) 80TE	
Date: 26/09/2023	Name: S WOOTTON		Drg No: 10P64559	Sht: 2
Date:	Chkd:			Next Sht: -

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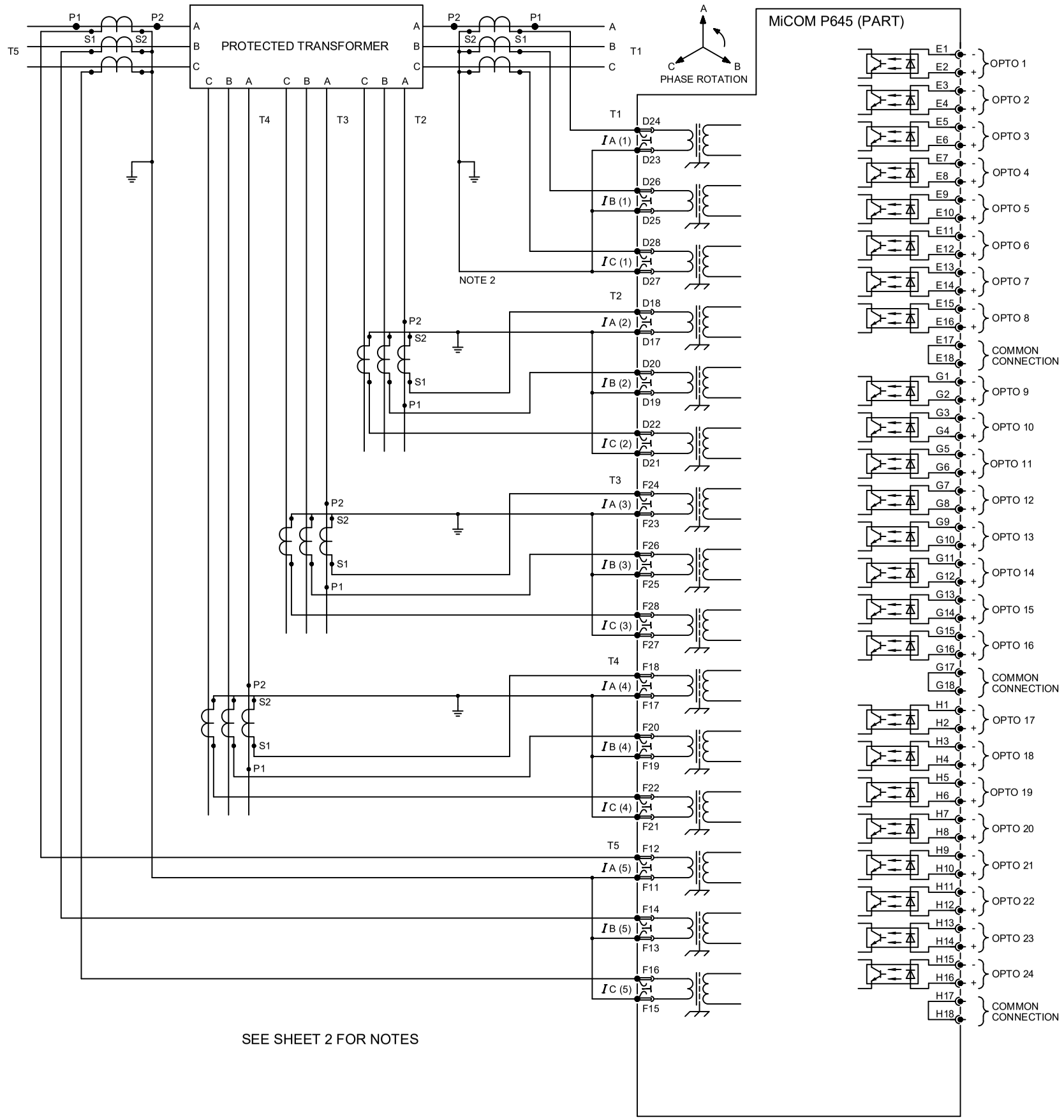
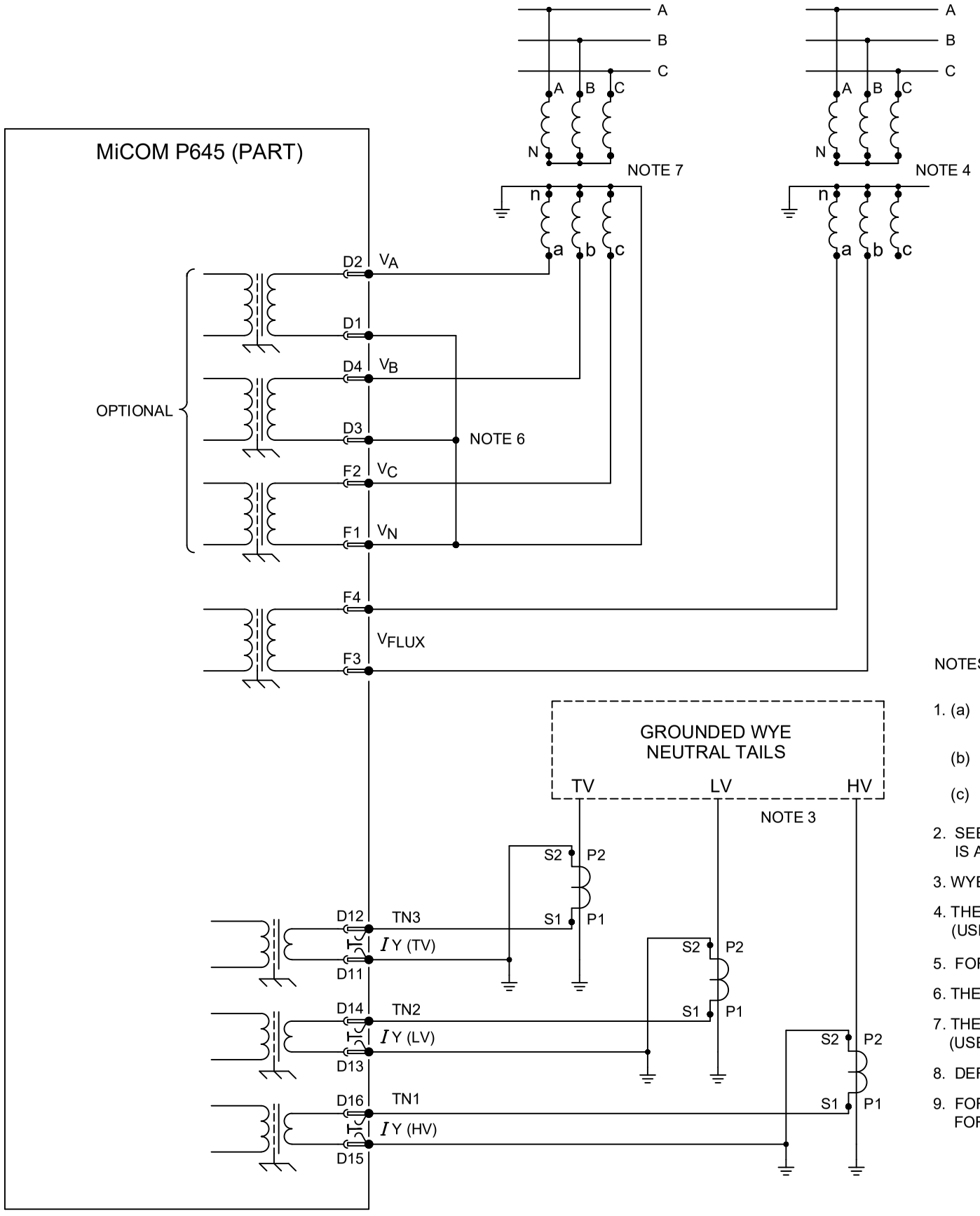
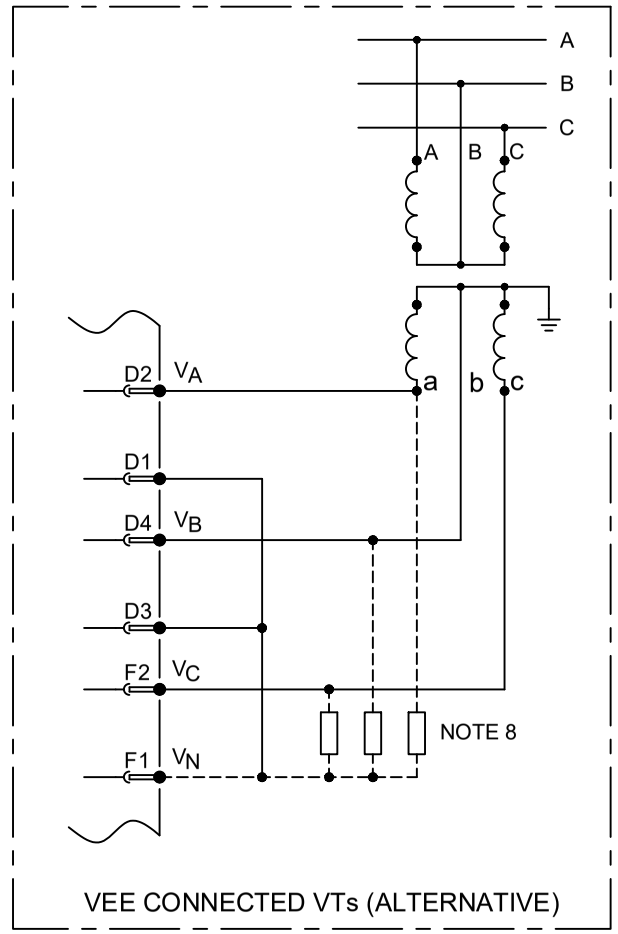


Issue: A	Revision: CID007575. INMTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS 80TE		
Date: 27/09/2023	Name: S WOOTTON		Drg No: 10P64565	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INTIAL ISISUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFF. WITH 4 POLE VT INPUTS (24I/24O) 80TE	
Date: 27/09/2023	Name: S WOOTTON		Drg No: 10P64565	Sht: 2
Date:	Chkd:			Next Sht: -

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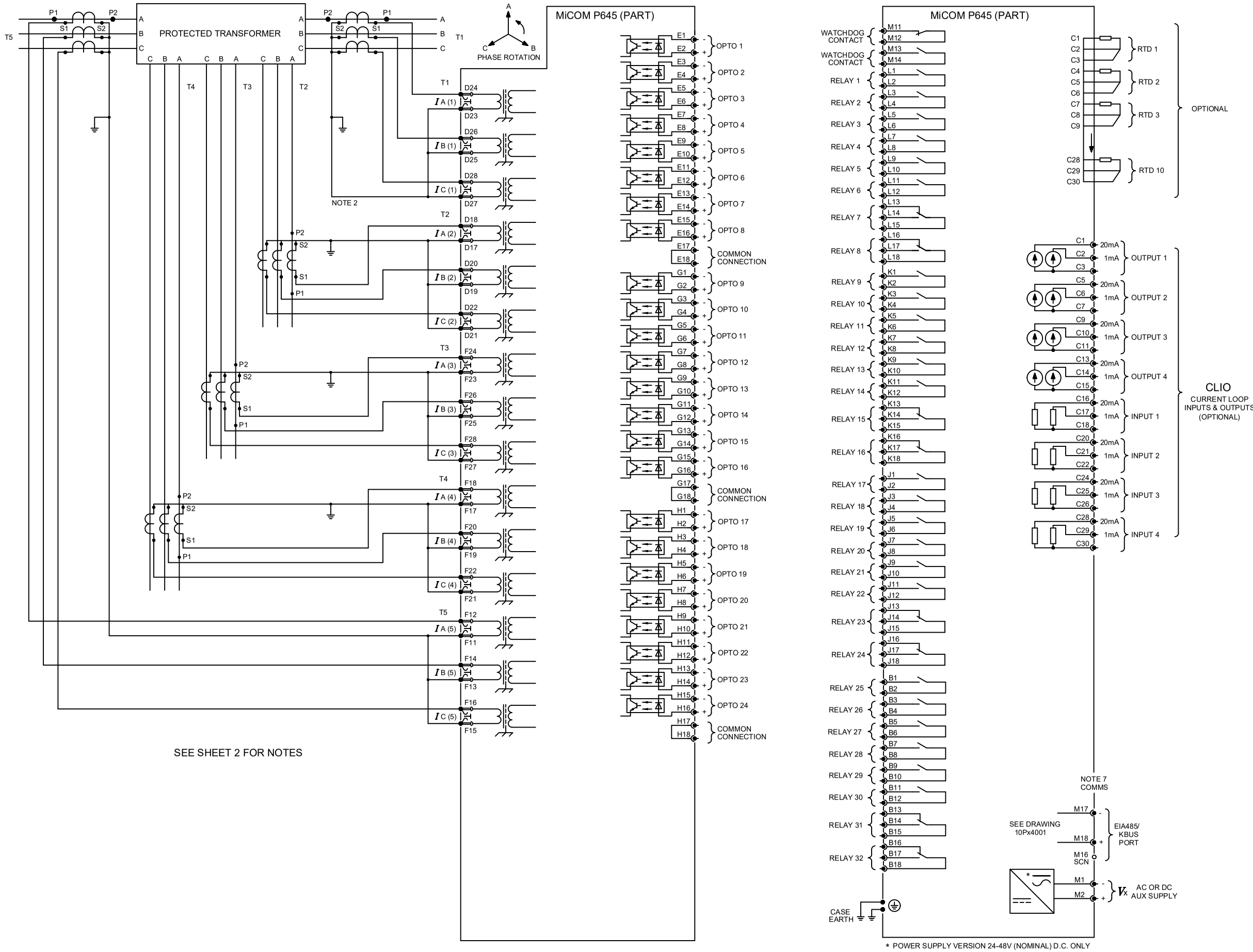
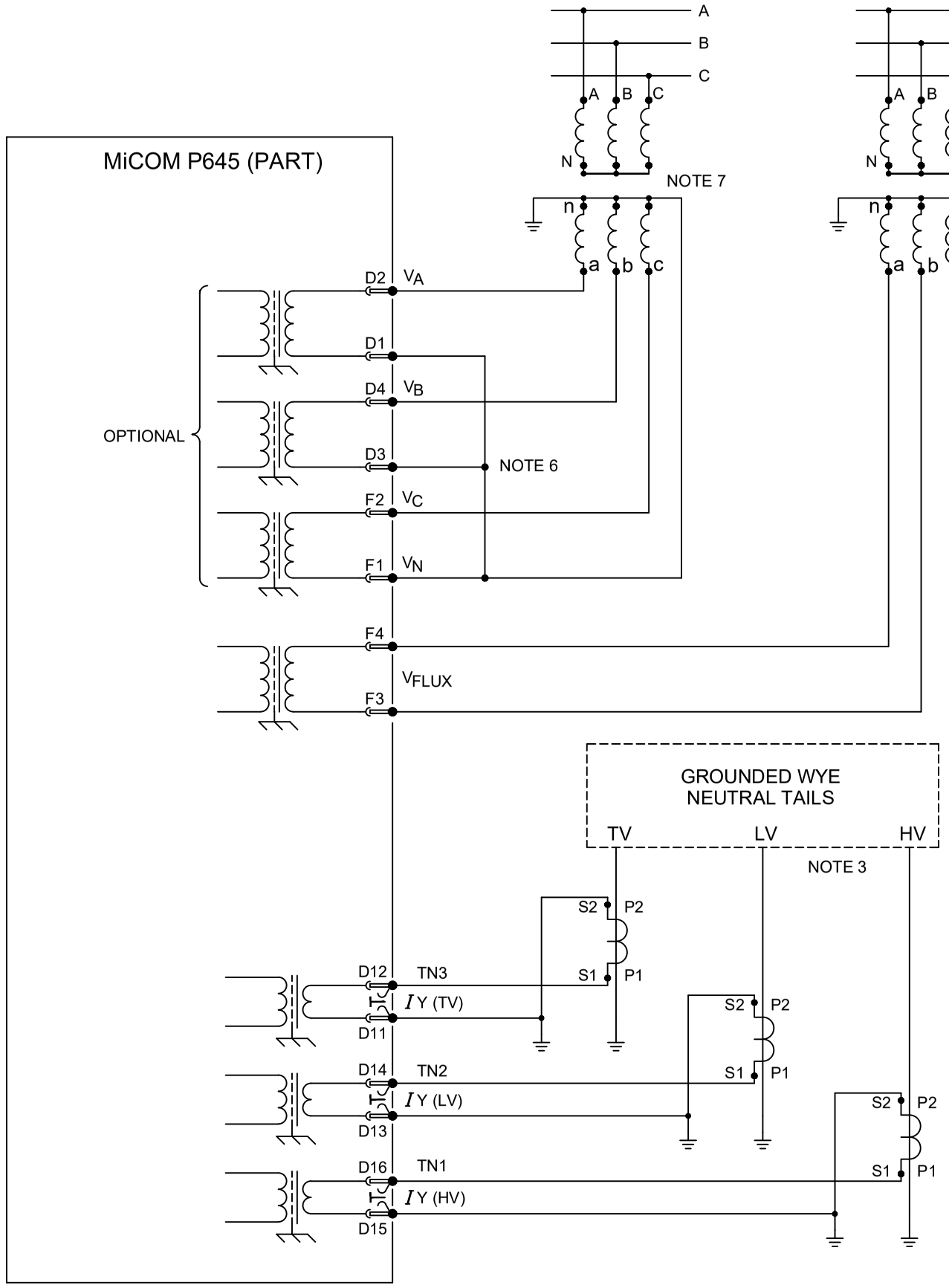
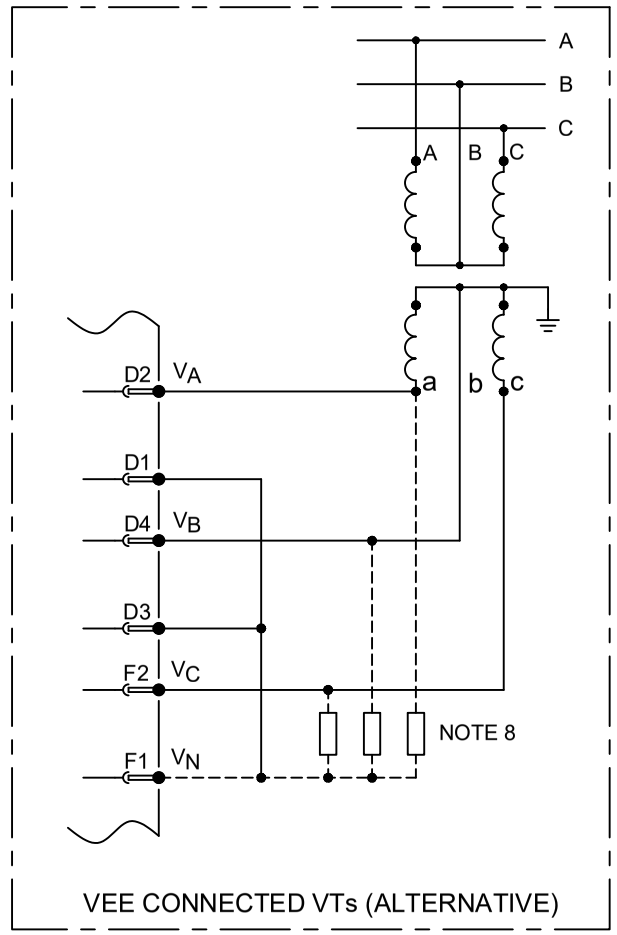


Issue: A	Revision: CID007575. INTIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24I/32O) 80TE		
Date: 27/09/2023	Name: S WOOTTON		Drg No: 10P64566	Sht: 1	GE VERNOVA ©UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford. ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
   FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INTIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (24I/32O) 80TE	
Date: 27/09/2023	Name: S WOOTTON		Drg No: 10P64566	Sht: 2
Date:	Chkd:			Next Sht: -

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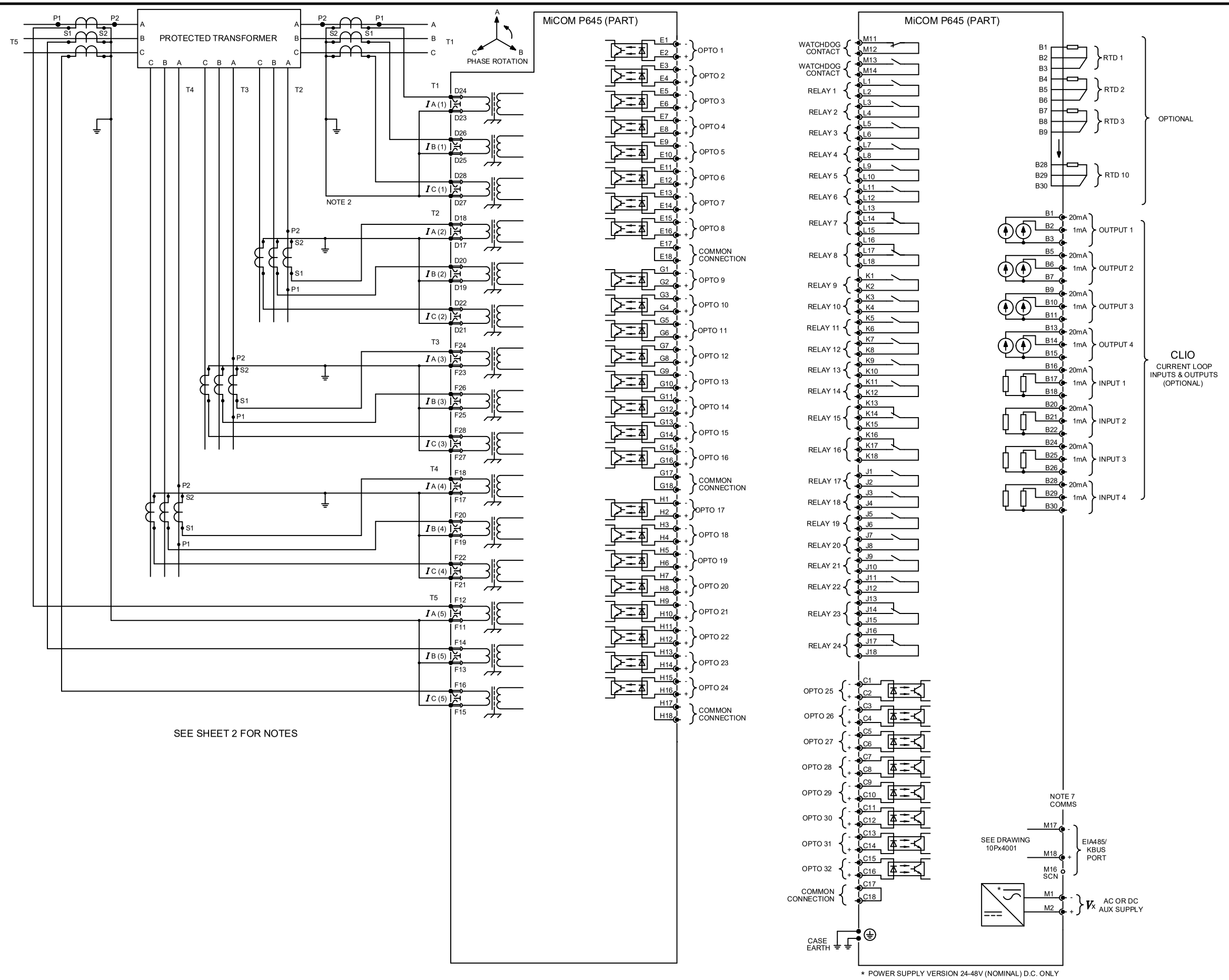
Stafford.
ST16 1WT, UK.



Issue: A	Revision: CID007575. INITIAL ISSUE.		Title:	EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/24O) 80TE	
Date: 02/10/2023	Name: S WIOOTTON		Drg No:	10P64573	Sht: 1
Date:	Chkd:				Next Sht: 2

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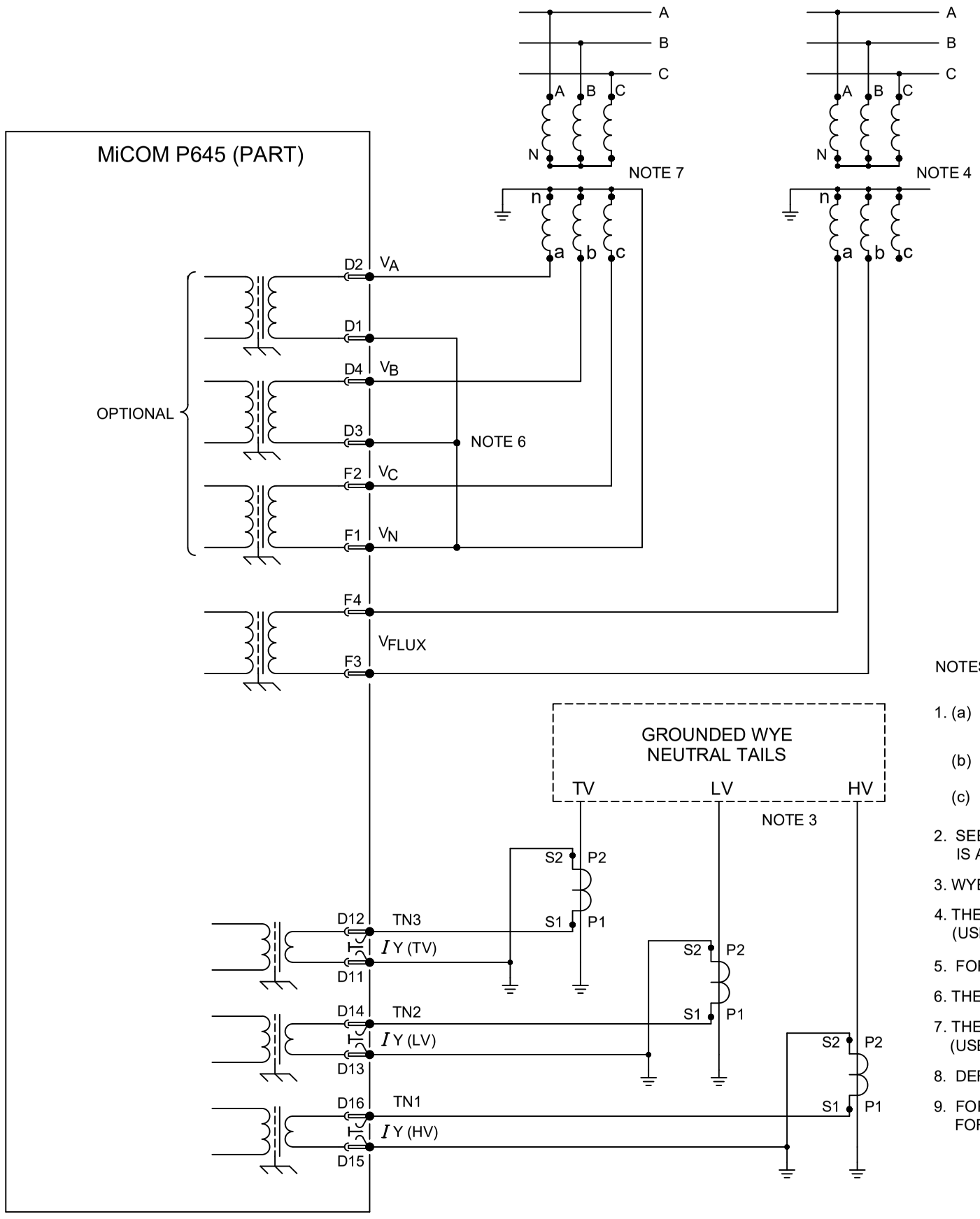
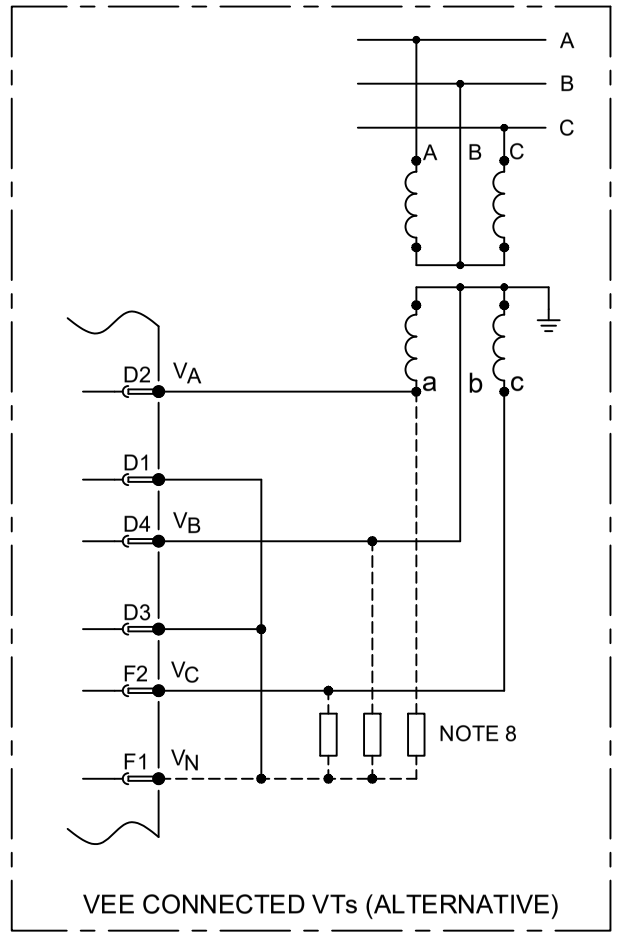
ST16 1WT, UK.





NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
6. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
7. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
8. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
9. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Issue: A	Revision: CID007575. INITIAL ISSUE		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/24O) 80TE	
Date: 02/10/2023	Name: S WOOTTON		Drg No: 10P64573	Sht: 2
Date:	Chkd:			Next Sht: -

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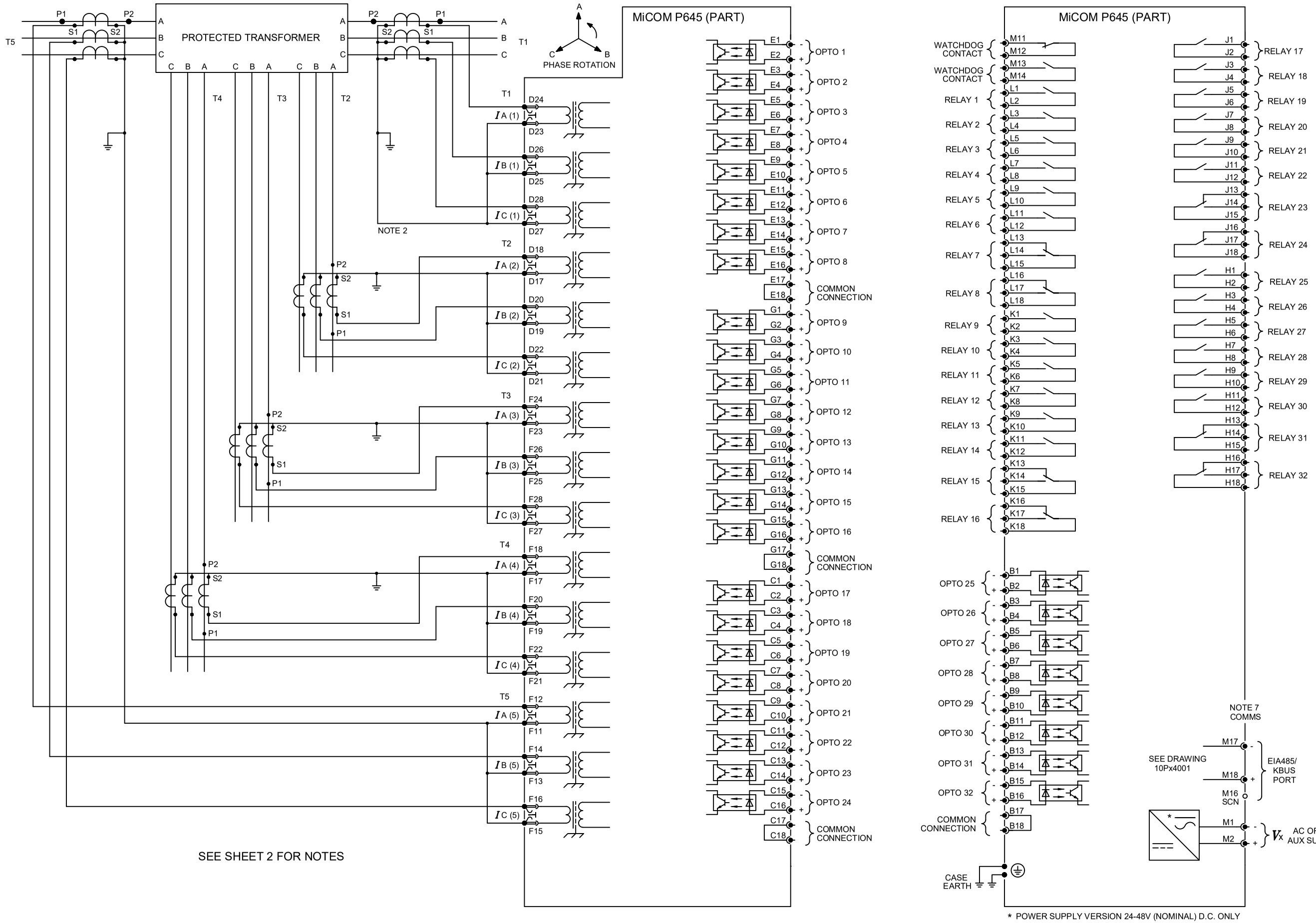

Issue: A	Revision: CID007575. INITIAL ISSUE.		Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (32I/32O) 80TE	
Date: 02/10/2023	Name: S WOOTTON		Drg No: 10P64576	Sht: 1
Date:	Chkd:			Next Sht: 2

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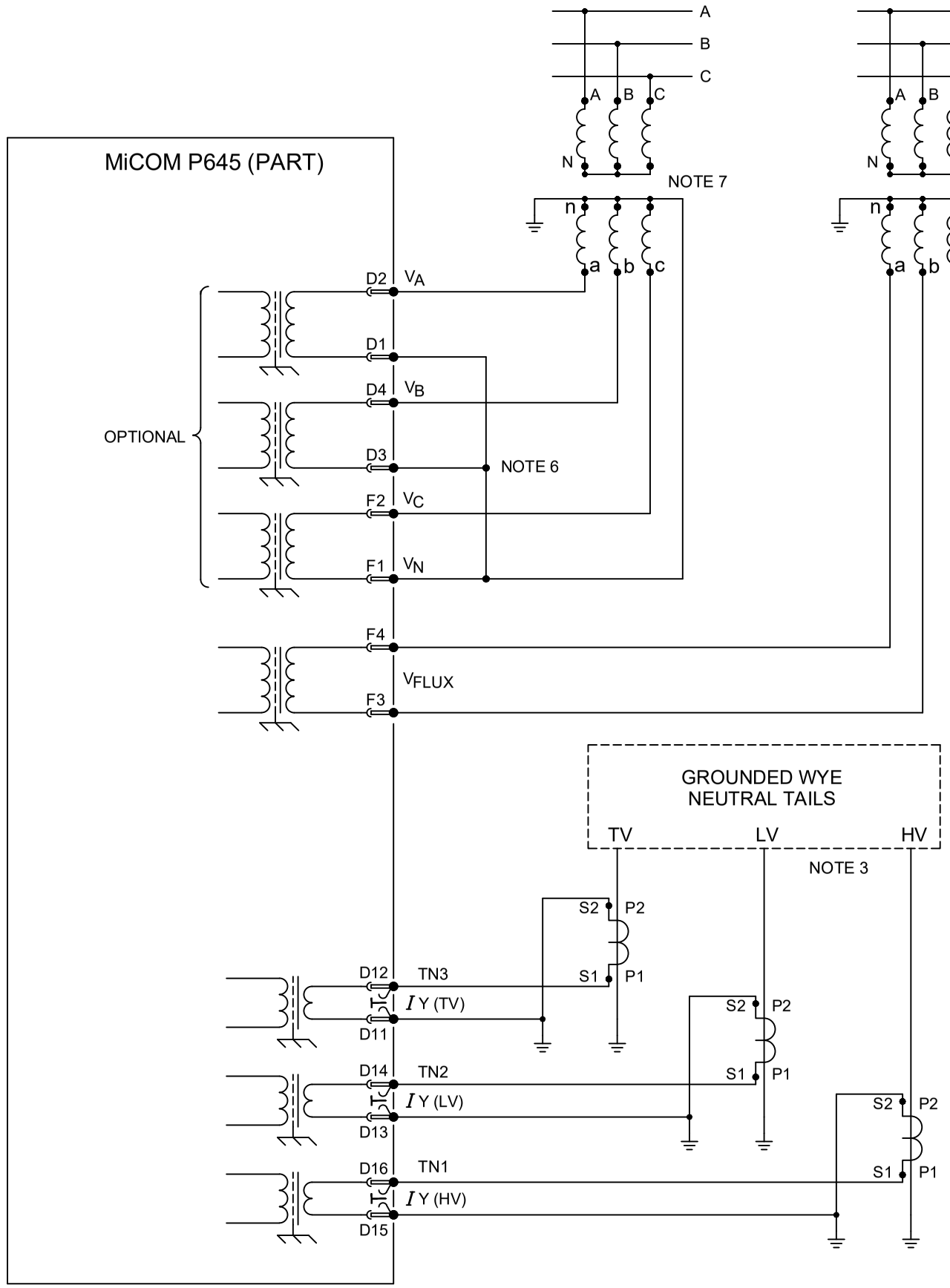

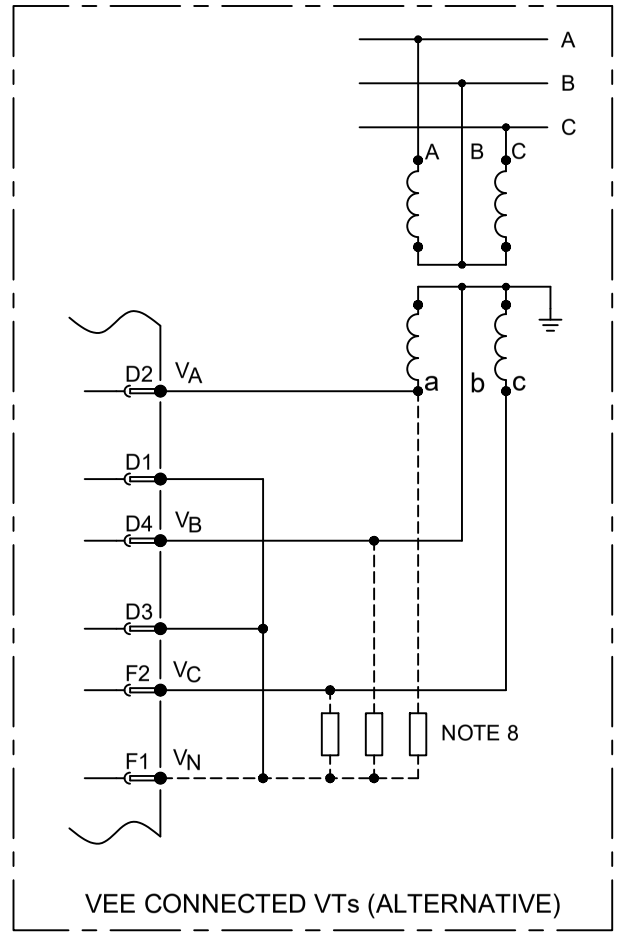

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
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Date: 02/10/2023	Name: S WOOTTON		Drg No: 10P64576	Sht: 2
Date:	Chkd:			Next Sht: -

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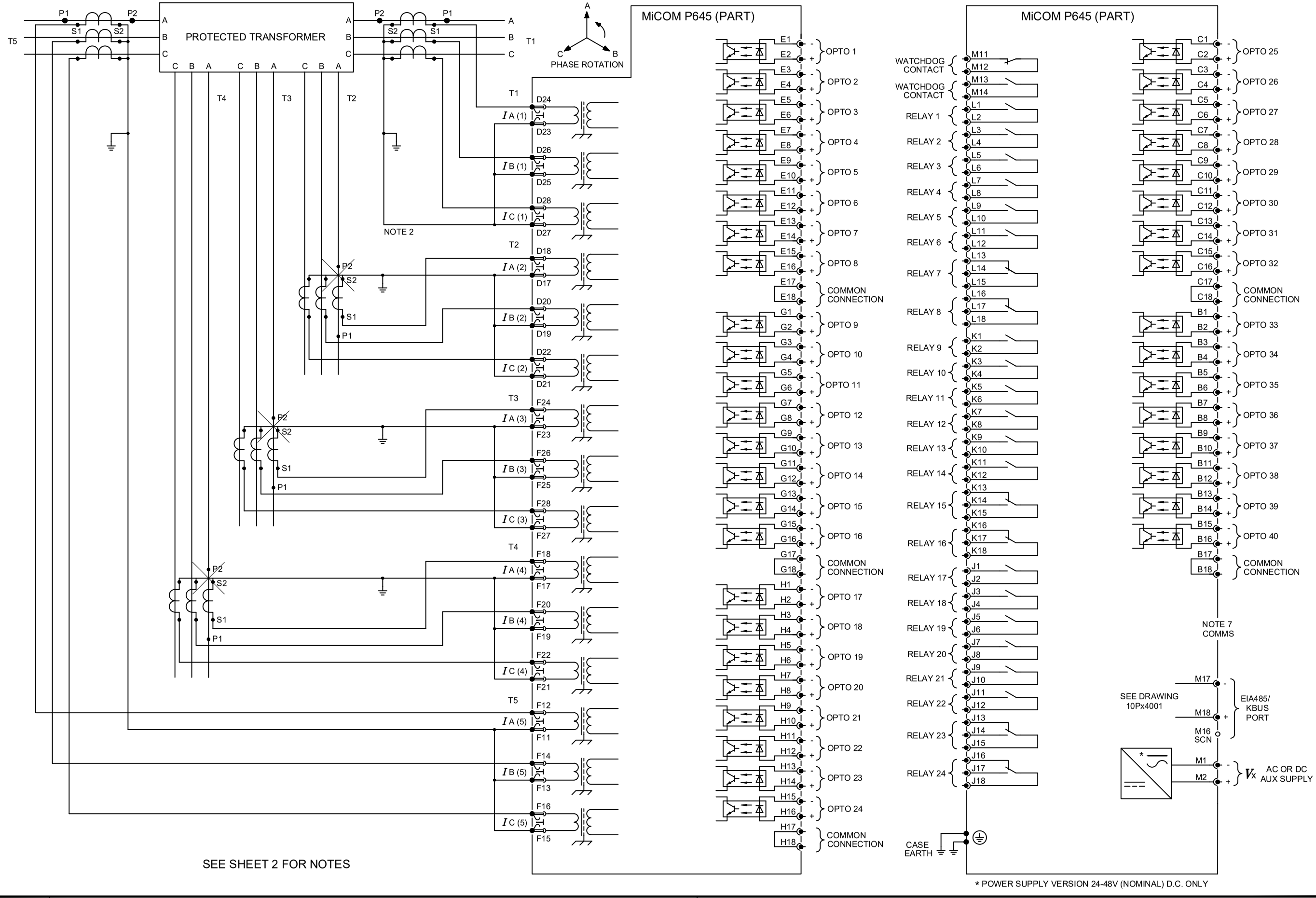

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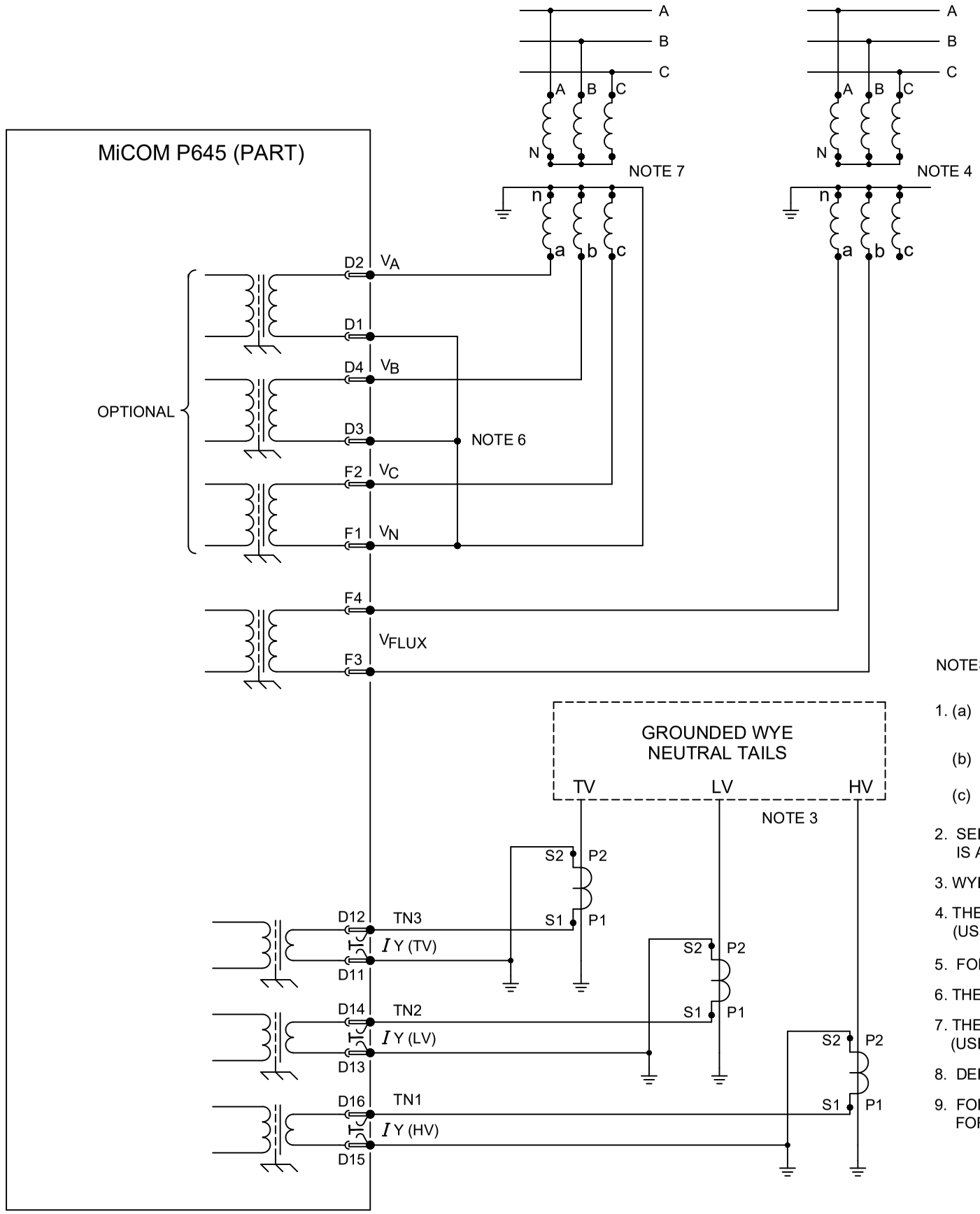
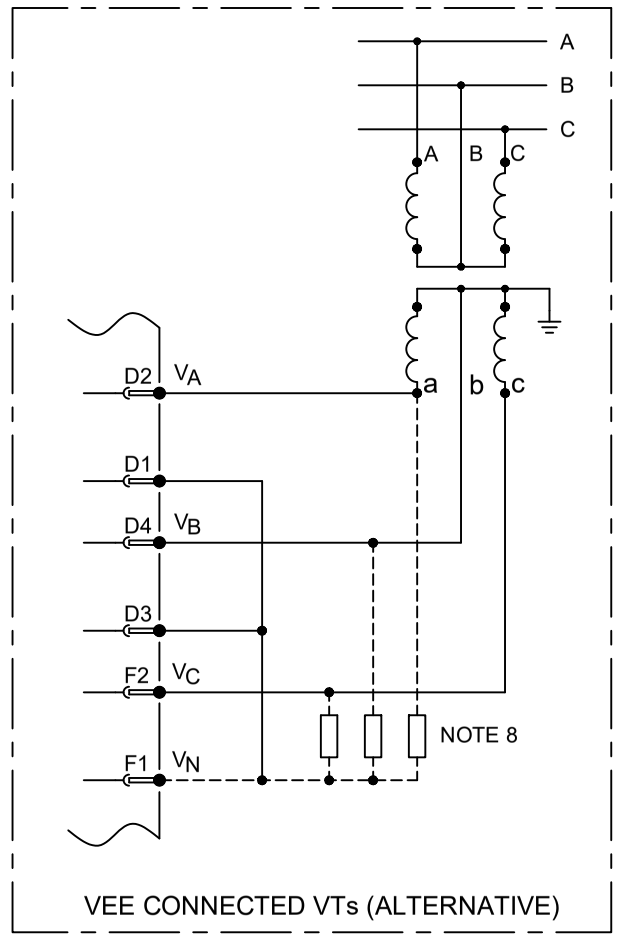
Date: 02/10/2023	Name: S WOOTTON		Drg No: 10P64577	Sht: 1	GE VERNOVA UK Grid Solutions Ltd St Leonards Building, Harry Kerr Drive, Stafford, ST16 1WT, UK.
Date:	Chkd:			Next Sht: 2	





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Date: 02/10/2023	Name: S WOOTTON		Drg No: 10P64577	Sht: 2
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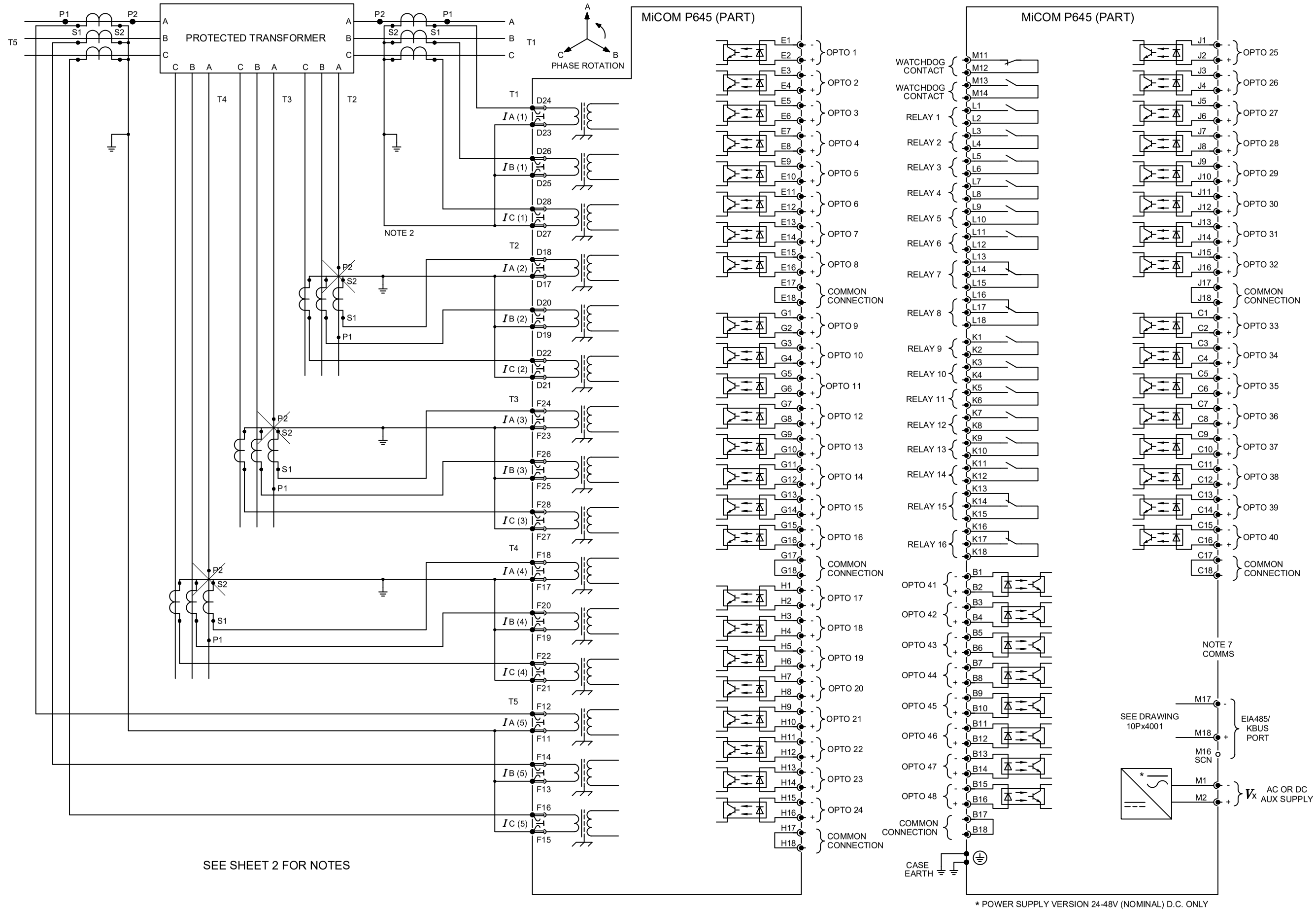

Issue: A	Revision: CID007575. INITIAL ISSUE	Title: EXTERNAL CONNECTION DIAGRAM 5 BIAS INPUT TRANSFORMER DIFFERENTIAL WITH 4 POLE VT INPUTS (48I/16O) 80TE	
Date: 02/10/2023	Name: S WOOTTON	Drg No: **10P64578**	Sht: 1 / Next Sht: 2
Date:	Chkd:		

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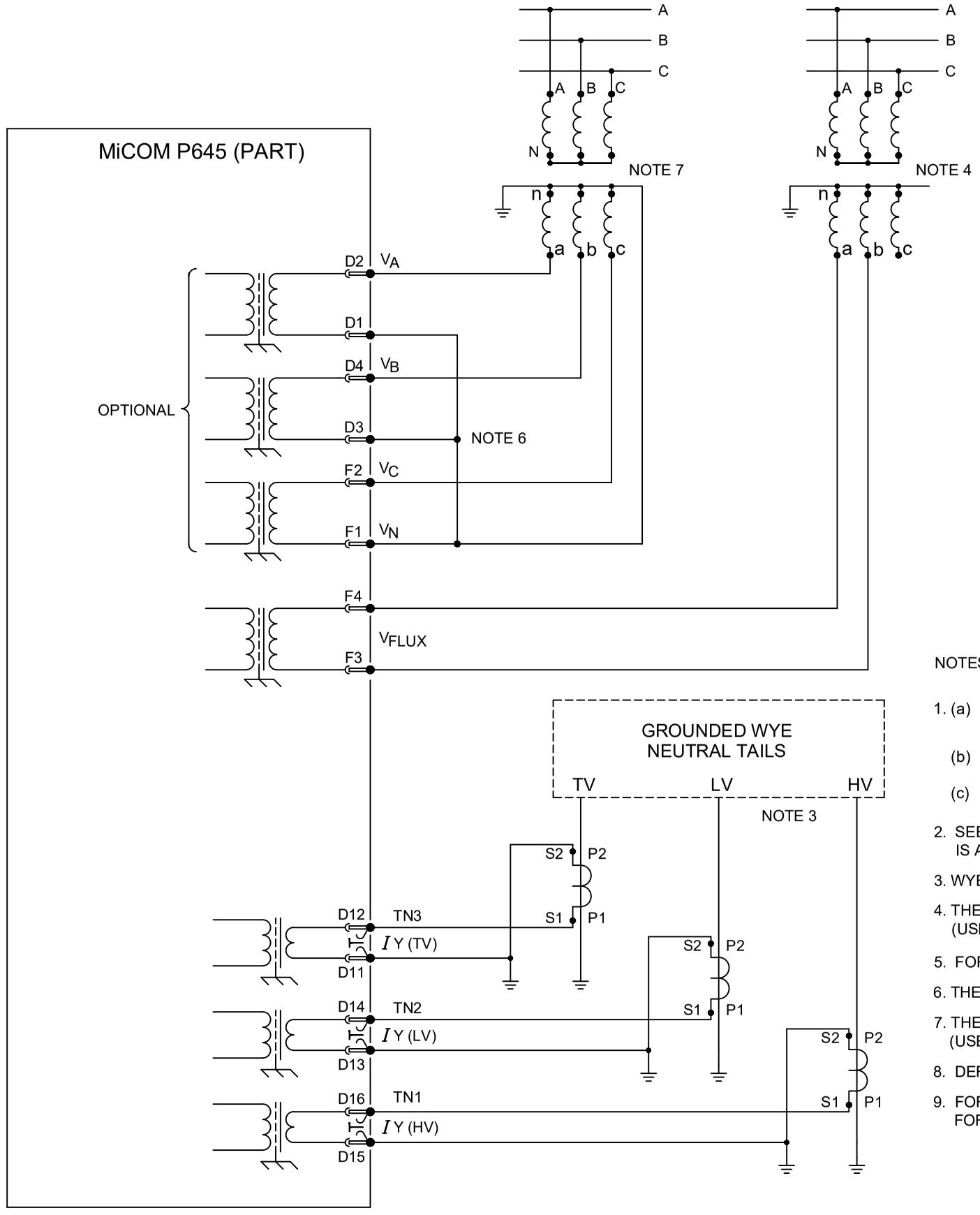

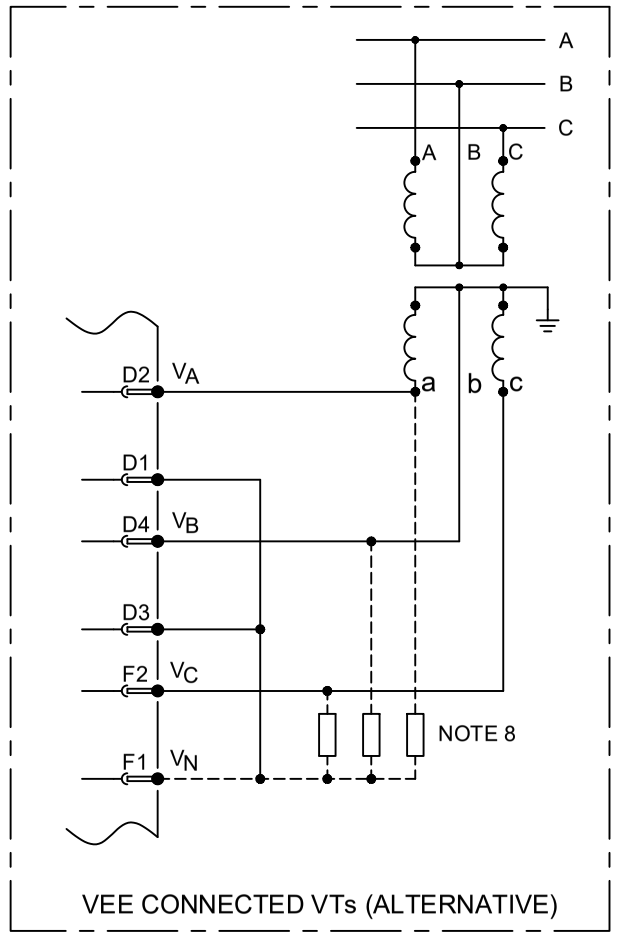

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Harry Kerr Drive,
Stafford.
ST16 1WT, UK.

APPENDIX D

VERSION HISTORY

1 HARDWARE AND SOFTWARE VERSION HISTORY

S/W Version Major	S/W Version Minor	H/W Version	Original Date of Issue	Description of Changes	S1 Compatibility	Technical Documentation
AB	-	Q	August 2024	First release of MiCOM 5th Generation transformer protection. Relay models: P642/3/5 are released based on software 91. The main changes in this new hardware and software release are as follows: ▪ A 10x performance increase in processing power over the previous Generation (4th Gen) ▪ Colour graphical HMI available as standard, and with native USB support. It includes 1 configurable page, for SLD, measurements and status signals ▪ Any model can be ordered in the 3 size cases: 40TE (W 203.2 mm or 8”), 60TE (W 304.8 mm or 12”) or 80TE (W 406.4 mm or 16”), with a variation in the number of I/O ▪ PRP, HSR and RSTP supported in the same order option ▪ CyberSentry IEC 62351-8 ▪ 5000 Events, 100 Faults, 1050s Oscillography and 128 Digital Signals ▪ Compliance to IEC 61850 Edition 2.1 ▪ Support for IEC 61850 Substitution - data points for status and measurement can be substituted ▪ Time Synchronization modelled in new LN LTIM/LTMS ▪ Support for Alarm Handling new LN CALH ▪ Ethernet port link status via new LN LCCH and new DDBs ▪ Top-down engineering - configuration of P40 including GOOSE from SCD file ▪ Configurable RCB name and GCB name ▪ Multi-level control, new DO MltLev - select local or remote for control. To comply to local and remote requirements ▪ Secure Event Logging aligned to IEC 62351-14 - separate audit log for security operations and Syslog updated to align with IEC 62351-14 ▪ Implementation of secure SSH (Secure Shell) communication to the relay from S1 Agile for configuration over Ethernet ▪ New Ethernet board - 1-2 Station Bus ports + Engineering port (CORTEC Hardware Option U/V/W/Y) ▪ Increased execution speed for REF. Trip time improved from 45 to 30ms at 2xIs	MiCOM S1 Agile v3.0.1 or later	P64-TM-EN-1

2 SOFTWARE VERSION COMPATIBILITY

IED S/W Version	Setting File Version	Menu Text File Version*8	PSL File Version
AB	AB	AB	AB

Notes:

*1: Compatible except for Disturbance recorder digital channel selection

*2: Additional functionality added such that setting files from earlier software versions will need additional settings to be made

*3: Compatible except for Disturbance recorder digital channel selection & settings for additional functionality will be missing

*4: Compatible except for the Disturbance recorder digital channel selection and the distance settings

*5: Compatible except for Disturbance recorder digital channel selection & the setting file contains a large number of Distance setting which will each produce an error on download

*6: Additional DDBs were added such that PSL files from earlier software versions will not be able to access them

*7: Additional DDB for the Distance protection will not be included

*8: Menu text remains compatible within each software version but is NOT compatible across different versions

Imagination at work

GE Vernova
St Leonards Building
Redhill Business Park
Stafford, ST16 1WT, UK
+44 (0) 1785 250 070
contact.centre@ge.com