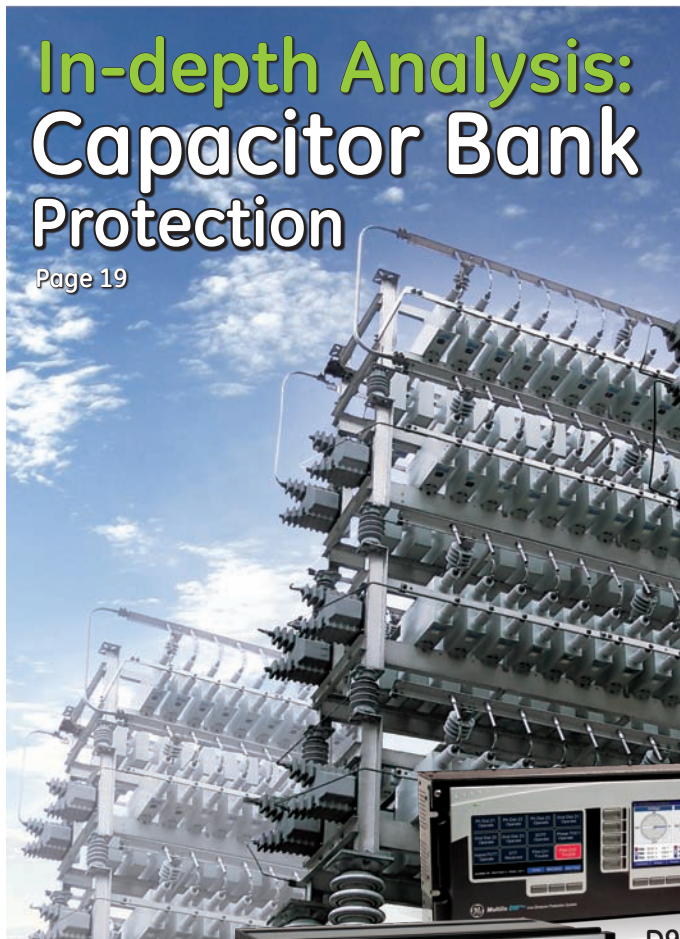


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The screenshot shows the AVTS Basic 3.1.1 software interface. On the left is a tree view of devices including Areva, AVO, GE, and MEGGER. The main area displays several tables of Modbus settings for different relay functions. A circular callout highlights a specific Modbus address.

Setting Name	Data Type	Min Value	Max Value	Enum Strings	Modbus Address	Num. Decim	Description
1 Function	Integer	0	1		24064	0	0 = Disabled ; 1 = Enabled
2 Pickup	Integer	0	100		24066	3	IOC Pickup setting, in pu
3 Delay	Integer	0	600		24067	2	Delay time in seconds

Setting Name	Data Type	Min Value	Max Value	Enum Strings	Modbus Address	Num. Decim	Description
1 Function	Integer	0	1		61184	0	0 = Disabled ; 1 = Enabled
2 Pickup	Integer	0	30		43362	3	Relay pickup, in pu
3 Slope	Integer	0	100		43363	0	Slope, in %
4 Delay	Integer	0	600		43364	2	Delay time in seconds

Setting Name	Data Type	Min Value	Max Value	Enum Strings	Modbus Address	Num. Decim	Description
1 Function	Integer	0	1		61193	0	0 = Disabled ; 1 = Enabled
2 Pickup	Integer	0	30		43371	3	Relay pickup, in pu
3 Slope	Integer	0	100		43372	0	Slope, in %
4 Delay	Integer	0	600		43373	2	Delay time in seconds

Setting Name	Data Type	Min Value	Max Value	Enum Strings	Modbus Address	Num. Decim	Description
1 Function	Integer	0	1		61202	0	0 = Disabled ; 1 = Enabled
2 Pickup	Integer	0	30		43380	3	Relay pickup, in pu
3 Slope	Integer	0	100		43381	0	Slope, in %
4 Delay	Integer	0	600		43382	2	Delay time in seconds

Setting Name	Data Type	Min Value	Max Value	Enum Strings	Modbus Address	Num. Decim	Description
1 Function	Integer	0	1		26432	0	0 = Disabled ; 1 = Enabled
2 Inom	Integer	0	2		26434	3	in pu
3 Pickup1	Integer	0	100		26435	2	in %
4 K_Stage1	Integer	0	100		26436	2	in Seconds
5 Tmin_Stage1	Integer	0	50		26437	3	in Seconds
6 Tmax_Stage1	Integer	0	1000		26438	1	in %
	Integer	0	1000		26439	2	in Seconds
	Integer	0	100		26440	1	in Seconds
	Integer	0	1000		26441	1	in Seconds

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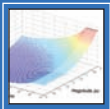
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Transmission Line Protection Principles



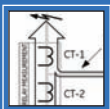
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Featuring advanced automation and control, dedicated digital fault recording, comprehensive communications including IEC61850, and an extensive local HMI, the **D90Plus** represents the next benchmark in protective relaying.



Transmission Line Protection Principles

1. Introduction

Transmission lines are a vital part of the electrical distribution system, as they provide the path to transfer power between generation and load. Transmission lines operate at voltage levels from 69kV to 765kV, and are ideally tightly interconnected for reliable operation.

Factors like de-regulated market environment, economics, right-of-way clearance and environmental requirements have pushed utilities to operate transmission lines close to their operating limits. Any fault, if not detected and isolated quickly will cascade into a system wide disturbance causing widespread outages for a tightly interconnected system operating close to its limits.

Transmission protection systems are designed to identify the location of faults and isolate only the faulted section. The key challenge to the transmission line protection lies in reliably detecting and isolating faults compromising the security of the system.

2. Factors Influencing line Protection

The high level factors influencing line protection include the criticality of the line (in terms of load transfer and system stability), fault clearing time requirements for system stability, line length, the system feeding the line, the configuration of the line (the number of terminals, the physical construction of the line, the presence of parallel lines), the line loading, the types of communications available, and failure modes of various protection equipment.

The more detailed factors for transmission line protection directly address dependability and security for a specific application. The protection system selected should provide redundancy to limit the impact of device failure, and backup protection to ensure dependability. Reclosing may be applied to keep the line in service for temporary faults, such as lightning strikes. The maximum load current level will impact the sensitivity of protection functions, and may require adjustment to protection functions settings during certain operating circumstances. Single-pole tripping applications impact the performance requirements of distance elements, differential elements, and communications schemes.

The physical construction of the transmission line is also a factor in protection system application. The type of conductor, the size of conductor, and spacing of conductors determines the impedance of the line, and the physical response to short circuit conditions, as well as line charging current. In addition, the number of line terminals determines load and fault current flow, which must be accounted for by the protection system. Parallel lines also



impact relaying, as mutual coupling influences the ground current measured by protective relays. The presence of tapped transformers on a line, or reactive compensation devices such as series capacitor banks or shunt reactors, also influences the choice of protection system, and the actual protection device settings.

3. GE Multilin Application Advantages

Before considering using a GE Multilin relay for a specific transmission line protection application, it is important to understand how the relay meets some more general application requirements for simplicity, security, and dependability. GE Multilin relays provide simplicity and security for single pole tripping, dependability for protection communications between line terminals, security for dual-breaker line terminals, and simplicity and dependability of redundant protection schemes.

3.1 Single-Pole Tripping

Single pole tripping using distance protection is a challenging application. A distance relay must correctly identify a single-phase fault, and trip only the circuit breaker pole for the faulted phase. The relay also must initiate the recloser and breaker failure elements correctly on the fault event. The distance elements protecting the unfaulted phases must maintain security during the open-pole condition and any reclosing attempts.

The D90^{Plus} Line Protection System and D60 Line Distance Relay use simple, dedicated control logic for single pole tripping applications. This control logic uses a Phase Selector, Trip Output and Open Pole Detector in conjunction with other elements as shown in the simplified block diagram.

The Trip Output is the central logic of single pole tripping. The Trip Output combines information from the Open Pole Detector, Phase Selector, and protection elements to issue a single pole or three pole trip, and also to initiate automatic reclosing and breaker failure. The Phase Selector is the key element for maintaining the security of single pole tripping applications, quickly and accurately identifying the faulted phase or phases based on measured currents and voltages, by looking at the phase angles between the positive sequence, negative-sequence, and zero-sequence components.

The Open Pole Detector ensures the relay operates correctly during a single pole trip, placing the relay in an open pole condition when a single pole trip command is issued, or one pole of the circuit breaker is open. The Open Pole Detector asserts on a single pole trip command, before the circuit breaker pole actually opens, to block protection elements that may misoperate under an open pole condition, such as negative sequence elements, undervoltage

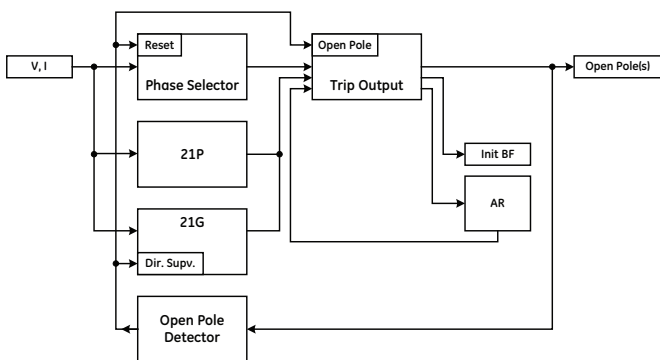


Figure 1. Single pole trip logic.

protection, and phase distance elements associated with the faulted phase (for example, AB and CA elements for an AG fault). The Open Pole Detector also resets and blocks the Phase Selector so the other distance elements may operate for evolving faults. The Open Pole Detector also accounts for line charging current and for weak infeed conditions.

Once the Open Pole Detector operates, a further trip will cause the Trip Output to declare a three pole fault, indicating either an evolving fault condition or a reclose onto a permanent phase-to-ground fault. This total logic simplifies the setting of the D60 for single pole tripping, and ensures dependable and secure operation when faced with single line-to-ground faults.

The L90 Line Differential Relay and the L60 Line Phase Comparison Relay are both phase-segregated, current only relays. Single pole tripping on these relays does not present any unusual challenges, as each phase of the protection element operates independently of the other unfaulted phases.

3.2 Communications

Often transmission lines are protected by using schemes that require communications with relays located at other line terminals. The reliability of the communications obviously impacts the reliability of the protection system. GE Multilin relays include features that maintain reliable operation of the protection communications during power line faults, communications channel delays, communications channel switching, and communications channel dropout.

Pilot protection: Pilot protection schemes, such as directional comparison blocking and permissive over-reaching transfer trip, use simple on/off communications between relays. There are many methods to send this signal. The most common method is to use contact closure to an external communication circuit, such as power line carrier, microwave, radio, or fiber optic communications. GE Multilin relays simplify fiber optic communications method by using internal fiber optic communications via Direct I/O, eliminating the need for external communications devices. Direct I/O is a reliable mechanism that is simple to configure, securely transmits digital status points such as tripping or blocking commands between relays via directly-connected or multiplexed fiber optic channels. Direct I/O operates within 2ms for high speed communications to the remote line end.

Direct I/O is available in any of the transmission line relays by adding an internal communications card. The output of the card can be IEEE C37.94, RS422 or G.703 communications to interface with fiber optic multiplexers, or may be a direct fiber connection to other relays. The communications card can be single-channel or dual-channel, to support point-to-point communications, dual point-to-point communications, or ring communications between up to 16 relays.

Line Current Differential: Communications is an integral piece of a line differential relay, as the currents from one line terminal must be sent to relays at other line terminals to perform the differential calculation. This requires the use of a digital communications channel, which is commonly a multiplexed channel where channel switching may occur. The analog information must be precisely

time synchronized between the line ends for the differential calculation to be correct. Synchronization errors show up as phase angle offset, where identical currents produce phasors with different phase angles, and transient errors, where changes in current are seen at different times at different measurement points. For example, on a 60 Hz system, every 1ms of time shift between terminals introduces a 21.6° phase shift into the measured currents.

There are two methods to account for the phase shift between line terminals due to the communications channel delay. One method is to measure the round-trip channel delay, and shift the local current phase by an angle equal to $\frac{1}{2}$ of the round-trip delay time. This method is simple to implement, but creates a transient error when the communications channel is switched. In addition, the differential element will be temporarily blocked when the communications channel switches, or noise in the communications channel causes communications packet loss.

The L90 Line Differential Relay employs a different method, using synchronous sampling by internally synchronizing the clocks on each L90. This method achieves high reliability, as the round-trip channel delay is not vitally important. The differential element successfully operates during channel switching or after packet loss, because the communications packets are precisely synchronized.

In the L90, synchronization is accomplished by synchronizing the clocks to each other rather than to a master clock. Each relay compares the phase of its clock to the phase of the other clocks and compares the frequency of its clock to the power system frequency and makes appropriate adjustments. The frequency and phase tracking algorithm keeps the measurements at all relays within a plus or minus 25 microsecond error during normal conditions for a 2 or 3 terminal system. In all cases, an estimate of phase error is computed and used to automatically adapt the restraint region of the differential element. The time synchronization algorithm can also use a GPS satellite clock to compensate for channel asymmetry. The use of a GPS clock is not normally required, except in applications such as a SONET ring where the communications channel delay may be asymmetric.

This method produces synchronization accurate to within 125 microseconds between the relays on each end of the protected line. By using internally synchronized sampling, the L90 can accommodate 4 consecutive cycles of communications channel loss before needing to block the differential element. If the communications channel is restored within 5 seconds of channel loss, the L90 differential element will restart on the first received packet, without any time synchronization delay, due to the inertia of the internal clocks of the relays.

Line Phase Comparison: As with line differential, communications is an integral part of phase comparison relaying. Simple binary communications, such as power line carrier or microwave, is used to send a pulse to the remote end when the phase angle of the measured current is positive. Coordination between the pulses from the remote end, and the phase angle measured at the local end, must be maintained.

The L60 Line Phase Comparison Relay directly solves two common challenges with the carrier signal. The first issue is channel delay. The channel delay is measured during commissioning and is entered as a setting in the phase comparison element. The remote phase angle measurements are buffered and delayed by this value to match the incoming pulses from the remote relays. The L60 has two communications channels, and two independent channel time delays, to support three-terminal lines.

The other common issue is pulse asymmetry of the carrier signal. Carrier sets may extend, either the mark (on) or space (off) signals at the receiving end compared with the originally sent signal. This difference is measured during commissioning by using oscillography data, and simply entered as a setting in the phase comparison element.

In addition, the L60 supports some other methods to improve the reliability of protection communications. For short lines with negligible charging current, the channel delay measurement can be automated by running a loop-back test during normal system conditions and measuring the difference between the sent and received pulses. The L60 also supports automated check-back of the carrier system. Under normal conditions, the relay can initiate transmission of and modulate the analog signal to exchange small amounts of information. This automatic loop-back can replace the carrier guard signal, and more importantly, verifies the entire communications path, including the relays on both ends.

3.3 Security for Dual-Breaker Terminals

Dual-breaker terminal line terminals, such as breaker-and-a-half and ring bus terminals, are a common design for transmission lines. The standard practice is to sum the currents from each circuit breaker externally by paralleling the CTs, and using this external sum as the line current for protection relays. This practice

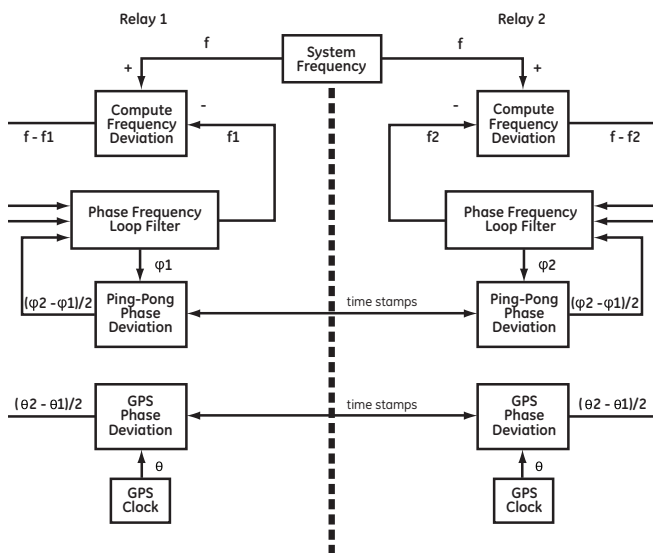


Figure 2. Clock synchronization block diagram for a two terminal system using L90 current differential system.

works well during actual line faults. However, for some external fault events, poor CT performance may lead to improper operation of line protection relays.

When current flows through a dual-breaker line terminal, the line current measured by a relay using external summation matches the actual line current only if the two CTs are accurate. The most significant relaying problem is CT saturation in either CT. The current measured by the relay may contain a large error current, which can result in the relay operating due to an incorrect magnitude or direction decision. This incorrect operation may also occur if the linear error current of the CTs due to accuracy class is close to the through current level. These errors appear in the measured phase currents. As a result, relays that calculate the negative sequence and zero sequence currents from the measured phase currents may also see errors.

Distance: Distance relays applied at dual-breaker line terminals are vulnerable to mis-operation on external faults. During a close-in reverse external fault, the voltage is depressed to a very low level, and the security of the relay is maintained by directional supervision. If one of the line CTs saturates, the current measured by the relay may increase in magnitude, and be in the opposite direction of the actual fault current, leading to an incorrect operation of the forward distance element for an external fault.

The D90^{Plus} Line Protection System and the D60 Line Distance Relay handles the challenge of dual-breaker line terminals by supporting two three-phase current inputs to support breaker failure, overcurrent protection, and metering for each circuit breaker. The relays then mathematically add these currents together to form the total line current used for distance and directional overcurrent relaying.

Directly measuring the currents from both circuit breakers allows the use of supervisory logic to prevent the distance element and directional overcurrent elements from operating incorrectly for reverse faults due to CT error. This supervisory logic does

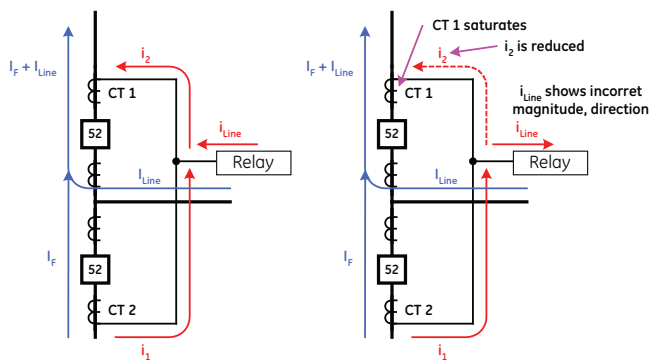


Figure 3.
Impact of CT saturation on two-breaker line applications
a) Accurate CTs preserve the reverse line current direction under weak remote feed.
b) Saturation of the CT carries the reverse current may invert the line current as measured from the externally summated CTs.

not impact the speed or sensitivity of the protection elements, operates during all load conditions, and correctly allows tripping during an evolving external-to-internal fault condition.

The dual-breaker line terminal supervisory logic essentially determines if the current flow through each breaker is either forward or reverse. Both currents should be forward for an internal fault, and one current should be forward and one reverse for an external line fault. The supervisory logic uses, on a per-phase basis, a high-set fault detector (FDH), typically set at 2-3 times the nominal rating of the CT, and a directional element for each CT input to declare a forward fault, for each breaker. The logic also uses, on a per-phase basis, a low-set fault detector (FDL), typically set at 1.5-2 times the nominal rating of the CT, and a directional element to declare a reverse fault, for each breaker.

Tripping is permitted during all forward faults, even with weak infeed at the dual-breaker terminal. Tripping is blocked for all reverse faults when one breaker sees forward current and one breaker sees reverse current. During an evolving external-to-internal fault, tripping is initially blocked, but when the second fault appears in the forward direction, the block is lifted to permit tripping.

Line Differential: Line differential protection is prone to tripping due to poor CT performance on dual-breaker terminals, as the error current from the CTs is directly translated into a differential current. The only possible solution for traditional line differential relays is to decrease the sensitivity of the differential element, which limits the ability of the differential element to detect low magnitude faults, such as highly resistive faults.

The L90 Line Differential Relay supports up to four three-phase current inputs for breaker failure, overcurrent protection, and metering for each circuit breaker. The relay then uses these individual currents to form the differential and restraint currents for the differential protection element.

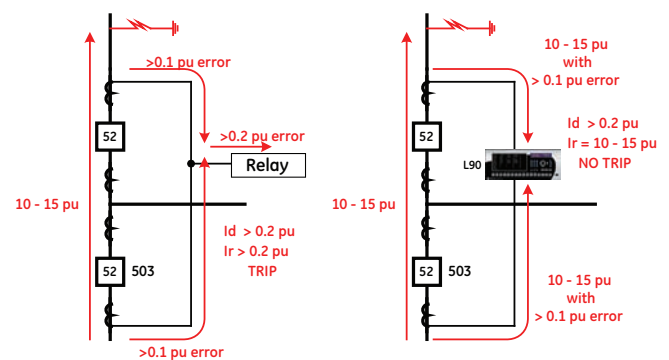


Figure 4.
Sensitivity of line differential system for dual-breaker applications.

The L90 differential element design explicitly accounts for the performance of the CTs for dual-breaker line terminals. Each L90 protecting a transmission line calculates differential and restraint quantities based on local information directly measured by the relay, and information received from relays located at the remote line ends. Tripping decisions are made locally by each relay.

The information sent by one L90 to the other L90s on the line is the local differential and restraint currents. The local differential current is the sum of all the local currents on a per-phase basis. One L90 can accept up to 4 current measurements, but only 2 currents are used for a dual-breaker application.

$$I_{LOC} = I_1 + I_2 + I_3 + I_4$$

The local restraint current is defined by the following equation for each phase.

$$I_{LOC_RESTRAINT} = \sqrt{(I_{LOC_REST_TRAD})^2 + MULT \cdot (I_{LOC_ADA})^2}$$

The starting point for the restraint is the locally measured current with the largest magnitude. This ensures the restraint is based on one of the measured currents for all fault events, and increases the level of restraint as the fault magnitude increases. ILOC_REST_TRAD is this maximum current magnitude applied against the actual differential characteristic settings. ILOC_ADA is the sum of the squares estimate of the measurement error in the current, and is used to increase the restraint as the uncertainty of actual measurement increases, such as during high magnitude fault events and CT saturation. MULT is an additional factor that increases the error adjustment of the restraint current based on the severity of the fault event and the likelihood the fault is an external fault, when CT saturation is most likely to cause an incorrect operation.

The values of I_{LOC} and $I_{LOC_RESTRAINT}$ are transmitted to the L90 relays located at the other line ends. The differential and restraint values used in the actual tripping decision combine both the local differential and restraint current, and the differential and restraint currents from the remote line ends. These calculations are performed individually on each phase.

$$I_{DIFF} = I_{LOC} + I_{REMOTE 1} + I_{REMOTE 2}$$

$$(I_{REST})^2 = (I_{LOC_RESTRAINT})^2 + (I_{REM 1_RESTRAINT})^2 + (I_{REM 2_RESTRAINT})^2$$

Considering the worst case external fault with CT saturation, the differential current IDIFF will increase due to the CT error that appears in ILOC. However, the restraint current IREST will increase more significantly, as the ILOC_RESTRAINT uses the maximum of the local currents, that is increased based on the estimation of CT errors and presence of CT saturation. The end result is a correct restraining of the differential element.

Phase Comparison: The L60 Line Phase Comparison Relay supports two three-phase current inputs for breaker failure, overcurrent protection, and metering for each circuit breaker. The relay then uses these individual currents to form the local phase angle information for use in the phase comparison scheme.

A phase comparison relay operates by comparing the relative phase angles of the current from each end of the transmission line. When the measured current exceeds the level of a fault detector, and the phase angles from each end of the line are in phase, the phase comparison relay operates. For a dual-breaker application using an external sum, the saturation of one CT may cause the relay current to increase high enough to operate the fault detector. Because the current from the unsaturated CT predominates in this waveform, the phase angle of the relay current may change. If the phase angle of the relay current is in phase with the relay current at the remote end of the line, the relay will trip.

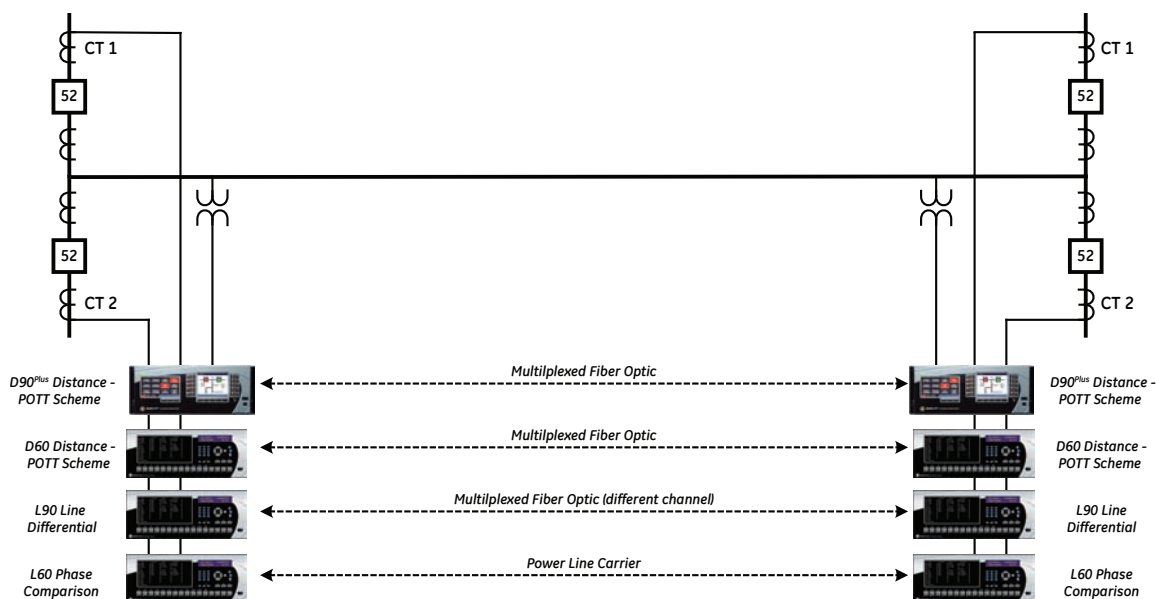


Figure 5. Redundancy Requirements - Alternate main protection possibilities from GE Multilin.

The L60 in dual-breaker applications selects the appropriate phase angle, based on the information measured from the current flow through both circuit breakers. The relay uses fault detectors on each current input, and develops the phase angle for each current input, and then special dual breaker logic consolidates the fault detector flags and the phase angle pulses for the line terminal.

The fault detector flag is set for a line terminal if either fault detector from the two breakers is picked up. The type of phase comparison protection scheme, tripping or blocking, controls the pulse combination logic. For a tripping scheme, a positive polarity is declared for the terminal if one breaker displays positive polarity with its respective fault detector picked up, while the other breaker either does not show negative polarity or its fault detector is not picked up.

3.4 Redundancy Considerations to Enhance Reliability

The reliability of transmission system protection is dependent on the reliability of the protection scheme used and the individual components of the protection scheme. Transmission protection systems typically use redundancy to increase the dependability of the system. There are two general methods of implementing redundancy. One method is to use multiple sets of protection using the same protection scheme. The other method is to use multiple sets of protection using different protection principles. Depending on the voltage class, either method of redundancy may involve using 2 or 3 sets of protection. In both cases, the goal is to increase dependability, by ensuring the protection operates for a fault event. Security may be improved through the use of so-called voting schemes (e.g. 2-out-of-3), potentially at the expense of dependability.

Multiple sets of protection using the same protection scheme involves using multiple relays and communications channels. This is a method to overcome individual element failure. The simplest method is to use two protection relays of the same type, using the same scheme and communications channel. This only protects against the failure of one relay. In some instances, relays of different manufacturers are used, to protect against common mode failures. It is also common to use redundant communications channels, in case of failure on one communications channel. Often, the communications channels use different methods, such as power line carrier and fiber optic. This is especially true due to the concerns of power line carrier operation during internal fault events.

An alternative way to increase reliability through redundancy is to use multiple protection methods on the same line such as phase comparison and permissive over-reaching transfer trip, using different communications channels. This method protects against individual element failure of both relays and communications channels. More importantly, it protects against the failure of one of the protection methods. For example, a VT circuit fuse failure blocks a distance relay from operating, while a line differential system or phase comparison system will continue to operate. For this reason, often at least one current-only scheme, such as phase comparison or line differential, and then one pilot protection scheme based on distance relays are employed.

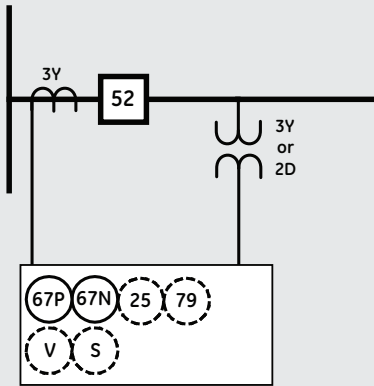
A second advantage of using multiple protection methods to protect one line is the ability to increase the security of the line. It is possible to implement a “voting” scheme, where at least 2 protection methods must operate before the line can be actually tripped. Such a voting scheme may be applied permanently on lines where security is an issue, such as major inter-tie lines. A voting scheme may also be applied only when the system is at risk, such as during wide-area disturbances, either automatically based on system conditions, or by command from system operators.

GE Multilin simplifies solutions when multiple protection schemes are used by providing both protective relays that only use current and protective relays that use both current and voltage. The L60 Line Phase Comparison Relay and the L90 Line Differential Relay are both current-only protection relays with different operating principles. The D90^{Plus}, D60 and D30 Line distance protection systems are full-featured distance relays. These relays are on a common hardware and software platform, simplifying engineering, design, installation, and operations issues. All of these relays support multiple communications options, including power line carrier, microwave, and fiber optic communications. The relays are also designed to communicate with each other, to implement voting schemes, reclosing control, and other applications.

4. Typical Applications

This section highlights some typical application of GE Multilin line protection relays. This section is not intended as a comprehensive list of possible applications. For questions about the correct relay for a specific application, visit www.GEMultilin.com to review the brochure for a specific relay model, or contact GE Multilin.

Directional Overcurrent



Typical Functions

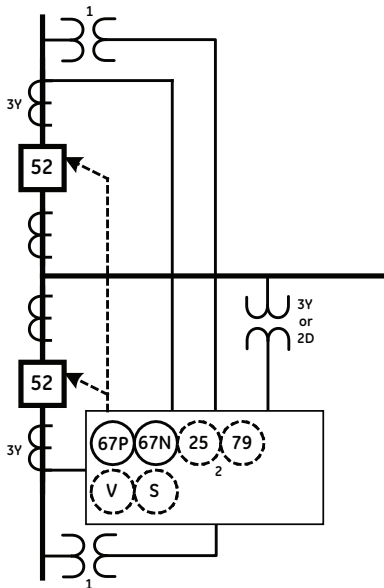
67P	Phase directional overcurrent
67N	Neutral directional overcurrent

Additional Functions

25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Functions	Typical Product Order Code
Typical Functions	F60-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
Alternative	D30-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
+ Additional functions	Included in typical
Alternative	Included in typical
Alternative	Included in typical

Directional Overcurrent – Dual Breaker



Typical Functions

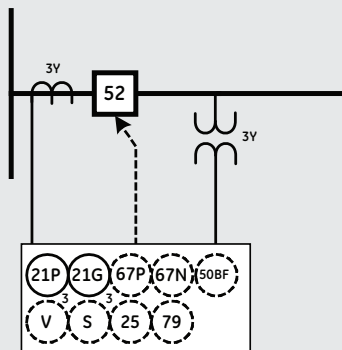
67P	Phase directional overcurrent
67N	Neutral directional overcurrent

Additional Functions

25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Functions	Typical Product Order Code
Typical Functions	D60-N02-HCH-F8L-H6P-M8L-PXX-UXX-WXX
+ Additional functions	Included in typical
External electrical sum of breaker currents (traditional method)	F60-N00-HCH-F8L-H6P-M8L-PXX-UXX-WXX D30-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
Only 1 synchrocheck function in F60 and D30	D60-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX

Stepped-Distance Protection



Typical Functions

21P	Phase distance
21G	Ground distance

Additional Functions

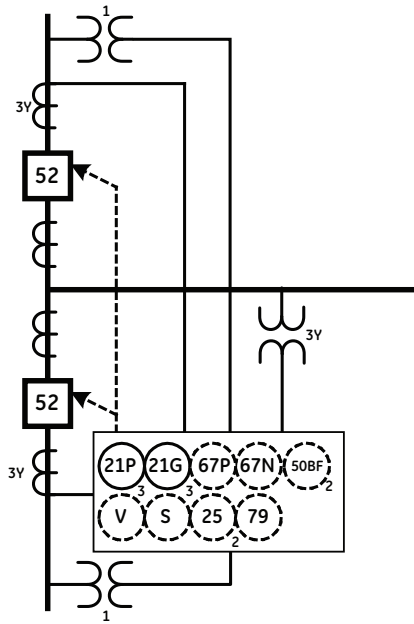
67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Synchrophasors

Phasor Measurement Unit

Functions	Typical Product Order Code
Typical Functions	D30-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
Alternative	D60-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX D90P-A-E-S-S-01-S-S-S-X-H-X-A-X-A-X-X-01-X
+ Additional functions	Included in typical No 50BF in D30
+ Synchrophasors	D60-N06-HCH-F8L-H6P-MXX-PXX-UXX-WXX D90P-A-E-S-S-01-P-S-S-X-H-X-A-X-A-X-X-01-X

Stepped-Distance Protection – Dual Breaker



Typical Functions

21P	Phase distance
21G	Ground distance

Additional Functions

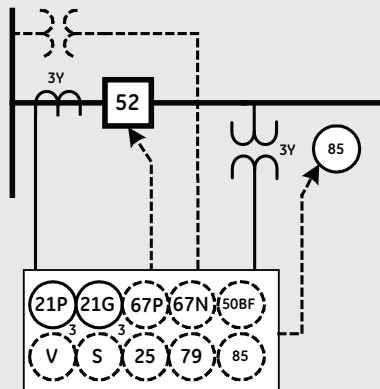
67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Synchphasors

Phasor Measurement Unit

Functions	Typical Product Order Code
Typical Functions	D90P-A-E-S-S-01-S-S-S-X-H-X-A-X-A-X-X-01-X D60-N02-HCH-F8L-H6P-M8L-PXX-UXX-WXX
+ Additional functions	Included in typical
External electrical sum of breaker currents (traditional method) Only 1 synchrocheck function in D30	D60-N00-HCH-F8L-H6P- MXX-PXX-UXX-WXX D30-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
+ Synchphasors	D90P-A-E-S-S-01-P-S-S-X-H-X-A-X-A-X-X-01-X D60-N08-HCH-F8L-H6P-M8L-PXX-UXX-WXX

Pilot Protection Schemes



Typical Functions

21P	Phase distance
21G	Ground distance
85	Power line carrier / microwave transmitter & receiver / fiber or digital channel

Additional Functions

67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Other Communications Options

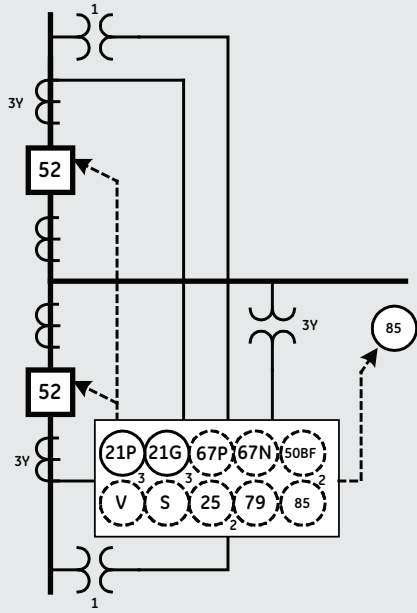
85	Inter-Relay Communications
85	Sonet Multiplexer

Synchphasors

Phasor Measurement Unit

Functions	Typical Product Order Code
Typical Functions 85 by others	D90P-A-E-S-S-01-S-S-S-X-H-X-A-X-A-X-X-01-X D60-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
+ Additional functions	Included in typical
+ Synchphasors	D90P-A-E-S-S-01-P-S-S-X-H-X-A-X-A-X-X-01-X D60-N06-HCH-F8L-H6P-MXX-PXX-UXX-WXX
Other Communications Options	
Direct I/O, 1300nm Singlemode Laser, 64km	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W7K
RS422 interface	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W7W
G.703	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W7S
C37.94	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W77
SONET Multiplexer	JungleMux with 86448 and 86441 units

Pilot Protection Schemes – Dual Breaker



Typical Functions

21P	Phase distance
21G	Ground distance
85	Power line carrier / microwave transmitter & receiver

Additional Functions

67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Other Communications Options

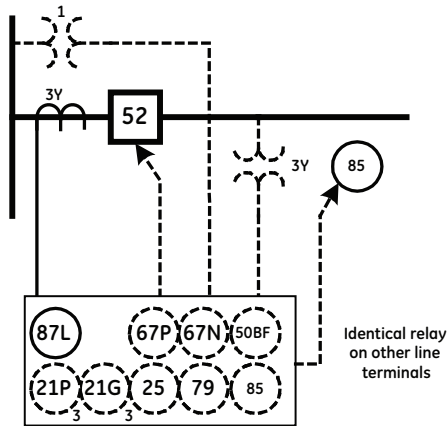
85	Inter-Relay Communications
85	Sonet Multiplexer

Synchphasors

Phasor Measurement Unit

Functions	Typical Product Order Code
Typical Functions 85 by others	D90P-A-E-S-S-01-S-S-X-H-X-A-X-A-X-X-01-X D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-WXX
+ Additional functions	Included in typical
+ Synchphasors	D90P-A-E-S-S-01-P-S-S-X-H-X-A-X-A-X-X-01-X D60-N06-HCH-F8L-H6P-M8L-PXX-UXX-WXX
External electrical sum of breaker currents (traditional method)	D60-N00-HCH-F8L-H6P-MXX-PXX-UXX-WXX
Other Communications Options	
Direct I/O, 1300nm Singlemode Laser, 64km	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W7K
RS422 interface	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W7W
G.703	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W7S
C37.94	D60-N00-HCH-F8L-H6P-M8L-PXX-UXX-W77
SONET Multiplexer	JungleMux with 86448 and 86441 units

Line Differential Protection



Typical Functions

87L	Line differential
85	Sonet Multiplexer

Additional Functions

21P	Phase distance
21G	Ground distance
67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Other Communications Options

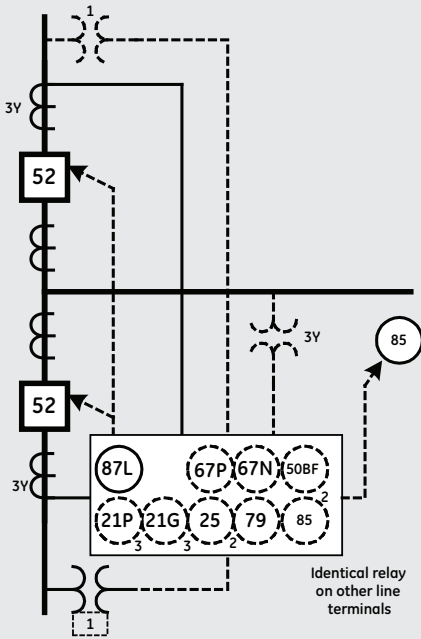
85	Inter-Relay Communications
----	----------------------------

Synchphasors

Phasor Measurement Unit

Functions	Typical Product Order Code
Typical Functions	L90-N00-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W7W
+ Additional functions	Included in typical
+ Synchphasors	L90-N06-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W7W
SONET Multiplexer	JungleMux with 86448 and 86443 units
Other Communications Options	D60-N08-HCH-F8L-H6P-M8L-PXX-UXX-WXX
Direct I/O, 1300nm Singlemode Laser, 64km	Included in typical
+ Synchphasors	L90-N00-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W7K
G.703	L90-N00-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W7S
C37.94	L90-N00-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W77

Line Differential Protection – Dual Breaker



Typical Functions

87L	Line differential
85	Sonet Multiplexer

Additional Functions

21P	Phase distance
21G	Ground distance
67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Other Communications Options

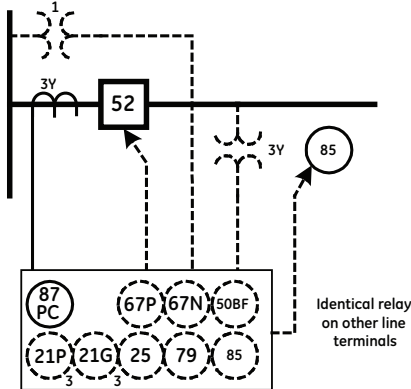
85	Inter-Relay Communications
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Synchrophasors

Phasor Measurement Unit

Functions	Typical Product Order Code
Typical Functions	L90-N02-HCH-F8L-H6P-L8L-NXX-SXX-UXX-W7W
+ Additional functions	Included in typical
+ Synchrophasors	L90-N08-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W7W
Electrical sum of breaker currents (traditional method)	L90-N00-HCH-F8L-H6P-LXX-NXX-SXX-UXX-W7W
SONET Multiplexer	JungleMux with 86448 and 86443 units
Other Communications Options	
Direct I/O, 1300nm Singlemode Laser, 64km	L90-N02-HCH-F8L-H6P-L8L-NXX-SXX-UXX-W7K
G.703	L90-N02-HCH-F8L-H6P-L8L-NXX-SXX-UXX-W7S
C37.94	L90-N02-HCH-F8L-H6P-L8L-NXX-SXX-UXX-W77

Phase Comparison Protection



Typical Functions

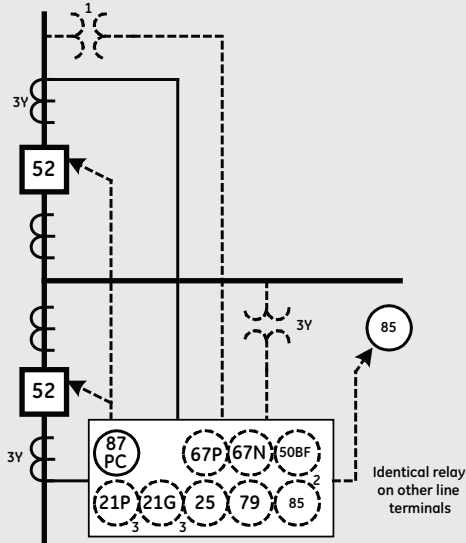
87PC	Phase Comparison
85	Power Line Carrier / Microwave

Additional Functions

21P	Phase distance
21G	Ground distance
67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Functions	Typical Product Order Code
Typical Functions	L60-N00-HCH-F8P-H6P-L8L-NXX-SXX-UXX-WXX

Phase Comparison Protection – Dual Breakers



Typical Functions

87PC	Line differential
85	Power Line Carrier / Microwave

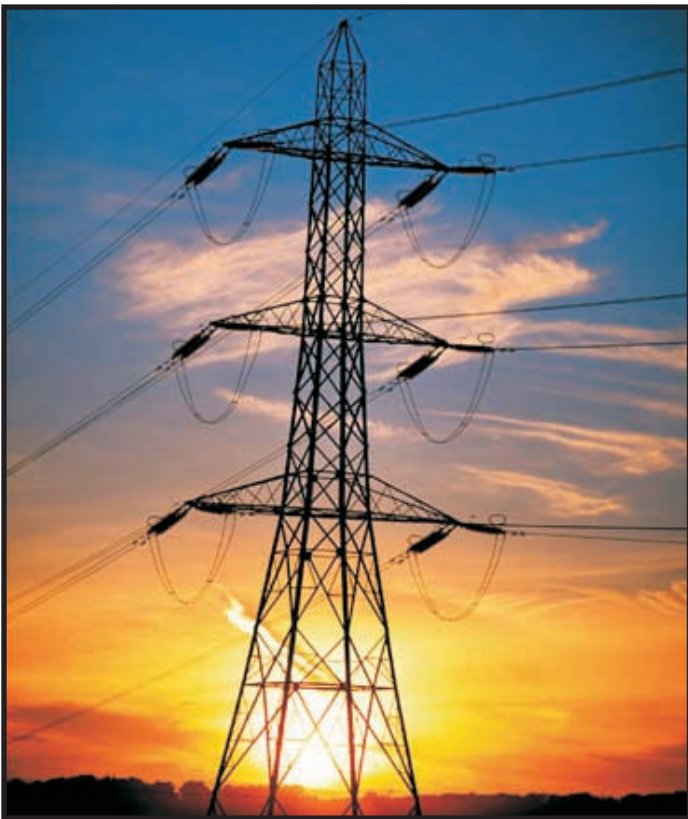
Additional Functions

21P	Phase distance
21G	Ground distance
67P	Phase directional overcurrent
67N	Neutral directional overcurrent
50BF	Breaker Failure
25	Synchrocheck
79	Reclosing
V, S	Voltage and Power metering

Functions	Typical Product Order Code
Typical Functions	L60-N00-HCH-F8P-H6P-L8L-NXX-SXX-UXX-WXX

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All banks need protection

Today, **shunt capacitor banks** play an increasingly vital role in **blackout prevention** and supporting the growth of **distributed generation** facilities like wind farms. Protecting this equipment has historically involved complex, custom protection schemes consisting of multiple products that rarely addressed the inherent system and bank unbalance.

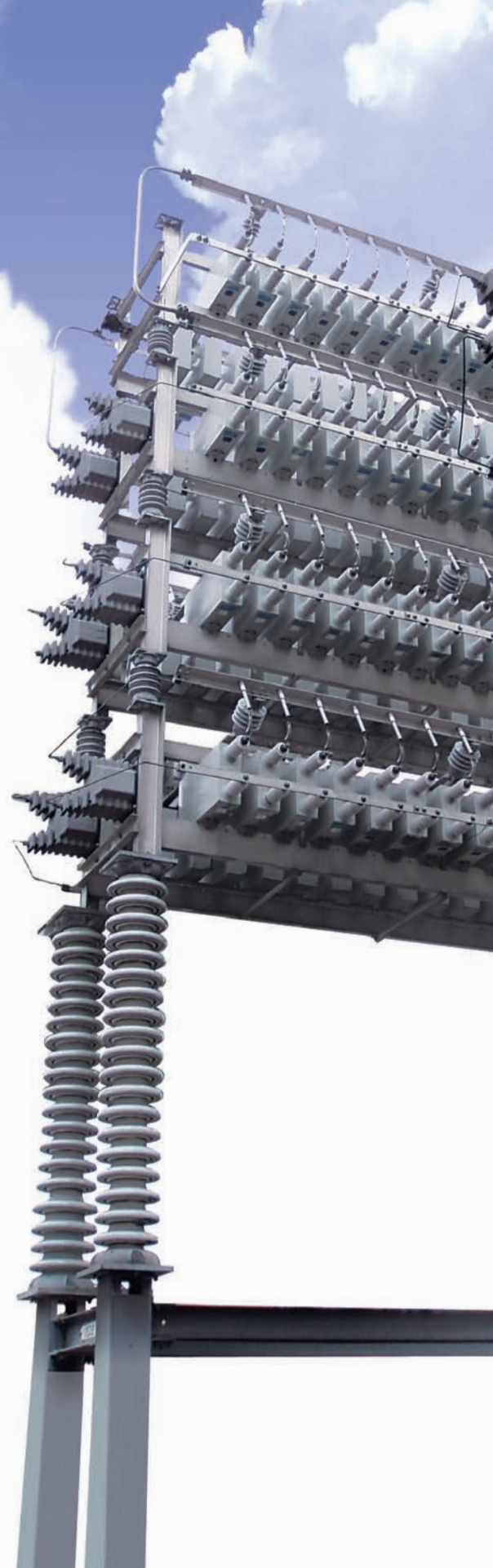
Now, there's a single universal product combining advanced **capacitor bank protection** with **automatic capacitor control**. The C70's superior protection elements provide sensitive protection with unprecedented unbalance compensation while the Automatic Voltage Regulator allows for intelligent automated cap bank control to minimize VAR consumption costs.



GE Multilin's C70 Capacitor Bank Protection and Control System is based on the well-established and proven UR platform



Multilin



Fundamentals of Adaptive Protection of Large Capacitor Banks

Bogdan Kasztenny
GE Multilin

Joe Schaefer
Florida Power & Light Company

Ed Clark
Florida Power & Light Company

1. Introduction

Shunt Capacitor Banks (SCB) are installed to provide capacitive reactive compensation and power factor correction. The use of SCBs has increased because they are relatively inexpensive, easy and quick to install, and can be deployed virtually anywhere in the grid. SCB installations have other beneficial effects on the system such as improvement of the voltage profile, better voltage regulation (if they were adequately designed), reduction of losses and reduction or postponement of investments in the transmission and generation capacity.

The role of SCBs increased recently in the light of blackout prevention activities, and increasing penetration of distributed generation, wind farms in particular, which add generation without addressing the problem of reactive power support. Moreover, capacitor banks are valuable assets that must be available for the daily demands of system operation and must provide reliable operation through abnormal power system scenarios.

From the protective relaying perspective, however, capacitor banks are historically considered a relatively low-volume market, and therefore, did not encourage development of advanced protective relays dedicated to capacitor banks. Quite often protection for SCBs is provided by general-purpose multi-function relays, with only a very few products on the market offering protection functions specifically tailored to capacitor bank protection. The utility relay engineer has generally needed to combine the functionality of multiple relays and customize their programming to provide the necessary protective system that will avoid false tripping for system disturbances and obtain the sensitivity for detecting capacitor CAN faults and minimizing damage.

The SCBs are assembled out of individual cans that are highly repairable. The need for advanced protection functions is particularly visible when SCBs are operated under conditions where one or more capacitor cans are temporarily removed but the bank is returned to service pending completion of repairs. However, continuous operation and repairs if needed can be done only if the bank is protected by a reliable and sensitive relay. This in turn, can be accomplished by deploying protection principles that are developed assuming an inherent unbalance in the protected bank.

Presently, in many custom applications or even dedicated capacitor bank protection products, compensation for inherent unbalance is based on subtracting historical values from the operating quantities, and thus making the relay respond to incremental, "delta" signals.

This paper will show that such simplified approaches are not optimal. Instead this paper derives technically accurate operating equations for capacitor bank protection that are derived assuming both inherent capacitor bank and system unbalance.

It is important that the relay is capable of dynamically compensating for unbalances between the power system phase voltages. These differences are constantly changing and may be on the order of 2 percent or more under normal conditions, and tens of percent during major system events such as close-in faults. The presented protection methods allow compensating simultaneously for the bank inherent unbalance and system unbalance increasing both sensitivity and security of protection.

The presented methods also facilitate auto-setting and self-tuning applications. Auto-setting is an operation of calculating new accurate relay constants to account for the inherent bank unbalances following the bank repair, and is performed in response to the user's request and under user supervision. Self-tuning is an operation of constantly self-adjusting the balancing constants in order to maintain optimum sensitivity of protection when the bank reactances change slowly in response to seasonal temperature variations and other conditions. The self-tuning applications require monitoring the total changes in the balancing constants in order to detect slow failure modes, and account for a series of small changes that do not trigger alarms on their own.

2. Capacitors

Protection engineering for shunt capacitor banks requires knowledge of the capabilities and limitations of the capacitor unit and associated electrical equipment including individual capacitor unit, bank switching devices, fuses, location and type of voltage and current instrument transformers.

A capacitor unit, Figure 1, is the building block of any SCB. The capacitor unit is made up of individual capacitor elements, arranged in parallel/series connected groups, within a steel enclosure. The internal discharge device is a resistor that reduces the unit residual voltage allowing switching the banks back after removing it from service. Capacitor units are available in a variety of voltage ratings (240V to 25kV) and sizes (2.5kVAr to about 1000kVAr).

The capacitor unit protection is based on the capacitor element failing in a shorted mode. A failure in the capacitor element dielectric causes the foils to weld together and short circuits the other capacitor elements connected in parallel in the same group, refer to Figure 1. The remaining series capacitor elements in the unit remain in service with a higher voltage across each of them and an increased capacitor can current. If a second element fails the process repeats itself resulting in an even higher voltage for the remaining elements.

There are generally four types of the capacitor unit designs to consider.

2.1 Externally Fused Capacitors

An individual fuse, externally mounted between the capacitor unit and the capacitor bank fuse bus, protects each capacitor unit. The capacitor unit can be designed for a relatively high voltage because the external fuse is capable of interrupting a high-voltage fault. However, the kilovar rating of the individual capacitor unit is usually smaller because a minimum number of parallel units are required to allow the bank to remain in service with a capacitor can out of service. A SCB using fused capacitors is configured using one or more series groups of parallel-connected capacitor units per phase, as shown in Figure 2.

2.2 Internally Fused Capacitors

Each capacitor element is fused inside the capacitor unit. A “simplified” fuse is a piece of wire sized to melt under the fault current, and encapsulated in a wrapper able to withstand the heat produced by the arc during the current interruption. Upon the capacitor failure, the fuse removes the affected element only. The other elements, connected in parallel in the same group, remain in service but with a slightly higher voltage across them.

Figure 3 illustrates a typical capacitor bank utilizing internally fused capacitor units. In general, banks employing internally

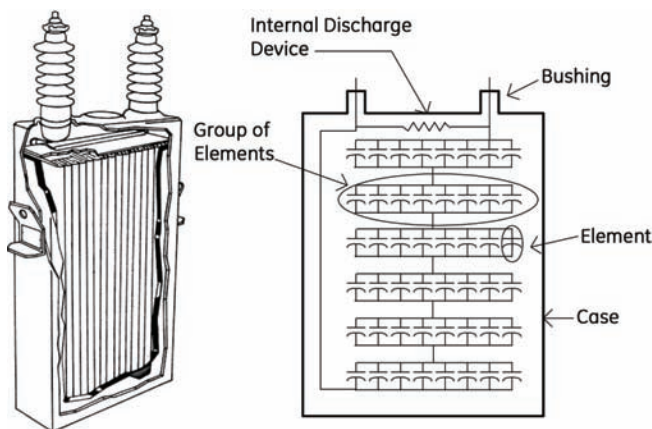


Figure 1. Capacitor unit.

fused capacitor units are configured with fewer capacitor units in parallel, and more series groups of units than are used in banks employing externally fused capacitor units. The capacitor units are built larger because the entire unit is not expected to fail.

2.3 Fuseless Capacitors

Fuseless Capacitor Bank designs are typically the most prevalent designs in modern day. The capacitor units for fuseless capacitor banks are connected in series strings between phase and neutral, as shown in Figure 4. The higher the voltage for the bank, the more capacitor elements in series.

The expected failure of the capacitor unit element is a short circuit, where the remaining capacitor elements will absorb the additional voltage. For example, if there are 6 capacitor units in series and each unit has 8 element groups in series there is a total of 48 element groups in the string. If one capacitor element fails, this element is shorted and the voltage across the remaining elements is 48/47 of the previous value, or about 2% higher. The capacitor bank remains in service; however, successive failures of elements would aggravate the problem and eventually lead to the removal of the bank.

The fuseless design is usually applied for applications at or above 34.5kV where each string has more than 10 elements in series to ensure the remaining elements do not exceed 110% rating if an element in the string shorts.

2.4 Unfused Capacitors

Contrary to the fuseless configuration, where the units are connected in series, the unfused shunt capacitor bank uses a series/parallel connection of the capacitor units. The unfused approach would normally be used on banks below 34.5kV, where series strings of capacitor units are not practical, or on higher voltage banks with modest parallel energy. This design does not require as many capacitor units in parallel as an externally fused bank.

3. Configurations of Shunt Capacitor Banks

Protection of shunt capacitor banks requires an understanding of the basics of capacitor bank design and capacitor unit

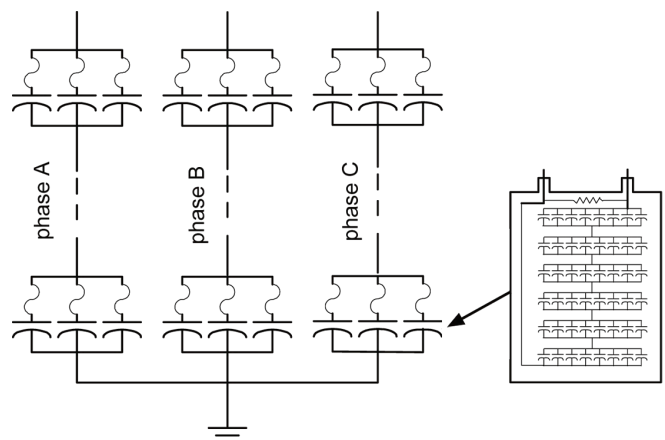


Figure 2. Externally fused shunt capacitor bank and capacitor unit.

connections. As a general rule, the minimum number of units connected in parallel is such that isolation of one capacitor unit in a group should not cause a voltage unbalance sufficient to place more than 110% of rated voltage on the remaining capacitors of the group. Equally, the minimum number of series connected groups is that in which the complete bypass of the group does not subject the other capacitors remaining in service to a permanent overvoltage of more than 110%. The value of 110% is the maximum continuous overvoltage capability of capacitor units as per IEEE Std 18-1992.

The maximum number of capacitor units that may be placed in parallel per group is governed by a different consideration. When a capacitor bank unit fails, other capacitors in the same parallel group contain some amount of charge. This charge will drain off as a high frequency transient current that flows through the failed capacitor unit. The capacitor can fuse holder, when used, and the failed capacitor unit must withstand this discharge transient.

The discharge transient from a large number of paralleled capacitors can be severe enough to rupture the failed capacitor unit or explode a fuse holder, which may damage adjacent units and even cause a major bus fault within the bank. To minimize the probability of failure of the explosion of the fuse holder, or rupture of the capacitor case, or both, the standards impose a limit to the total maximum energy stored in a parallel-connected group to 4650 kVAR. In order not to violate this limit, more capacitor groups of a lower voltage rating connected in series (with fewer units in parallel per group) may be a suitable solution. However, this may reduce sensitivity of applied unbalance detection schemes. Splitting the bank into two sections as a double wye may be the preferred solution, and may allow for better unbalance detection scheme.

Two prevalent designs of SCBs are the externally fused bank and the fuseless bank. There are advantages to each design.

Externally fused banks typically have a higher unbalance current when a unit fails which is used to operate a fused disconnect device. This design typically results in a simpler bank configuration and provides an easy method for field identification of a failed unit. A fused design also requires less sensitive unbalance protection since the fuse is the principal method used for isolating a can failure. However, this style of bank has a higher initial cost and usually higher maintenance costs. Since the fused element is exposed to the environment, the fuses become less reliable

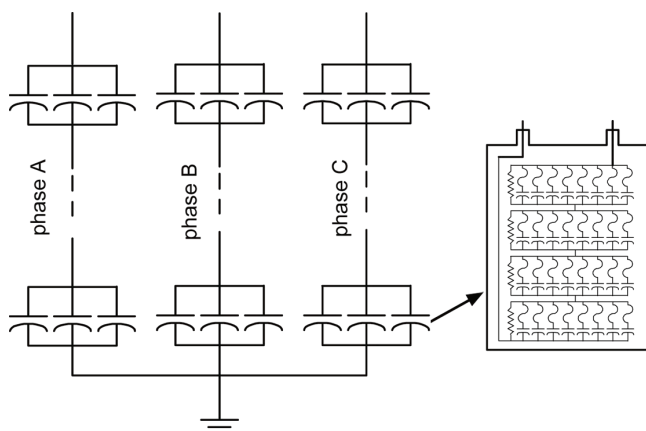


Figure 3.
Internally fused shunt capacitor bank and capacitor unit.

and require more maintenance to ensure correct operation. As a result, fuseless capacitor banks have become increasingly popular. Elimination of the fused connection results in a lower initial cost, reduced maintenance costs, smaller bank footprint, and fewer losses. Also, this bank design typically makes catastrophic can rupture less likely since the discharge energy of a failed element will be small.

However, the fuseless bank design has two main disadvantages that increase the emphasis on requiring sensitive relaying protection. One, the elimination of the external fuse means that visual indication of the failed capacitor has been lost. In addition, an element failure results in an overvoltage condition of the remaining elements, stressing them. Without a fuse as a means of isolating the failed can, the protective relay must now be sensitive enough to detect a failed element and alarm before additional elements fail causing a higher overvoltage condition on the remaining units. Because of these two factors, it is especially important to utilize a sensitive protective relay which can correctly isolate a bank for a failed element. Also, the use of faulted phase identification assists field personnel in locating a failed capacitor can without having to test the entire bank.

The optimum connection for a SCB depends on the best utilization of the available voltage ratings of capacitor units, fusing, and protective relaying. Virtually all HV and EHV banks are connected in one of the two wye configurations listed below [1,2]. Distribution capacitor banks, however, may be connected in wye or delta. Some banks may use an H configuration on each of the phases with a current transformer in the connecting branch to detect the unbalance.

3.1 Grounded Wye-Connected Banks

Grounded wye capacitor banks are composed of series and parallel-connected capacitor units per phase and provide a low impedance path to ground. This offers some protection from surge overvoltages and transient overcurrent conditions.

When a capacitor bank becomes too large, making the parallel energy of a series group too high for the capacitor units or fuses (above 4650kVAR), the bank may be split into two wye sections. The characteristics of the grounded double wye are similar to a grounded single wye bank. The two neutrals should be directly connected with a single path to ground.

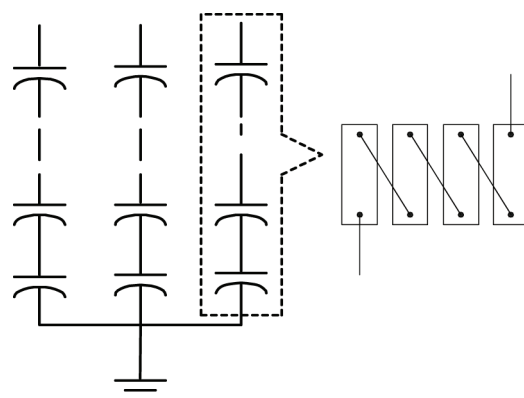


Figure 4.
Fuseless shunt capacitor bank and series string.

The double wye design facilitates better protection methods. Even with inherent unbalances the two banks will respond similarly to system events, and therefore, methods based on comparing one split-phase versus the other are more sensitive and less prone to system events (phase current balance technique, for example).

3.2 Ungrounded Wye-Connected Banks

Ungrounded wye banks do not permit zero sequence currents, third harmonic currents, or large capacitor discharge currents during system ground faults (phase-to-phase faults may still occur and will result in large discharge currents). Another advantage is that overvoltages appearing at the CT secondaries are not as high as in the case of grounded banks. However, the neutral should be insulated for full line voltage because it is momentarily at phase potential when the bank is switched or when one capacitor unit fails in a bank configured with a single group of units.

3.3 Delta-Connected Banks

Delta-connected banks are generally used only at distribution voltages and are configured with a single series group of capacitors rated at line-to-line voltage. With only one series group of units no overvoltage occurs across the remaining capacitor units from the isolation of a faulted capacitor unit.

3.4 H-Configuration

Some larger banks use an H configuration in each phase with a current transformer connected between the two legs to compare the current down each leg. As long as all capacitors are balanced, no current will flow through the current transformer. If a capacitor fuse operates, some current will flow through the current transformer. This bridge connection facilitates very sensitive protection. The H arrangement is used on large banks with many capacitor units in parallel.

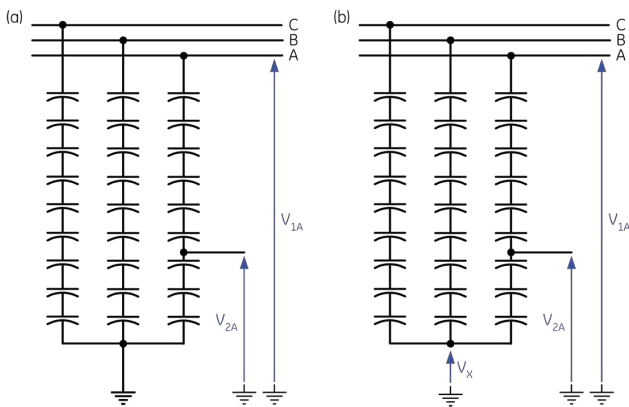


Figure 5.
Voltage differential application to grounded (a) and ungrounded (b) banks.

4. Sensitive Capacitor Bank Protection Methods

4.1 Voltage Differential (87V)

With reference to Figure 5, this function is based on a voltage divider principle – a healthy capacitor string has a constant and known division ratio between its full tap (typically the bus voltage) and an auxiliary tap used by the protection. The principle could be used on both grounded (Figure 5a) and ungrounded (Figure 5b) banks. In the latter case the neutral point voltage (V_x) must be measured by the relay, and used to derive the voltage across the string.

The function uses the following operating signal:

$$V_{OP(A)} = |V_{1A} - k_A \cdot V_{2A}| \quad \text{for grounded banks} \quad (1a)$$

$$V_{OP(A)} = |V_{1A} - k_A \cdot V_{2A} + V_x \cdot (k_A - 1)| \quad \text{for ungrounded banks} \quad (1b)$$

Where k_A is a division ratio for the A-phase of the bank.

Identical relations apply to phases B and C.

Note that equations (1) can be implemented using either phasors or magnitudes. During no-fault conditions and under small bank unbalances caused by internal bank failures, the two voltages will be almost in phase, suggesting the phasors and magnitude versions would yield similar results. However, the function is set very sensitive and given possible angular errors of the used VTs, there will be differences in performance between the two possible versions. The performance depends on the type of security measures used to deal with errors of instrument transformers. More information is provided in one of the following sections.

Typically, the method is used on grounded banks and equation (1a) is used. In theory, the algorithm could be applied on ungrounded banks using equation (1b), but it requires both the neutral voltage and the tap voltages to be measured. Such arrangements may not be practical (the tap voltages not measured on ungrounded banks). If the tap voltages are measured, one could apply multiple overlapping protection zones to the ungrounded bank as long as the applied relay(s) support the required number of inputs and associated protection functions. Specifically, equation (1b) can be used for voltage differential; and two neutral voltage unbalance protection elements can be used – one balancing the bus voltages with the neutral voltage, and another balancing the tap voltages against the neutral voltage.

Equations (1) apply to primary voltages, and as such they incorporate the voltage-dividing ratio of the capacitor, but ignore the ratios of applied instrument transformers. In secondary voltages, the operating voltage is:

$$V_{OP(A)} = |V_{1A} - k_A \cdot V_{2A}| \quad \text{for grounded banks} \quad (1c)$$

$$V_{OP(A)} = |V_{1A} - k_A \cdot V_{2A} + V_x \cdot (k_A - 1)| \quad \text{for ungrounded banks} \quad (1d)$$

Where the operating signal is in secondary volts of the bus VT, and the n_{VT1} , n_{VT2} and n_{VTX} stand for ratios of the bus, tap, and neutral voltage transformers, respectively.

Normally the VT ratios are selected so that the secondary voltages for the bus and tap voltages are similar under nominal system voltage. This leads to the effective matching factor for the secondary voltages being close to unity:

$$k_A \cdot \frac{n_{VT2}}{n_{VT1}} \approx 1 \quad (1e)$$

Voltage-based capacitor protection functions are set sensitive. Given the format of equations (1) both the bus and tap voltages shall be measured accurately in order to gain sensitivity of protection. As a result the VT ratios shall be selected so that the resultant secondary voltages fall in the region of maximum relay accuracy, and the two VTs work within their maximum class accuracy under nominal system voltage. The latter is ensured for the bus voltage; selection of the VT for the tap voltage shall be done carefully to minimize VT and relay errors for the tap voltage. Relay setting range for the ratio-matching factor is another condition that may limit selection of this VT ratio.

The following characteristics apply to the voltage differential function [3]:

- The element shall support individual per-phase settings to cope with different unbalances between the phases (repairs and shorted units).
- The element is capable of indicating the affected phase, and potentially the number of faulted capacitor elements, to aid troubleshooting and repairs of the bank.
- The function shall apply appropriate security measures for sensitive but secure operation: appropriate restraint signal could be developed to accompany the operating signal (1). Setting range shall allow disabling the restraint if desired so.
- Several independent pickup thresholds shall be provided for alarming and tripping.
- The voltage matching coefficients (k) shall be individually settable per phase.
- Both auto-setting and self-tuning applications of this method are possible. Provision could be made to calculate the matching factors k automatically under manual supervision of the user, either locally or remotely (auto-setting), or calculate the factor constantly in a slow adjusting loop (self-tuning).

The process of finding the constant balancing a given phase of protection is based on the following simple equation:

$$\hat{k}_A = \frac{V_{1A}}{V_{2A}} \quad (\text{under no-fault conditions}) \quad (2)$$

The voltage differential method can be used in a number of configurations as long as the relay allows wide range of ratio matching for the compared voltages: tap voltage can be compared with the bus voltage; two taps can be compared on the same bank; two taps can be compared between two parallel banks, etc.

4.2 Compensated Bank Neutral Voltage Unbalance (59NU)

With reference to Figure 6 this function is applicable to ungrounded banks, and is based on the Kirchhoff's currents law for the neutral node of the bank:

$$\frac{V_A - V_X}{Z_A} + \frac{V_B - V_X}{Z_B} + \frac{V_C - V_X}{Z_C} = 0 \quad (3a)$$

The above expression can be rearranged as follows:

$$-V_X \cdot \left(\frac{1}{Z_A} + \frac{1}{Z_B} + \frac{1}{Z_C} \right) + \frac{V_A}{Z_A} + \frac{V_B}{Z_B} + \frac{V_C}{Z_C} = 0 \quad (3b)$$

and further to an equivalent form of:

$$-V_X \cdot \left(\frac{1}{Z_A} + \frac{1}{Z_B} + \frac{1}{Z_C} \right) + \frac{V_A}{Z_A} + \frac{V_B}{Z_A} + \frac{V_C}{Z_A} + \frac{V_B}{Z_B} - \frac{V_B}{Z_A} + \frac{V_C}{Z_C} - \frac{V_C}{Z_A} = 0 \quad (3c)$$

which is identical with:

$$-V_X \cdot \left(\frac{1}{Z_A} + \frac{1}{Z_B} + \frac{1}{Z_C} \right) + \frac{1}{Z_A} \cdot (V_A + V_B + V_C) + V_B \cdot \left(\frac{1}{Z_B} - \frac{1}{Z_A} \right) + V_C \cdot \left(\frac{1}{Z_C} - \frac{1}{Z_A} \right) = 0 \quad (3d)$$

Multiplying both sides by $3 \cdot V_0$ and substituting the sum of the phase voltages by $3 \cdot V_0$

yields:

$$V_X \cdot \left(1 + \frac{Z_A}{Z_B} + \frac{Z_A}{Z_C} \right) - 3 \cdot V_0 + V_B \cdot \left(1 - \frac{Z_A}{Z_B} \right) + V_C \cdot \left(1 - \frac{Z_A}{Z_C} \right) = 0 \quad (3e)$$

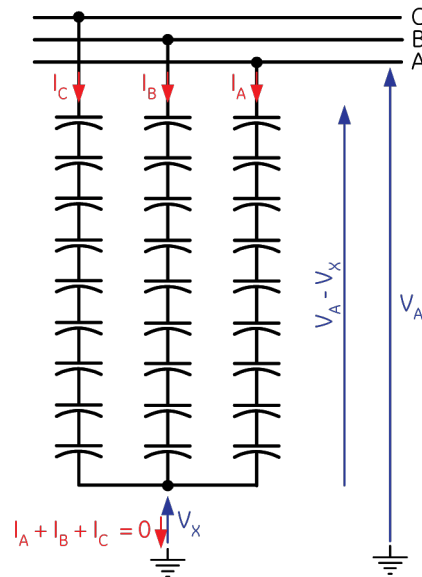


Figure 6. Compensated bank neutral overvoltage application.

Introducing the following matching k -values to reflect the inherent bank unbalance:

$$k_{AB} = \frac{Z_A}{Z_B} \approx \frac{X_A}{X_B}, \quad k_{AC} = \frac{Z_A}{Z_C} \approx \frac{X_A}{X_C} \quad (4)$$

allows re-writing the balance equation (3e) into the following operating signal:

$$V_{OP} = \frac{1}{3} \left| (1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC}) \right| \quad (5)$$

Equation (5) involves phasors, not magnitudes, i.e. the vectorial sum of the voltages is created by the protection function implementing the method.

Note that the ratios of the capacitor impedances between phase A and the two other phases are close to unity, and therefore the correcting factors for the B and C-phase voltages are small numbers, while the coefficient in front of the V_x voltage is close to 3.

Equation (5) while following relations (4) is a proper neutral overvoltage function compensated for both the system unbalance (V_0), and the bank unbalance (k_{AB} , k_{AC}). To understand it better assume the bank is perfectly balanced ($k_{AB} = 1$, $k_{AC} = 1$). If so, the precise operating equation takes a familiar simplified form [1]:

$$V_{OP} = |V_x - V_0| \quad (6)$$

Equation (5) identifies the source of the inherent bank unbalance, and therefore allows for proper compensation. In addition, this key equation allows analyzing the impact of imperfect compensation and/or errors of instrument transformers on sensitivity of protection as explained later in this paper.

Equation (5) can be implemented using either derived neutral component in the bus voltages (vectorial sum of the phase voltages calculated by the relay), or directly measured neutral voltage component (open-delta VT voltage). Slightly different errors would occur in these two approaches.

When deriving the $3 \cdot V_0$ internally the relay is presented with near-nominal voltages under internal failures that require high protection sensitivity, typically has maximum accuracy of voltage measurement under such conditions, and calculates the vectorial voltage sum with relatively high accuracy.

When measuring the $3 \cdot V_0$ directly the relay is presented with a very small signal under internal failures that require high protection sensitivity. In order to keep high accuracy a high-sensitivity voltage relay input shall be used. At the same time, this voltage could reach as high as system nominal voltage during external faults. Therefore, the input range shall be high enough to measure this voltage correctly and balance it accurately against the V_x signal.

The V_x voltage, in turn, is relatively small under internal failures that require high protection sensitivity. Therefore either the relay shall be equipped with a high-sensitivity voltage input, or the VT ratio is selected to create this signal and improve measuring accuracy of this signal, or both. In any case, the ratio must be selected such as the input voltage does not exceed the conversion range of a given relay. Sometimes this requirement may be relaxed allowing

saturation of the relay input – the function shall be blocked in this case under external faults either by time delay or explicit logic in order to cope with the spurious unbalance caused by saturation of the V_x measurement. In any case, one shall observe the thermal withstand rating of the relay input when selecting relatively low-ratio VT for the measurement of the V_x signal.

When written for secondary voltages the key operating equation becomes:

- When measuring the $3 \cdot V_0$ internally and expressing the operating signal in secondary volts of the bus voltage:

$$V_{OP} = \frac{1}{3} \left| \frac{n_{VTX}}{n_{VT}} (1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC}) \right| \quad (7a)$$

- When measuring the $3 \cdot V_0$ from an open-delta VT and expressing the operating signal in secondary volts of the bus voltage:

$$V_{OP} = \frac{1}{3} \left| \frac{n_{VTX}}{n_{VT}} (1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot \frac{n_{VT0}}{n_{VT}} V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC}) \right| \quad (7b)$$

The following characteristics apply to the compensated bank neutral voltage unbalance function [3]:

- The single element function does not indicate explicitly the effected phase. It could, however, aid troubleshooting and repairs by reporting the k -factors (pre-fault and fault values).
- The function shall apply appropriate security measures for sensitive but secure operation: appropriate restraint signal could be used with the operating signal (5). Disabling the restraint should be allowed if desired so.
- Several independent pickup thresholds shall be provided for alarming and tripping.
- The inherent bank unbalance constants (k -values) shall be settable.
- Both auto-setting and self-tuning applications are possible as long as the neutral point voltage is non-zero and is measured with adequate accuracy. Provision could be made to calculate factors k automatically under manual supervision of the user, either locally or remotely (auto-setting), or continuously in a slow adjusting loop (self-tuning).

$$\text{Re} \left\{ (1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC}) \right\} = 0 \quad (8a)$$

$$\text{Im} \left\{ (1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC}) \right\} = 0 \quad (8b)$$

The process of finding the two unknown constants is based on the following principle. When the bank is healthy, equation (5) is perfectly balanced, and therefore it can be zeroed out. Writing the real and imaginary parts of the equation separately one obtains two equations for two unknowns.

The above is now solved for the two unknowns k_{AB} and k_{AC} while treating the involved voltages as knowns (the k -values are treated as real numbers per equations (4)). The method works as long as the V_x voltage is above the measuring error level. The procedure does not call for the system to be unbalanced (V_o can be zero) as the unknowns (k) do not appear as multipliers for the V_o value in equations (8).

4.3. Phase Current Balance (60P)

With reference to Figure 7, this function is based on the balance between phase currents of the two parallel banks, and is applicable to both grounded and ungrounded arrangements. Higher sensitivity can be achieved when using a window CT (compared with the two individual CTs summated electrically). With the two banks slightly different, a circulating current flows, and shall be compensated for in order to increase sensitivity of the function. This protection element is founded on the following theory.

Both parallel banks work under identical voltage, and therefore:

$$I_{DIF(A)} = V_{BANK(A)} \frac{Z_{1A} - Z_{2A}}{Z_{1A} \cdot Z_{2A}} \quad (9a)$$

$$I_A = V_{BANK(A)} \frac{Z_{1A} + Z_{2A}}{Z_{1A} \cdot Z_{2A}} \quad (9b)$$

Utilizing the fact the voltage is the same in expressions (9a) and (9b) one writes:

$$V_{BANK(A)} = I_{DIF(A)} \cdot \frac{Z_{1A} \cdot Z_{2A}}{Z_{1A} - Z_{2A}} = I_A \cdot \frac{Z_{1A} \cdot Z_{2A}}{Z_{1A} + Z_{2A}} \quad (9c)$$

creating the following balance equation:

$$I_{DIF(A)} \frac{Z_{1A} \cdot Z_{2A}}{Z_{1A} - Z_{2A}} - I_A \frac{Z_{1A} \cdot Z_{2A}}{Z_{1A} + Z_{2A}} = 0 \quad (9d)$$

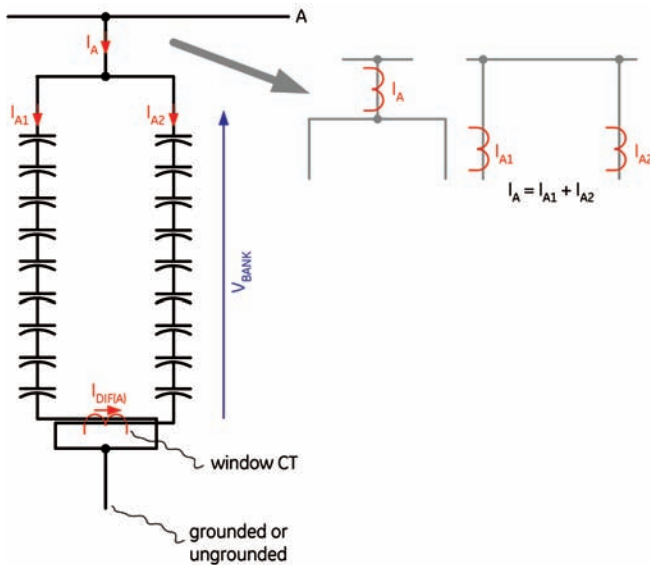


Figure 7. Phase current balance application.

Dividing both sides by the coefficient next to the differential current gives:

$$I_{DIF(A)} - I_A \frac{Z_{1A} - Z_{2A}}{Z_{1A} + Z_{2A}} = 0 \quad (9e)$$

Introducing the inherent unbalance compensating factor, k :

$$k_A = \frac{Z_{1A} - Z_{2A}}{Z_{1A} + Z_{2A}} \approx \frac{X_{1A} - X_{2A}}{X_{1A} + X_{2A}} \quad (10)$$

yields the following operating signal of the phase current balance protection:

$$I_{OP(A)} = \left| I_{DIF(A)} - k_A \cdot I_A \right| \quad (11)$$

Identical relations apply to phases B and C.

The operating signal (11) implements proper compensation for the inherent unbalance of the bank. The equation identifies that the error is proportional to the amount of the total phase current (I_A) and the difference between the impedances of the two banks (k_A). When not compensated, the straight differential current would display a non-zero value "leaking" from the phase current. Subtracting the historical value of such leakage current, often applied today, improves sensitivity but it is not a correct way of compensating this functions. More discussion follows in section 5 of this paper.

Note that equation (11) is a vectorial difference between the two signals. However, as the k -factor is a real number (very small or zero imaginary part), the two currents are in phase and their magnitudes, not phasors, could be used as well.

Typically CTs used to measure the total phase current and the differential current would have drastically different ratios. The differential CT might have much lower ratio in order to increase magnitude of the secondary current under internal bank failures requiring high sensitivity of protection. During external fault conditions, the differential current remains low further promoting the usage of low-ratio CT. On the relay side, a sensitive ground current input shall be used for better sensitivity and accuracy.

When written in secondary terms, the key equation (11) when expressed in secondary amperes of the differential CT becomes:

$$I_{OP(A)} = \left| I_{DIF(A)} - k_A \cdot \frac{n_{CT}}{n_{CT DIF}} \cdot I_A \right| \quad (12)$$

The following characteristics apply to the phase current balance function [3]:

- The element shall support individual per-phase settings.
- The function indicates the effected phase, as well as reports the change in the current division ratio, k (pre-fault and fault values) to aid troubleshooting and repairs of the bank.
- The element shall apply appropriate security measures for sensitive but secure operation: appropriate restraint signal could be provided to accompany the operating signal (11). Disabling the restraint shall be possible if desired so.

- Several independent thresholds shall be provided per phase for alarming and tripping.
- The current dividers (k) are individually set per phase.
- Both auto-setting and self-tuning applications of this method are possible. Provision could be made to calculate factors k automatically under manual supervision of the user, either locally or remotely (auto-setting), or constantly in a slow adjusting loop (self-setting).

The process of finding the balancing constants for each phase of protection is based on the following simple equation:

$$\hat{k}_A = \frac{I_{DIF(A)}}{I_A} \quad (\text{under no-fault conditions}) \quad (13)$$

4.4 Neutral Current Balance (60N)

With reference to Figure 8, this function is based on the balance between interconnected neutral currents of two parallel banks, and is applicable to both grounded and ungrounded installations. A window CT measuring the vectorial difference between the two neutral currents allows for better accuracy/sensitivity.

With the two banks possibly slightly different, a circulating zero-sequence current may be present and shall be compensated for in order to increase sensitivity of the function.

Proper inherent unbalance compensation is founded on the following theory.

Both parallel banks work under identical voltages, therefore their phase currents are driven by the individual admittances in each phase of each bank:

$$I_{A1} = (V_A - V_X) \cdot Y_{A1}; \quad I_{A2} = (V_A - V_X) \cdot Y_{A2} \quad (14a)$$

$$I_{B1} = (V_B - V_X) \cdot Y_{B1}; \quad I_{B2} = (V_B - V_X) \cdot Y_{B2} \quad (14b)$$

$$I_{C1} = (V_C - V_X) \cdot Y_{C1}; \quad I_{C2} = (V_C - V_X) \cdot Y_{C2} \quad (14c)$$

The sum of the two neutral currents can be derived from the above equations:

$$I_{N1} = I_{A1} + I_{B1} + I_{C1} = (V_A - V_X) \cdot Y_{A1} + (V_B - V_X) \cdot Y_{B1} + (V_C - V_X) \cdot Y_{C1} \quad (14d)$$

$$I_{N2} = I_{A2} + I_{B2} + I_{C2} = (V_A - V_X) \cdot Y_{A2} + (V_B - V_X) \cdot Y_{B2} + (V_C - V_X) \cdot Y_{C2} \quad (14e)$$

The differential current is a vectorial difference between the two currents. By subtracting (14e) from (14d) one obtains:

$$I_{DIF} = I_{N1} - I_{N2} = (V_A - V_X) \cdot (Y_{A1} - Y_{A2}) + (V_B - V_X) \cdot (Y_{B1} - Y_{B2}) + (V_C - V_X) \cdot (Y_{C1} - Y_{C2}) \quad (14f)$$

At the same time the total currents in each phase are driven by the total admittance of the two banks in each phase:

$$I_A = I_{A1} + I_{A2} = (V_A - V_X) \cdot (Y_{A1} + Y_{A2}) \quad (15a)$$

$$I_B = I_{B1} + I_{B2} = (V_B - V_X) \cdot (Y_{B1} + Y_{B2}) \quad (15b)$$

$$I_C = I_{C1} + I_{C2} = (V_C - V_X) \cdot (Y_{C1} + Y_{C2}) \quad (15c)$$

Inserting equations (15) into equations (14) allows eliminating the voltages and derive the all-current balance equation for the two banks:

$$I_{DIF} = I_A \cdot \frac{Y_{A1} - Y_{A2}}{Y_{A1} + Y_{A2}} + I_B \cdot \frac{Y_{B1} - Y_{B2}}{Y_{B1} + Y_{B2}} + I_C \cdot \frac{Y_{C1} - Y_{C2}}{Y_{C1} + Y_{C2}} \quad (16)$$

Labeling:

$$k_A = \frac{Y_{A1} - Y_{A2}}{Y_{A1} + Y_{A2}}; \quad k_B = \frac{Y_{B1} - Y_{B2}}{Y_{B1} + Y_{B2}}; \quad k_C = \frac{Y_{C1} - Y_{C2}}{Y_{C1} + Y_{C2}} \quad (17)$$

One gets the following operating equation balancing the protected bank:

$$I_{OP} = |I_{DIF} - (k_A \cdot I_A + k_B \cdot I_B + k_C \cdot I_C)| \quad (18)$$

When the banks are identical, i.e. phases A are equal, phases B are equal and phases C are equal, the operating equation (18) simplifies to a straight overcurrent condition for the measured neutral differential current.

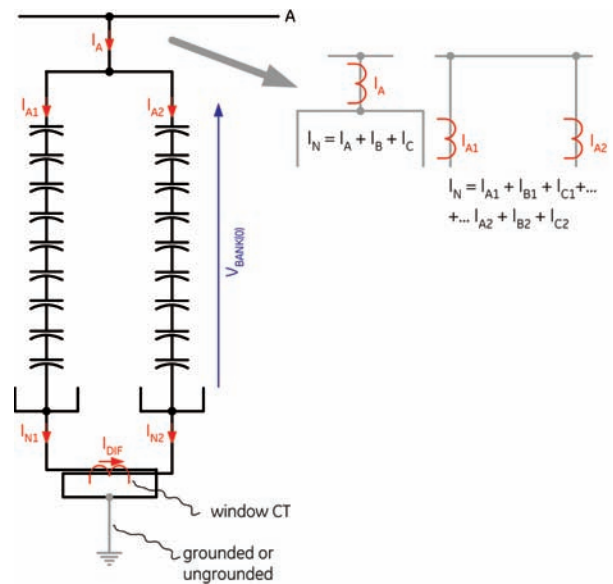


Figure 8.
Neutral current balance application.

It is justified to assume the balancing constants, k , are real numbers. Still, this leaves the balance equation (18) with 3 unknowns. These unknowns can be calculated based on several measurements taken under unbalanced conditions.

Alternatively, equation (18) may be re-written from phase coordinates, into sequence components:

$$I_{OP} = \left| I_{DIF} - (k_0 \cdot I_0 + k_1 \cdot I_1 + k_2 \cdot I_2) \right| \quad (19)$$

It is justified to assume that the positive-sequence current would leak into the operating quantity more considerably compared with the zero and negative-sequence components. Therefore only the positive-sequence leakage can be eliminated to improve sensitivity. This approach yields a slightly simplified form of the mathematically accurate equations (18) and (19):

$$I_{OP} = \left| I_{DIF} - k_1 \cdot I_1 \right| \quad (20)$$

With one unknown balancing factor (k_1) the auto-setting or self-tuning procedures can be implemented simply as:

$$I_{OP} = \left| I_{DIF} - k_1 \cdot I_1 \right| \quad (\text{under no-fault conditions}) \quad (21)$$

Unlike in previous methods, this compensating coefficient may be a complex number.

Operating signal (18) or (19) implements proper compensation for the inherent unbalance of the bank. Equation (20) is a good practical approximation.

Equation (18) holds for primary currents, when applied to secondary amperes, it takes the following form:

$$I_{OP} = \left| I_{DIF} - \frac{n_{CT}}{n_{CT DIF}} \cdot (k_A \cdot I_A + k_B \cdot I_B + k_C \cdot I_C) \right| \quad (22)$$

Typically the differential CT would be of lower ratio in order to increase the level of the secondary current for internal failures that call for increased sensitivity of protection. During external faults, the differential current will be increased but not dramatically.

The following characteristics apply to the neutral current balance function [3]:

- The single element function does not indicate explicitly the effected phase.
- The function shall apply appropriate security measures for sensitive but secure operation (provision for a restraint signal).
- Several independent thresholds shall be provided that can be freely used for alarming and tripping.
- The positive-sequence compensating factor k_1 shall be a setting.
- Provision could be made to calculate the k -factor automatically under manual supervision of the user, either locally or remotely (auto-setting), or continuously in a slow adjusting loop (self-tuning).

5. Sensitivity to Internal Bank Failures

The key equations defining the outlined capacitor bank protection methods ((1), (5), (11) and (18)) allow not only proper compensation for the inherent bank unbalance, but also facilitate analysis of sensitivity of protection.

Each of the four methods as described in this paper is founded on a balance equation that assumes:

First, that the bank is intact in terms of experiencing a ground or phase fault.

Second, that the inherent unbalance between the capacitor phases does not change.

A ground or phase fault violating the first assumption results in severe unbalance in the operating equations, and leads to protection operation as expected. This aspect of operation is backed-up by overcurrent protection, and therefore is of secondary importance.

A short or open in a single or several cans violates the second assumption, causes a minor unbalance in the operating equations, and results in operation of protection set sensitive enough given the size of the internal failure.

This latter way of responding to internal failures is critical for analysis of protection sensitivity. For this purpose one could assume nominal system voltages and resulting currents, and use the operating equations to determine the amount of the operating signals in response to any given unbalance in the bank.

5.1 Sensitivity of the Voltage Differential Function

For simplicity let us focus on the application to grounded banks. Neglecting the phase index, the operating signal in this method is (equation (1a):

$$V_{OP} = \left| V_1 - k_{SET} \cdot V_2 \right|$$

The actual voltage-dividing ratio during internal failures of the bank is:

$$k_{FAIL} = \frac{Z_{BUS-TAP} + Z_{TAP-GND}}{Z_{TAP-GND}} = 1 + \frac{Z_{BUS-TAP}}{Z_{TAP-GND}} = 1 + \frac{C_{TAP-GND}}{C_{BUS-TAP}} \quad (23a)$$

The tap voltage during the failure is:

$$V_2 = V_1 \cdot \frac{1}{k_{FAIL}} \quad (23b)$$

and the operating signal becomes:

$$V_{OP} = \left| V_1 \right| \cdot \left| 1 - \frac{k_{SET}}{k_{FAIL}} \right| \quad (23c)$$

As a percentage of the full bus voltage the operating signal is:

$$\frac{V_{OP}}{|V_1|} = \left| 1 - \frac{k_{SET}}{k_{FAIL}} \right| \cdot 100\% \quad (24d)$$

Equation (24d) yields a proportional relationship between k_{FAIL} and the operating voltage: a change by 1% in the k -value, yields an extra 1% of nominal in the operating signal.

What is more interesting, however, is the relation between changes in the bus-tap and tap-ground capacitances and the increase in the operating voltage. Given equation (23a) one can write:

$$\Delta V_{OP\%} = \Delta k_{FAIL\%} = \Delta C_{BUS-TAP\%} = \Delta C_{TAP-GND\%} \quad (25)$$

The above signifies that a 1% change in either of the bus-to-tap or tap-to-ground capacitances would yield 1% of bus nominal in the operating voltage.

Depending on the serial/parallel arrangement of the cans, it will take a certain amount of shorted/opened cans to cause a single percentage change in the capacitance and an equivalent increase in the operating voltage. The final assessment of sensitivity has to take into account the actual arrangement of the capacitor bank.

An interesting question is the optimum location of the tap. Regardless of the number of parallel cans, the longer the string, the higher the impedance. If so a single can failure would cause a smaller percentage change in the overall impedance/capacitance. For best sensitivity both the portions (bus-tap and tap-ground) shall be kept as short as possible as measured in the number of cans. In reality, the number of cans is not a variable. Within this restriction, half of the total length is the smallest possible length.

Therefore the exact middle position of the tap is optimum from the point of view of sensitivity. Under the mid-tap both the portions (bus-tap and tap-ground) are protected with the same sensitivity measured in the number of cans.

Often, the tap is installed below the mid-point in order to apply lower voltage VTs. This creates a classical trade-off between optimum performance and low cost of installation.

5.2 Sensitivity of the Compensated Bank Neutral Voltage Unbalance Function

The analysis shall start with the full operating equation (5):

$$V_{OP} = \frac{1}{3} \left| (1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC}) \right|$$

in which the following assumptions can be made:

- The $1-k$ terms can be neglected for simplicity.
- The system zero-sequence voltage can be considered zero (the system is practically always strong enough to maintain the balance at the bus despite few cans affected within the bank itself).

This leads to the following relationship:

$$V_{OP} = \frac{1}{3} \left| (1 + k_{AB} + k_{AC}) \cdot V_x \right| \quad (26a)$$

As both the k -values are close to unity, the above simplifies to:

$$V_{OP} \approx |V_x| \quad (26b)$$

Equation (3e) helps calculating the amount of the neutral point voltage. Assuming system zero-sequence voltage nil, the equation can be re-arranged to calculate the value of V_x :

$$|V_x| = \left| \frac{V_B(1 - k_{AB}) + V_C(1 - k_{AC})}{1 + k_{AB} + k_{AC}} \right| \quad (27a)$$

Assuming a balanced bus voltage:

$$V_B = a^2 \cdot V_A, \quad V_C = a \cdot V_A, \quad a = 1 \angle 120^\circ \quad (27b)$$

One simplifies further:

$$|V_x| = |V_A| \cdot \left| \frac{a^2 \cdot (1 - k_{AB}) + a \cdot (1 - k_{AC})}{1 + k_{AB} + k_{AC}} \right| \quad (27c)$$

Observing the k -values are real numbers close to unity and using properties of the a -operand yields the following:

$$\frac{|V_x|}{|V_A|} = \left| \frac{1 - \frac{1}{2}(k_{AB} + k_{AC}) + j \frac{\sqrt{3}}{2}(k_{AC} - k_{AB})}{1 + k_{AB} + k_{AC}} \right| \quad (27d)$$

Because the actual operating equation (5) compensates for the inherent bank unbalance, it is further justified to assume the ratios of the impedances to be a perfect unity (say k_{AB}), and treat the other ratio as a variable (k_{AC} correspondingly):

$$\frac{|V_x|}{|V_A|} = \left| \frac{\frac{1}{2} - j \frac{\sqrt{3}}{2} - \frac{1}{2}k + j \frac{\sqrt{3}}{2}k}{2 + k} \right| = \left| \frac{k - 1}{2 + k} \right| \quad (27e)$$

The above equations means that only 1/3rd of the percentage change in the ratio of impedances between any two phases will be seen as a percentage of nominal bus voltage:

$$\Delta V_{OP\%} = \frac{1}{3} \Delta k_{\%} = \frac{1}{3} \Delta C_{\%} \quad (28)$$

For example it will take 3% in the drop of the phase A impedance, to see 1% of bus nominal voltage as the V_x signal, and thus the operating signal of the function.

The operating signal has an arbitrary factor 1/3rd to comply with the common understanding of this method (equation (6)). Using microprocessor-based relay technology this scaling is not important as any scaling can be handled accurately. What is important is the 1:3 ratio between the measured neutral point voltage and changes in the capacitor impedance.

This reinforces using low-ratio VTs for measuring the neutral-point voltage.

Relation (28) can also be used to calculate the required ratio. For example, assuming target sensitivity for the function, one calculates the effective operating signal as percentage of the bus voltage. Using relay accuracy claim, one determines the minimum secondary voltage that is required for the proper operation of the relay. Combining the two requirements allows calculating the ratio for the VT:

$$n_{VTX} = \frac{\Delta C_{\%} \cdot V_{BUS}}{3 \cdot \sqrt{3} \cdot V_{SEC(MIN)}} \quad (29)$$

For example, with the target sensitivity of 1% of impedance change on a 345kV bus, and the minimum relay voltage of 0.5V secondary, the maximum VT ratio is:

$$n_{VTX} = \frac{0.01 \cdot 345kV}{3 \cdot \sqrt{3} \cdot 0.5V} = 1328$$

With this ratio, under SLG fault on the bus, the secondary voltage would be 150V. This is well within the range of modern relays. Assuming a relay conversion range of 260VRMS, the ratio can be lowered to $1328 \cdot 150 / 260 = 766$, yielding the operating signal of 0.87V secondary at 1% change in the capacitor impedance.

5.3 Sensitivity of the phase current balance function

Neglecting the phase index, the operating signal of this method is (equation (11)):

$$I_{OP} = |I_{DIF} - k_{SET} \cdot I|$$

It is justified to assume the total capacitor current does not change in response to the internal failure of limited size, therefore the operating current as a percentage of the total capacitor current equals the percentage change in the k -value:

$$\frac{\Delta I_{OP}}{I} = \frac{1}{100} \Delta k_{\%} \quad (30a)$$

For example, 1% of change in the k -factor yields 1% of the full current as measured by the split-phase CT.

Next step is to understand the impact of impedance/capacitance changes on the changes in the k -factor. From equation (10):

$$k = \frac{X_1 - X_2}{X_1 + X_2}$$

Observing that the two reactances are very similar, one obtains:

$$\Delta k_{\%} = \frac{1}{2} \Delta X_{\%} = \frac{1}{2} \Delta C_{\%} \quad (30b)$$

Equations (30) mean that for each % of change in the impedance/capacitance of one of the parallel banks, there will be increase in the differential current by 0.5% of the total bank current.

Again, the above observation may be used to select the ratio of the split-phase CT: the target accuracy allows calculating the minimum primary operating signal; the minimum relay sensitivity allows determining the minimum accurately measured secondary signal; the ratio dictates the maximum CT ratio that can be applied in this case:

$$n_{DIF} = \frac{\Delta C_{\%} \cdot I_{NOM}}{2 \cdot I_{SEC(MIN)}} \quad (31)$$

5.4 Sensitivity of the Neutral Current Balance

It is worth noticing that this method is a derivative of the phase current balance approach (60P), and as such it has identical sensitivity.

The balance equations for all three phases per the 60P protection principle are:

$$I_{DIF(A)} - I_A \frac{Z_{1A} - Z_{2A}}{Z_{1A} + Z_{2A}} = 0 \quad (32a)$$

$$I_{DIF(B)} - I_B \frac{Z_{1B} - Z_{2B}}{Z_{1B} + Z_{2B}} = 0 \quad (32b)$$

$$I_{DIF(C)} - I_C \frac{Z_{1C} - Z_{2C}}{Z_{1C} + Z_{2C}} = 0 \quad (32c)$$

Observing that in the 60P method:

$$I_{DIF(A)} = I_{A1} - I_{A2}, \quad I_{DIF(B)} = I_{B1} - I_{B2}, \quad I_{DIF(C)} = I_{C1} - I_{C2} \quad (33a)$$

While in the 60N method:

$$\begin{aligned} I_{DIF} &= I_{N1} - I_{N2} = (I_{A1} + I_{B1} + I_{C1}) - (I_{A2} + I_{B2} + I_{C2}) = \dots \\ &\dots = (I_{A1} - I_{A2}) + (I_{B1} - I_{B2}) + (I_{C1} - I_{C2}) \end{aligned} \quad (33b)$$

allows one to insert (33a) into (33b) and obtain:

$$I_{DIF} = I_{DIF(A)} + I_{DIF(B)} + I_{DIF(C)} \quad (33c)$$

Now inserting (32a-c) into (33c) yields:

$$I_{DIF} = I_A \frac{Z_{1A} - Z_{2A}}{Z_{1A} + Z_{2A}} + I_B \frac{Z_{1B} - Z_{2B}}{Z_{1B} + Z_{2B}} + I_C \frac{Z_{1C} - Z_{2C}}{Z_{1C} + Z_{2C}} \quad (34a)$$

Observing the relation between the impedance and admittance one can re-write the above into:

$$I_{DIF} - I_A \frac{Y_{1A} - Y_{2A}}{Y_{1A} + Y_{2A}} - I_B \frac{Y_{1B} - Y_{2B}}{Y_{1B} + Y_{2B}} - I_C \frac{Y_{1C} - Y_{2C}}{Y_{1C} + Y_{2C}} = 0 \quad (34b)$$

Which is precisely the 60N balance equation as derived in section 4.4 (equation (18)).

The above proves, that neglecting CT and relay accuracy the 60P and 60N functions have identical sensitivity. Specifically, per each percent of change in the impedance/capacitance of one of the banks, the differential CT would see an increase of 0.5% of the total bank current.

The phase variant of the method (60P) is easier to compensate for the inherent bank unbalance. The neutral variant of the method (60N) requires 1 CT and relay input, compared with 3 sets for the phase version (60P). If applied concurrently on one relay, the two functions may be treated as partially redundant using different CTs and relay inputs.

6. Sensitivity to Instrumentation Errors

This section analyses impact of finite accuracy of Instrument Transformers (ITs) and the relay on the four protection methods.

It is important to notice that errors of instrument transformers and the relay can be accounted for when tuning the coefficients. If the tuning coefficients (k) are implemented as real numbers, the magnitude errors can be eliminated, and the impact of angular errors could be reduced. If the coefficients are implemented as complex numbers, both magnitude and angle errors can be accounted for.

However, the IT and relay errors will slightly change with the magnitude of the signal and /or other factors such as residual flux or temperature. Even if tuned at one particular operating point, the method will show some errors at different operating point due to the IT and relay inaccuracies. It is important to realize, though, that these errors occur regardless of the protection principle. By compensating for bank inherent unbalance, and partially for IT and relay errors, the methods presented in this paper are already less susceptible to instrumentation errors. Detailed analysis follows.

Magnitude and angle errors of ITs and the relay can be modeled as a complex multiplier applied for the analysis purposes to the ideal transformation ratio of a given signal. For example, a negative 0.5% magnitude error combined with a 0.3 deg angle error can be modeled as:

$$n_{ACTUAL} = n_{IDEAL} \cdot b, \quad b = (1 - 0.005) \angle 0.3^\circ$$

6.1 Impact of Instrumentation Errors on the Voltage Differential Function

For simplicity consider applications on grounded banks. The operating signal in secondary volts is (equation (1c)):

$$V_{OP(A)} = \left| V_{1A} - k_A \cdot \frac{n_{VT2}}{n_{VT1}} \cdot V_{2A} \right|$$

Now assume that the equation was perfectly balanced making the operating signal above a perfect zero, but one of the VTs, say the tap VT (#2), works with an error of b . If so, the operating signal becomes non-zero:

$$V_{OP(A)} = \left| V_{1A} - k_A \cdot b \cdot \frac{n_{VT2}}{n_{VT1}} \cdot V_{2A} \right| \quad (35a)$$

Assuming a perfect balance, equation (1c) can be solved for the tap voltage:

$$0 = \left| V_{1A} - k_A \cdot \frac{n_{VT2}}{n_{VT1}} \cdot V_{2A} \right| \rightarrow k_A \cdot \frac{n_{VT2}}{n_{VT1}} \cdot V_{2A} = V_{1A} \quad (35b)$$

Substituting (35b) into (35a) yields:

$$V_{OP(A)} = \left| V_{1A} - b \cdot V_{1A} \right| = \left| V_{1A} \right| \cdot \left| 1 - b \right| \quad (35c)$$

Or expressing the error as a proportion of the bus voltage:

$$\frac{V_{OP(A)}}{\left| V_{1A} \right|} = \left| 1 - b \right| \cdot 100\% \quad (35d)$$

For example, with negative 0.5% magnitude error and 0.3 deg angle error, the spurious operating voltage would read:

$$\frac{V_{OP(A)}}{\left| V_{1A} \right|} = \left| 1 - (1 - 0.005) \angle 0.3^\circ \right| \cdot 100\% = 0.72\%$$

The error is at the level that encroaches on the targeted sensitivity settings. Note, however, that this method would accommodate some of the error in the matching factor k , leaving only a small variable fraction of this error unaccounted for. Assuming 0.15% magnitude error for both the ITs and the relay, and 0.2deg angle error gives 0.38% of bus voltage read as a spurious operating signal.

It is important to understand that the method compares two voltages. Both errors will play a role. They may cancel mutually, or add up.

6.2 Impact of Instrumentation Errors on the Compensated Bank Neutral Voltage Unbalance Function

The approach illustrated in the previous subsection applies to this protection method as well. Examining the key operating equation for secondary voltages (7) leads to a conclusion that during normal system conditions four voltage components, each of a very small or zero magnitude, are added as vectors: neutral point bank voltage, system neutral voltage and two phase voltages – the latter two with very small multipliers.

These four voltages are delivered by four VTs: (A,B,C,X) in case of implementation (7a) with internally derived system zero-sequence voltage; and (0,X,B,C) in case of implementation (7b) with externally supplied system zero-sequence voltage. For the purpose of error analysis, each of the VTs shall be represented with its own ratio, potentially slightly different than the nominal value.

When deriving the system zero-sequence voltage internally the three phase voltages are added as vectors – small errors could yield a relatively significant spurious system zero-sequence voltage. The following derivative of equation (7a) is useful:

$$V_{OP} = \frac{1}{3 \cdot n_{VT}} \left| n_{VTX} \cdot (1 + k_{AB} + k_{AC}) \cdot V_x - n_{VT} \cdot V_A - k_{AB} \cdot n_{VT} \cdot V_B - k_{AC} \cdot n_{VT} \cdot V_C \right| \quad (36a)$$

For the purpose of error analysis, the k -factors can be assumed to be unity, and therefore:

$$V_{OP} = \frac{1}{3 \cdot n_{VT}} \left| n_{VTX} \cdot 3 \cdot V_x - n_{VT} \cdot V_A - n_{VT} \cdot V_B - n_{VT} \cdot V_C \right| \quad (36b)$$

Assume the above is perfectly balanced and an error in the measurement of the bank neutral voltage is added, represented by the complex number b :

$$V_{OP} = \frac{1}{3 \cdot n_{VT}} \left| n_{VTX} \cdot b \cdot 3 \cdot V_x - n_{VT} \cdot V_A - n_{VT} \cdot V_B - n_{VT} \cdot V_C \right| \quad (36b)$$

From equation (36b):

$$n_{VTX} \cdot 3 \cdot V_x = n_{VT} \cdot V_A + n_{VT} \cdot V_B + n_{VT} \cdot V_C \quad (36c)$$

Substituting (36c) into (36b) gives:

$$V_{OP} = \frac{1}{3} |(b-1) \cdot (V_A + V_B + V_C)| = |b-1| \cdot |V_0| \quad (36d)$$

In other words, the error in the operating signal is proportional to the system unbalance, with a small multiplier. As a result, errors in the measurement of the bank neutral voltage are of secondary importance. For example, assume a system unbalance (V_0) of 3% of bus nominal voltage, and a 5% magnitude and 1 deg angle error for the neutral point transformer. Using equation (36d) one concludes that this error introduces about 0.16% of bus nominal voltage as a spurious operating signal.

Bus VTs must be much more accurate to facilitate sensitive protection. Assume, a phase A VT is now exposed to measurement errors:

$$V_{OP} = \frac{1}{3 \cdot n_{VT}} \left| n_{VTX} \cdot 3 \cdot V_x - n_{VT} \cdot b \cdot V_A - n_{VT} \cdot V_B - n_{VT} \cdot V_C \right| \quad (37a)$$

From equation (36b):

$$n_{VTX} \cdot 3 \cdot V_x - n_{VT} \cdot V_B - n_{VT} \cdot V_C = n_{VT} \cdot V_A \quad (37b)$$

Substituting (37b) into (37a) gives:

$$V_{OP} = \frac{1}{3} |b-1| \cdot |V_A| \quad (37c)$$

In other words, 1/3rd of the bus voltage “leaks” as a spurious operating signal due to errors in the measurement. For example, assume 0.3% magnitude error and 0.2 deg angle error. These errors in the A-phase voltage with all the other measurements intact, i.e. with errors not adding and not canceling, would yield according to equation (37c) 0.18% of bus voltage as an error in the operating signal of this protection method.

When using externally derived system zero-sequence voltage (equation (7b)), requirements for the bank and system neutral voltage measurements are relaxed, and the accuracy of measurement of the two phase voltages becomes secondary because of the low value of multipliers applied to the B and C voltages.

Generally speaking the method is most impacted by the accuracy of the measurement of the system neutral voltage. This quantity is derived regardless of the method applied (internally, externally to the relay) out of three vectors each having significant magnitude compared with the target sensitivity. Small magnitude and angle errors in sensing any of the three vectors would become significant for this sensitive protection function.

6.3 Impact of Instrumentation Errors of the Phase Current Balance Function

When using a window-type CT to measure the differential current, this method is quite immune to instrumentation errors. From equation (12) the method balances the differential current with a small fraction of the total bank current. Both signals are low: the former because of the near-zero circulating current; the latter because of the multiplier. As a result the errors are decimated when they “leak” into the operating signal.

Analysis of equation (12) yields the following expression the error analysis:

$$I_{OP} = |b-1| \cdot |I_{DIF}| = |b-1| \cdot |k| \cdot |I| \quad (38)$$

For example, assume 2% of full bank current circulating in the window CT ($k = 0.02$), and 5% magnitude and 3 deg angle error in the phase CT. According to equation (38) the spurious operating signal will reach 0.14% of the total bank current.

6.4 Impact of Instrumentation Errors of the Neutral Current Balance Function

As explained in the previous section, the neutral and phase current balance methods are equivalent. The differential neutral current is compensated for inherent unbalance by all three currents (per equation (18)), but similarly to the phase current balance method the multipliers for the phase currents are small. Therefore, equation (38) applies to this method, and yields the same results as to the impact of measurement errors.

Overall the relative insensitivity of the current balance methods to instrumentation errors can be understood by realizing only small portions of the phase currents are used for compensation, while the differential currents – if measured via window CTs – are not exposed to any significant errors.

7. Comparison with Traditional Methods

Traditionally, either a given function is desensitized to account for inherent bank unbalances and instrumentation errors. Or, a historical value of the non-zero operating quantity is subtracted (Δ -changes) before comparing with a pickup threshold (P) resulting in the rate-of-change mode of operation:

$$\Delta|V_x - V_0| > P \quad (\text{neutral unbalance}) \quad (39a)$$

$$\Delta|I_{DF}| > P \quad (\text{phase or neutral current unbalance}) \quad (39b)$$

The rate-of-change approach improves sensitivity to some extent but has limitations.

First, it is an approximation. As derived in section 4, the "leaking" values are proportional to present values of some other signals related to the bank (example: differential current in the phase balance method proportional to the total bank current). When the currents do not change, the delta method works satisfactory. But when the currents change, such as during close-in external faults, subtracting an old value will not compensate correctly. Time delay or other inhibit method may be needed to ride through such conditions.

Second, the rate-of-change approach will not provide for a sustained operating signal. When the delta-t window slides entirely into the fault, the operating signal will reset. This creates a problem when time-delayed operation is assumed.

Methods for inherent bank compensation presented in section 4 identify the true cause of the unbalance, and as such are accurate under system balanced conditions, minor unbalances, and major system events such as close-in faults. Their operating signals are sustainable allowing time delayed alarming and tripping with no restrictions.

Major system unbalance is an important condition to consider. For example, assume a close in ground fault elevating both the system zero-sequence voltage and the bank neutral point voltage. The compensated neutral unbalance method is based on equation (5):

$$V_{OP} = \frac{1}{3} |(1 + k_{AB} + k_{AC}) \cdot V_x - 3 \cdot V_0 + V_B \cdot (1 - k_{AB}) + V_C \cdot (1 - k_{AC})|$$

During the outlined ground fault event, V_x and V_0 assume significant values and will balance perfectly as long as the relay uses proper settings for the inherent bank unbalance compensation (k -values) and the instrumentation errors are low enough compared with the applied setting. The other two voltage components are of secondary importance as they use small multipliers.

Simplifying one can write the following balance equation for this function:

$$V_{OP} = |V_x - V_0| \quad (40a)$$

In other words, the operating signal is a vectorial difference of two voltages. In order to better cope with errors and avoid penalizing sensitivity an optimized restraining signal can be created as follows:

$$V_{REST} = |V_x + V_0| \quad (40b)$$

Note that the above signal is not a classical restraint in the form of a sum or average of the magnitudes. This would affect sensitivity of the function. Instead the restraint is a vectorial sum of the two voltages.

To understand better how this approach works, consider external fault and internal bank failure.

Assume an external fault producing 20% of system zero-sequence voltage. Assume further, the bank neutral point voltage is measured as $0.2 pu \angle 0^\circ$ while the system zero-sequence voltage is measured as $0.17 pu \angle 5^\circ$ due to finite accuracy of instrument transformers and the relay, transients, etc. If so, the function even if perfectly compensated for the bank inherent unbalance would see an operating signal of:

$$V_{OP} = |0.2 pu \angle 0^\circ - 0.17 pu \angle 5^\circ| = 0.034 pu$$

If used to trip instantaneously without a restraint the function will have to be set above this level.

Calculate the proposed restraining signal:

$$V_{REST} = |0.2 pu \angle 0^\circ + 0.17 pu \angle 5^\circ| = 0.37 pu$$

Note that the applied definition of the restraint practically doubles the two involved signals. Assuming a slope is used for tripping, it will take $0.034/0.37 = 9.2\%$ of slope to restrain the operation.

Consider an internal bank failure under 5% of system unbalance (system zero-sequence voltage). Assume further, the bank failure changes the neutral point voltage by 2% of bus voltage at the angle of 180° (worst case):

$$V_0 = 0.05 pu \angle 0^\circ, V_x = 0.05 pu \angle 0^\circ - 0.02 pu \angle 180^\circ = 0.07 pu \angle 0^\circ$$

The operating signal is:

$$V_{OP} = |0.07 pu \angle 0^\circ - 0.05 pu \angle 0^\circ| = 0.02 pu$$

The restraining signal is:

$$V_{REST} = |0.07 pu \angle 0^\circ + 0.05 pu \angle 0^\circ| = 0.12 pu$$

Assume a 10% slope setting is applied. The ratio between the operate and restraining signals is $0.02/0.12 = 17\%$ allowing for sensitive operation given the slope of 10%.

Change in the voltage at 180° is the worst case. Under the best case scenario one obtains $0.08 pu$ of restraint, or $0.02/0.08 = 25\%$ of the operate-to-restraint ratio.

Careful application of restraint allows further improvement of security while maintaining good sensitivity of the capacitor bank protection functions.

8. Summary

This paper derives correct balance equations for short circuit protection of shunt capacitor banks taking into account inherent unbalances in the protected bank. Four methods are derived: voltage differential, compensated neutral voltage unbalance, phase current balance, and neutral current balance.

As can be seen from key equations (1), (5), (11), and (18) the proper way of balancing the bank (or banks) involves instantaneous values of currents or voltages. Subtracting the residual unbalance as a time-delayed signal (a historical, or a constant value), and responding to the delta changes does not constitute a proper, sensitive and secure operating equation for protective relaying purposes.

The methods presented in this paper compensate for both bank and system unbalances. Therefore they are insensitive to major system events such as close-in faults. Presently used relaying techniques might misoperate on such system conditions, as they typically disregard system unbalances and compensate for the bank unbalance assuming no, or minor system unbalances.

The exact balance equations developed in this paper open a chance to perform manual, or automated adjusting of the operating logic in order to accommodate the inherent unbalance of the bank either due to un-repaired failures, temperature or seasonal changes, or changes due to removing, shorting, or repairing the cans. This can be done as auto-setting, i.e. one time adjustment after the repair and under user supervision, or as self-tuning, i.e. a continuous tracing of the slightly changing capacitor reactances in order to maintain optimum sensitivity to internal failures, and security during system unbalances.

The voltage differential, phase and current balance methods are subject to self-tuning under any conditions; the neutral voltage unbalance is subject to self-tuning as long as the neutral point voltage is above the measuring error level. When applied in the self-tuning mode the methods continuously compensate for temperature and seasonal changes, in a slow loop of modifying their balancing coefficients based on actual values. Note that the majority of the balancing coefficients developed in this paper are ratios of impedances. As such they are already greatly insensitive to temperature and seasonal changes.

If implemented in the self-tuning mode a given method shall still monitor the total drift in the operating signal even if very slow, and alarm if the amount of the drift signifies a danger of possible future failure, or a series of minor failures that went undetected or unattended to.

The involved balancing factors although in theory are complex numbers, could be very well represented by real numbers (uneven loss tangents of the capacitors in the bank, and errors of instrument transformers cause small imaginary parts of the matching factors). With the matching factors being real numbers, inherent unbalance of a capacitor bank can be easily zeroed out in the protection equations using only 1, 2 or a maximum of 3 coefficients. These coefficients can be tuned by measurements, and simple engineering calculations.

The paper analyses sensitivity of the developed methods and derives practical equations for the amount of the operating signals given the size of the bank failure. Also, impact of instrumentation errors (instrument transformers and relays) is analyzed quantitatively allowing one to optimize the secondary system design, and select settings based on data.

9. References

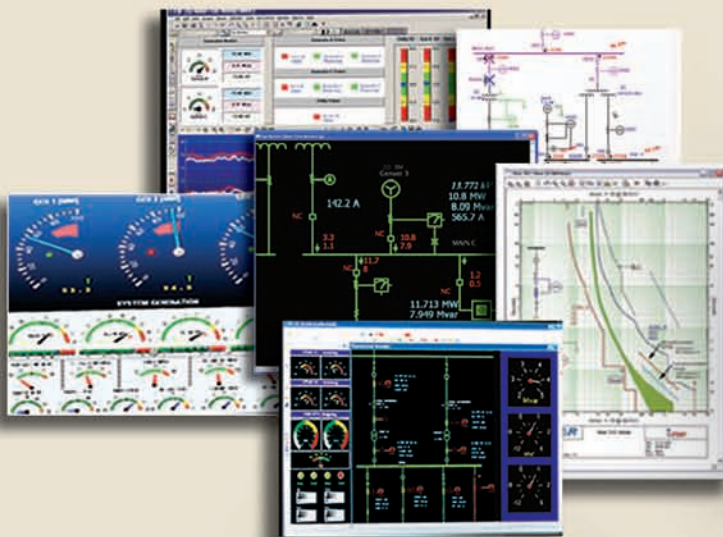
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Implementation and Performance of Synchronphasor Function within Microprocessor Based Relays

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1. Introduction

Synchronized phasor measurements have come a long way since their conception [1]-[3]. Many potential applications have been identified [2], including improved state estimation, frequency estimation, instability prediction, adaptive relaying, and wide area control, for example. The recently published IEEE Standard C37.118 [3] will assure that compliant phasor measurement units will all report phasors using the same convention for measuring phase angle, particularly when the underlying power system frequency is off-nominal.

Even though today's installations of Phasor Measurement Units (PMUs) are limited in cover-age and enterprise communication performance, it is clear the technology will advance quickly yielding significant benefits.

Widespread deployment of the PMUs providing for both appropriate penetration and redundancy of synchronized measurements is a key factor. Such widespread deployment can be achieved when integrating the PMU function within modern microprocessor-based relays - similar to the relay integration trend seen with metering, fault recording, and sequence of event re-cording capabilities.

Implementation of PMU functions, however, imposes new requirements on protection plat-forms. Most importantly PMUs require correlation of the waveform samples with the absolute time driven by the Global Positioning System (GPS), and reporting the measured phasors with reference to such absolute time. Traditional relay implementations sample their input voltages and currents asynchronously from any external process such as the GPS time, and derive measurements as quickly as possible for speed of response.

Additional processing requirements are presented for the relay to measure, communicate and record the PMU data in addition to providing for their core protection functionality.

All this raises potential concerns with respect to integrating PMU functions in protective re-lays. Whether on new platforms or as a part of an upgrade of an existing product, changes to the existing or commonly deployed data acquisition system of a relay in order to accommodate synchronphasors can have serious consequences for all the other functions of the relay- protection in particular.

This paper reviews the basic aspects of synchronphasor implementations integrated with protective relay functionality. It presents the key technical challenges, and discusses solutions that eliminate the risk of impacting the core protection functionality of the relay. The paper offers simple tests that can be applied to gauge the impact of an integrated PMU on the overall performance of a given relay.

The overall goal of this paper is to educate the user and allow for more rational decision making with respect to deploying integrated PMUs versus standalone PMUs.

2. Issues when Implementing Synchronphasors on Protection Platforms

It is self evident that wide penetration of PMUs facilitating both faster accumulation of experience in preparation for advanced applications, and redundancy of measurements required for the future critical applications of synchronphasors, can be naturally achieved by integrating PMU functions with protection and control platforms. Successful integration of sequence-of-events (SOE) and digital-fault-recorder (DFR) capabilities with protective relays is a historical lesson to follow when considering cost-efficient and widespread deployment of PMUs.

Modern protection platforms are capable of supporting synchronphasor measurements, local re-cording and reporting. This relates to internal architectures, time synchronization, metering accuracy, communication capabilities, and processing power required to comply with the C37.118 requirements.

However, microprocessor-based protection relays have been designed historically without regard to the notion of absolute time. Time stamping for SOE and DFR recording is probably the only instance of reference to an absolute time in protective relaying. Sampling and synchronization, even in critical and high performance systems such as the line current differential protection, is typically achieved without reference to the absolute time. This is a prudent protection approach as it limits exposure of mission-critical protection functions to availability and misbehavior of other devices such as the GPS system and associated receivers/clocks.

Predominantly protection relays sample asynchronously with respect to the absolute time, but in synch with power system frequency. The latter is to keep the digitally implemented measurements accurate should the power frequency depart from its nominal value.

The following sections provide some insight on implementation of synchrophasors on a typical microprocessor-based relay [4]. It presents some solutions, and highlights certain aspects that need to be understood and evaluated by a protection engineer to make sure the extra functionality put on a relay does not jeopardize the core protection task of the device.

3. Design Principles when Implementing Synchrophasors on Existing Platforms

It is prudent to follow these design principles when implementing synchrophasor measurements on existing or new protection platforms:

1. The underlying sampling process of the relay shall not be altered. Sampling and data collection potentially affects all other functions of the relay. To minimize the risk, this area shall not be modified. Sampling in synchronism with the absolute time is not only unnecessary; it actually yields a substandard solution from the point of view of metering accuracy as shown later in this paper.
2. The synchrophasor calculations shall be added in parallel to the existing protection, control and metering functions to minimize the risk of affecting these critical functions.
3. Hardware modifications shall be minimized for the reason of stability of the design.
4. Calculations shall be organized in a way that the extra processing power is optimally distributed and can be accommodated by existing platforms with appropriate security margin, even under fault conditions and other periods of increased activity of an IED.

The key design areas for implementation are: timing accuracy; sampling and correlating input signals with the absolute time, algorithms for accurate measurement of the phasors, data storage, recording and streaming.

4. Timing Accuracy

Accuracy of synchrophasors as measured by the C37.118 is defined as a Total Vector Error (TVE) being the percentage magnitude of a vectorial difference between the measured and actual phasors treated as vectors.

As such the TVE has three major components: magnitude error, angle error as related to the input signals, and angle error as related to the measurement of the absolute time.

It is enlightening to think of time as a quantity that needs to be “measured” by a given device based on a standard physical input, such as the 1 pulse per second (1pps) marker embedded in the standard IRIG-B input. Assuming 1% TVE target as per the C37.118, and budgeting accordingly for the three sources of error, leaves up to 5-8 microseconds for the total timing error.

Not only does a given device needs to synch with the 1pps signal but between the pulses, the device must internally maintain a very precise notion of time so that each of the synchrophasor reference points (referred in this paper as “synchrophasor interrupts”) occurring within the period of the full second is maintained with an error not larger than few microseconds.

Figure 1 illustrates this process. In one particular implementation a precise phase lock loop is run with the objective to null out the positional error between the 1pps signal and the last synchrophasor interrupt that ought to occur exactly at the top of the second. This phase lock loop compensates for the natural drift of the internal IED oscillator, and the finite resolution of the latter.

For example, a given oscillator could have an error of say 25 parts per million as specified by the component manufacturer. This means it could drift up to 25 microseconds over a period of 1,000,000 microseconds (1 second). This value would prevent successful implementation of synchrophasors. Moreover, the error can change with temperature and between different articles (samples) of the oscillator. The drift, however, is easily measurable with the aid of the 1pps signal. When measured, validated, and averaged, the drift of the oscillator is an input to the phase lock loop making the internal time keeping mechanism extremely accurate.

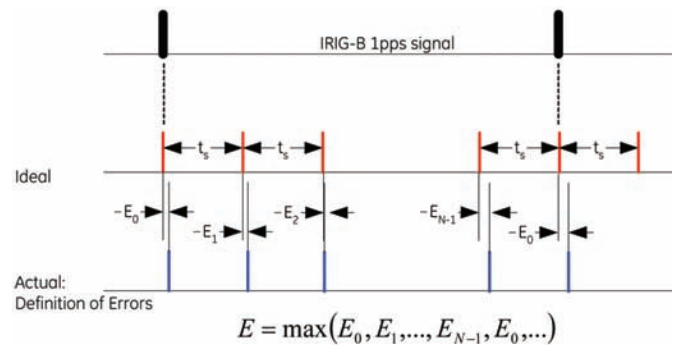


Figure 1. Defining synchrophasor interrupts and timing errors.

The compensation process works as follows. The algorithm, using a precise hardware-implemented interrupt service, captures the local relay time (oscillator value) at the exact moment of the 1pps reference pulse. If the internal relay oscillator is perfect, the captured value should be exactly 1,000,000 microseconds from the last 1pps pulse. A reading of 1,000,015 microseconds, for example, means the oscillator is 15 microseconds / second too fast; while the reading of 999,994 microseconds means the oscillator is 6 microseconds / second too slow.

The value of the second-over-second drift is checked for validity, and averaged over longer periods of time. The secure and smoothed out value is now used to control the oscillator or as a correction in the algorithm generating the synchrophasor interrupts. Our solution uses the measured drift of the internal oscillator to discipline the synchrophasor interrupt generator rather than control the oscillator [4]. This avoids changes to the relay and thus following the design goals outlined in section 3 above.

Another issue is the required resolution of the internal oscillator. Assuming 60 synchrophasors are produced per second, the synchrophasor interrupts are to be generated every 1,666.66(6) microseconds. When this number is rounded to a practical oscillating frequency, an error would accumulate making the last synchrophasor interrupts in a given second inaccurate. For example assume an implementation using 0.25-microsecond resolution that is generating synchrophasor interrupts every 1,666.50 microseconds. The 1,666.50 microsecond interval is off only by 0.166(6) microseconds from the ideal value. However, after 1 full second when this error adds up 59 times, the last interrupt within the second will come after $60 \times 1,666.50 = 999,990$ microseconds that is a 10 microsecond error from the required time.

In addition, assume the oscillator is too slow by 12 microseconds in each second (example). To compensate for the drift each synchrophasor interrupt will have to be adjusted by $12/60 = 0.2$ microsecond, while a practical resolution of the oscillator can be in the range of a quarter of a microsecond. The $0.25 - 0.20 = 0.05$ microsecond error repeated 60 times within each second would yield 3 microseconds of error eating away from the tight timing error budget required by synchrophasors.

To minimize this error, a dithering algorithm is applied yielding a high accuracy of timing for the synchrophasor interrupts. An internal variable is used to count the time with a nanosecond accuracy, while the interrupts are generated with a 0.25 microsecond resolution. The device keeps track of the error accumulated due to the finite resolution of the oscillator. Once the error reaches half the resolution period, the synchrophasor interrupt is moved by one resolution period. In this way the error is kept below half the period of the oscillator, and never accumulates.

The discussion on timing presented in this section is an excellent illustration of issues and challenges faced when implementing synchrophasors on existing relay platforms or traditionally designed new relay platforms. The solutions outlined in this section are elegant and avoid any changes to the existing relay hardware, thus minimizing the risk and avoiding expensive internal oscillator upgrades. The "time keeping" is implemented in software based on a carefully crafted algorithm.

5. Sampling for protection and synchrophasors

Protective relays typically do not sample synchronously with respect to the absolute time. Instead, they sample based on a free-running sample and hold timer and often apply frequency tracking or compensation so that the measurement calculations retain accuracy even if the system frequency departs from the nominal value. It is a common misconception that measuring synchrophasors requires sampling synchronously to absolute time.

Some applications force the data acquisition system (A/D converter) to take samples at precise pre-defined points in time with respect to absolute time. This, however, results in unnecessarily complicated designs, and is not required. In order to measure synchrophasors one needs to know the absolute time of each sample taken by the A/D, but these samples can be taken at any point in time. They do not have to be "hard-synched" to the GPS clock.

Relays and other devices measuring sine waves apply frequency tracking. These devices calculate features of sine-waves (magnitude, for example) using their measuring algorithms such as the Fourier Transform. These algorithms assume typically a constant pre-defined number of samples taken in each period of the waveform. If the system frequency changes, the period changes, and the number of samples in a period would change as well if using a constant sampling rate. This would yield certain finite measurement error. In order to eliminate this error either the sampling rate is made variable to follow the system frequency, or a numerical compensation is programmed in the device.

The first approach is typically more popular and referred to as "frequency tracking". Effectively, frequency tracking varies the length of the data window used for digital measurements to follow the length of the signal period as it varies under off-nominal frequencies and power swings.

Another misconception is that staying in synchronism with the system frequency (for accuracy) and staying in synchronism with the absolute time (for phase reference) are contradicting targets, and require convoluted solutions such as measuring the magnitude and angle using different algorithms.

The former is about adjusting the length of the data window so that it covers pre-selected multiples of power cycles; the latter is about positioning of this data window so that the measurement complies with the C37.118 angle convention.

Both can be controlled independently with no major obstacles. One may think about these two processes as having two controllers: one positions the center of the data window to align it precisely with the synchrophasor interrupts; the other controls the sampling rate to keep the length of the data window in relation to the slightly changing system frequency.

Although the samples must be correlate-able to absolute time, they can be taken at any time instant. Figure 2 presents a solution in which the samples are collected asynchronously with respect to absolute time. The platform applies frequency tracking to keep the number of samples constant in the actual period of the waveform as the period changes [4]. When the synchrophasor interrupt is asserted, the device locks the sample index and collects half its data window from the samples that follow the interrupt and half – from the samples preceding the interrupt. In this way, without altering the sampling process the device gets a data window that is placed very closely with respect to the required reporting point in time.

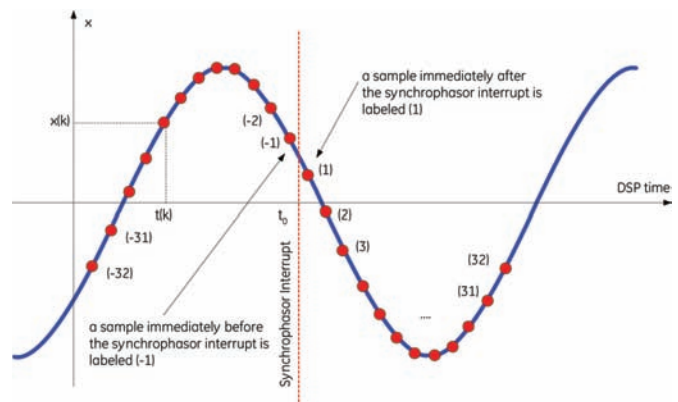


Figure 2. Data window based on asynchronously taken samples.

Note that in this approach:

- The length of the data window is already correct and adequate as the sampling period is controlled by the frequency tracking mechanism;
- The position of the window is within half of the sampling period from the required position as per the synchrophasor convention.
- It is trivial for the device to calculate the offset between the center of such “best-placed” window and the required position of the window. Calculate of this difference does not require referring to absolute time. This time difference is used to compensate the synchrophasor measurements as explained below.

The device calculates the center of the window by averaging the time stamps of the samples within the window. This averaging is done using any time reference, not necessarily the absolute time reference. In our implementation a free running microsecond counter is used to calculate the position of the center of the data window. The same free running counter is used to capture the time of the synchrophasor interrupt asserted based on the true absolute time. Even though the free running microsecond counter is not a true time, the time difference between the synchrophasor interrupt (point when the center of the window should be), and the calculated center of the window (point when the data window actually is) is precise and can be used for compensation.

Following the window selection procedure illustrated in Figure 2 the DSP places the window to within few degrees to the synchrophasor interrupt. The inherent displacement is precisely measured and is used for very precise compensation of the calculated phasor (an angular rotation of 2-3 degrees as described later in this paper).

This approach is ideal for typical relay architectures: samples are taken by data acquisition systems typically incorporating an A/D converter and a Digital Signal Processor (DSP). These data acquisition subsystems typically do not have a notion of absolute time. In our approach a very simple solution is adopted. In this architecture (Figure 3) the Central Processing Unit (CPU) of the IED synchronizes to the 1pps signal and executes the phase lock loop that generates precise synchrophasor interrupts. These interrupts are captured by the DSP using a “local DSP time” in the form of a free running counter. The interrupt triggers calculations for the synchrophasor instant and allows the DSP to obtain the notion of time, and produce the phasor precisely aligned with the time mark as driven by the interrupt.

6. Post-processing and Extra Filtering

As depicted in Figure 4, our device uses “best-placed” windows for synchrophasor measurement without altering the sampling process (windows X). It measures the small shift between the required and actual positions of such windows and compensates for the difference by a simple phasor rotation. This yields synchronized full-cycle Fourier windows (windows Y).

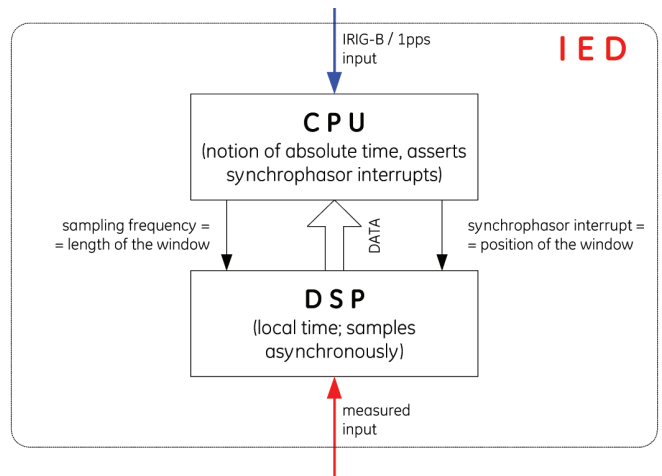


Figure 3. CPU & DSP architecture for synchrophasor implementation.

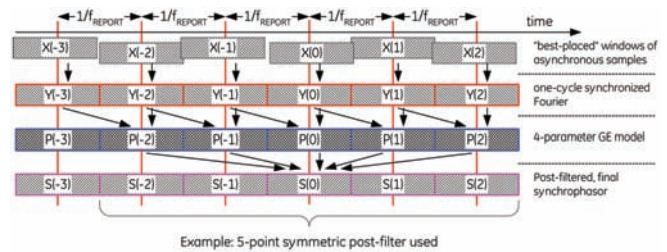


Figure 4. Processing of best-placed raw data windows into synchrophasor values.

The X and Y windows are produced at nominal system frequency regardless of the recording or reporting rates set for the PMU function. A pair of Y windows (the present and past windows) is used to implement the four-parameter signal estimator as described later in this paper. As a result a new, more accurate estimate of the phasor is calculated at the rate of nominal system frequency (windows P in Figure 4). The P-values are calculated assuming the phasor may change in time, and as such are extensions of the C37.118 synchrophasor standard, aimed at future dynamic applications of synchrophasors.

In order to control the balance between speed and accuracy of the measurement, the device further implements user selectable post-filtering, that is, a number of P-measurements can be combined into the filtered synchrophasor output, S, effectively extending the estimation window. The post-filtering is not a straight average, but takes into account the value and rotation speed of each of the used P-values as described later in this paper.

7. Compensating for Analog Errors

Synchrophasor implementation calls for accuracy above a typical protection accuracy or metering accuracy as typically provided on protective relays. When implemented on a protection platform, synchrophasors may need correcting for errors of the IED's input transformers.

Figure 5 shows a correcting function for the current inputs: the correction is small – in the order of 0.2 – 1.8 degrees – and depends on both the magnitude and frequency of the signal. In particular at very low signal levels and lower frequencies the excitation current of the input transformers starts causing some angular errors, and the device applies higher correction for the measured angle for the current inputs.

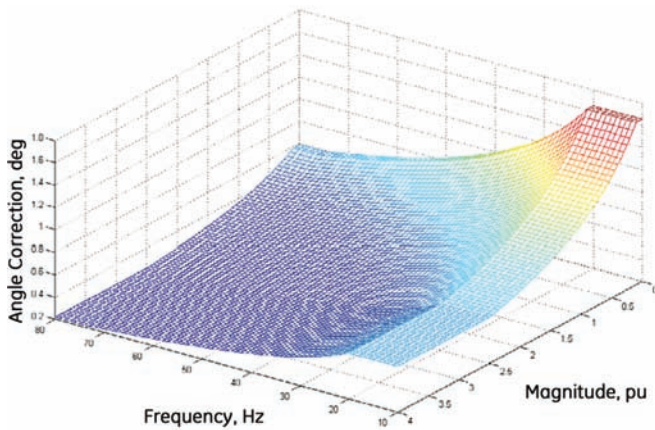


Figure 5.
Correction of current input transformers.

Figure 6 shows the correction applied to the voltage inputs. The required angle shift to keep the measurements accurate is smaller (up to 0.2 degrees), and again depends on the magnitude and frequency of a given voltage input.

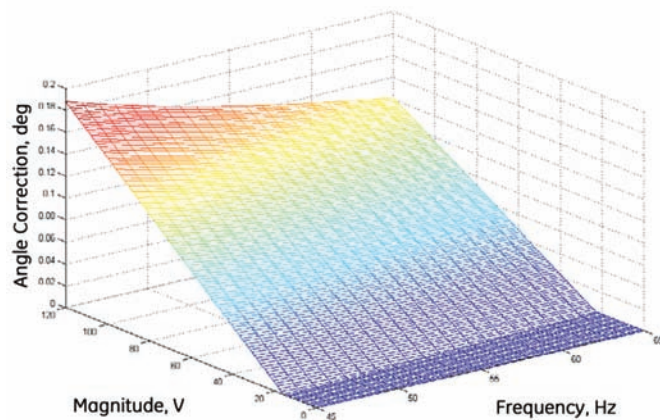


Figure 6.
Correction of voltage input transformers.

Analog filters, necessary in any digital measuring system to deal with aliasing of samples, introduce a phase shift, which also needs to be compensated. When the analog filter is set relatively high, the phase shift for the frequency band around the nominal is very linear, and can be easily compensated. Figure 7 shows the measured (red dots) and applied (blue line) correcting angles accounting for the impact of analog filters in the solution [4].

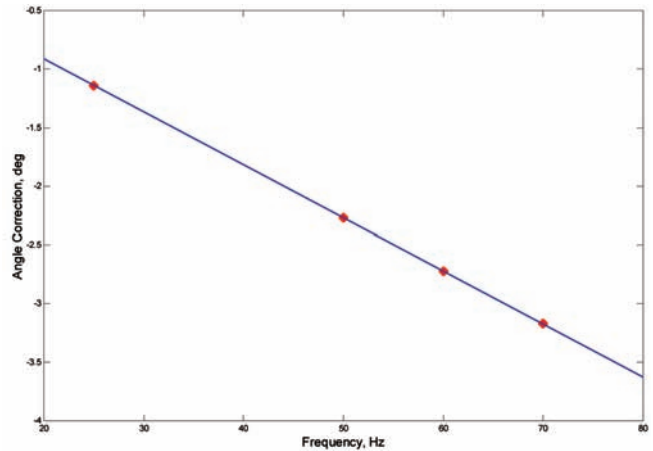


Figure 7.
Correction for the Analog Filter.

The few implementation details outlined above are meant to direct attention to the way synchrophasors are implemented on protective relays, and the potential impact on the existing mission-critical protection functionality. In the outlined implementation minor hardware changes were required to provide synchrophasor interrupts from the central processing unit, having the notion of the absolute time (from the IRIG-B input), to the digital signal processor, which is responsible for the majority of the calculations but has no direct relationship with absolute time. All the other aspects of the synchrophasor implementation have been accommodated in software, in subroutines completely detached from the key protection functions. This minimizes the risk and allows claiming a very secure implementation [4].

8. Implementation of the Data Communication Protocol

An important part of the C37.118 synchrophasor standard is the interoperable data communication protocol. The C37.118 protocol is a low-overhead “lean” protocol well suited for real-time data communication. The communication is organized around 4 types of frames:

- Configuration frames describing either present or maximum device configuration are sent to the higher order system (Phasor Data Concentrator, PDC) on demand or automatically upon configuration change of the PMU. These frames are therefore sent only exceptionally and are intended for the PDCs.
- Header frame is similar to the configuration frames but is not standardized and contain human-readable information about the PMU.

- Command frame is sent by a PDC and received by the PMU (relay when integrated). Commands are sent to stop and resume data transmission, request configuration data, or execute actual commands by sending data that could be used to close/open an out-put and execute other user-programmable actions.
- Data frames are sent continuously by the PMU (relay) at regular and C37.118 standardized time intervals.

Streaming data frames is of primary concern when considering integrating PMUs with micro-processor-based relays. The standard specifies 30 frames per second as the fastest reporting rate, but some implementations support up to 60 frames/second. Data content may vary from a single phasor (typically the positive-sequence voltage) to several sets of three-phase voltages and currents (frequency and rate-of-change of frequency are always sent).

Assume sending 6 phasors (3 currents and 3 voltages) each represented by 2 numbers (real and imaginary or magnitude and angle); with each number encoded on 2 bytes and reported at 30 frames a second. Ignoring the overhead one gets the bit rate of:

$$6 \text{ (phasors)} \times 2 \text{ (real, imaginary)} \times 2 \text{ (bytes)} \times 8 \text{ (bits)} \times 30 \text{ (frames / second)} \gg 5.76 \text{ kbps}$$

Even when accounting for the protocol overhead and doubling the reporting rate, as increasing the packet size by including frequency, rate of change of frequency, etc. one stays within the DSO level of 64kbps.

Modern protection relays are built to comfortably serve 64kbps real-time traffic. Such channels are used for teleprotection or in line current differential applications.

In additions, multi-function relays have been used for years to support SCADA and automation functions by providing for server functionalities of typical SCADA protocols (DNP, Mod-bus, UCA and IEC61850). Compared with these protocols the C37.118 synchrophasor protocol is neither complex nor demanding and can be safely implemented on a modern microprocessor-based relay.

9. Implementation of the Recording Functionality

Typically PMUs provide for data recording functions. These are useful in applications when no real-time communication is provided between the PMUs and the PDC, or in cases when the communication fails or is temporarily unavailable. Because system events are of interest, the time horizon for practical recorders is in the range of minutes or tens of minutes. This calls for mega-bytes of storage space.

Assume again the 5.67kbps data rate from the previous example, and consider a system event recorded for 10 minutes. The required storage space is in the range of:

$$10 \text{ (minutes)} \times 60 \text{ (seconds / min)} \times 5.67 \text{ kbps} \gg 3402 \text{ kb, or } 3.402 / 8 \text{ MB} \gg 0.42 \text{ MB.}$$

Modern relay may provide for tens of MB of data storage, allowing records as long as few tens of minutes even at very high recording rates.

Proper engineering of the recording function needs to allow for the following:

- Safe recording for tens of minutes during which faults and other events can occur.
- Safe power down when recording – the control power can be removed when the PMU function is recording and producing massive records. No data corruption or other unexpected deficiencies should take place under such circumstances.
- Safe retrieval of stored data. When using a slow communication media to access the relay, it may take minutes to download the stored records. During this time faults, system events, or new records may occur. The relay needs to respond accordingly always giving priority to the protection functions.

Recording capabilities are standard on modern relays. The above problems exist today, and have been solved. The only difference between an existing fault recorder and an added PMU re-corder is the amount of data and duration of recording or extracting the record from the device.

10. Requirements for the Extra Processing Power

Measuring (calculating) synchrophasors including: precise timing, data collection and data processing, and various required corrections as described earlier; communicating the measured data as well as serving requests from the PDC; and performing local triggering and recording re-quire extra processing power.

Modern relays use multiple processors for data processing, logic engines, and communications. As a result it is achievable and safe to integrate the PMU function, assuming a prudent approach is taken with respect to the architecture.

In our solution each set of 8 analog signals (ac voltage and currents) is given a separate DSP to process the associated data. This results in a scalable architecture when adding more inputs to a given relay does not put more requirements on the DSP. This is no different with the synchrophasor calculations. When interrupted by the synchrophasor time tag, a DSP gathers a data window, calculates the full-cycle Fourier phasor, calculates the center of the window and the offset of the center with respect to the synchrophasor interrupt, compensates (rotates) the phase to account for the small offset, and compensates for the errors of VTs, CTs and the impact of analog filtering. These operations are very lean and account for only a small portion of the full set of typical DSP calculations required.

The rest of the process of calculating synchrophasors runs only at 60 times a second, and is relatively simple (Figure 4).

The communication protocol runs at up to 60 times a second, and therefore is relatively lean as well. The same applies to the integrated PMU recorder.

In our approach, the processing power required to provide for the PMU function even when reporting at the rate of 60 phasors a second, is at the level similar to calculations required to run one zone of distance protection. We consider it moderate and acceptable. No protection functions are suspended or delayed as a result of synchrophasor activities/calculations. No synchrophasor functions are suspended or delayed as a result of protection events or activities.

11. TVE Accuracy Achievable when Integrating PMUs on Protection Platforms

The following summarizes the steady state performance as tested on the IED hardware [4]:

- TVE for voltages, frequency range 45-70Hz < 0.30%
- TVE for currents, frequency range 45-70Hz < 0.40%
- TVE at 10% of THD, nominal frequency < 0.45%

Figure 8 presents results of the interfering frequency test when reporting at 60 times per second, and using a user-selectable 7-point post-filtering algorithm.

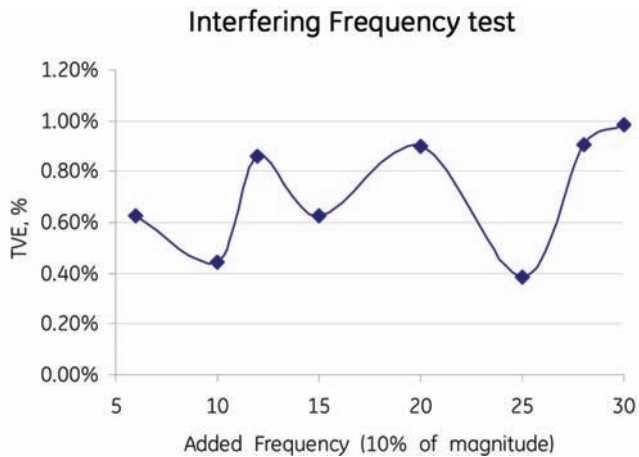


Figure 8.
TVE under interfering frequency tests
(reporting at 60/second, 7-point post-filter applied).

The described implementation details, and the test results prove that when carefully engineered, modern P&C platforms allow for both secure and accurate implementation of synchrophasor measurement, recording and reporting. When integrated with protection platforms the PMU functionality is provided universally with wide coverage of the metering points, at a fraction of the cost of stand-alone PMU solutions.

12. Examples of Synchrophasors Measurements under Fault Conditions

This section presents few examples of synchrophasor measurements under simulated fault conditions.

Figure 9 shows a case of a reverse ABG fault as recorded by a line current differential relay. During the fault the system frequency was 59Hz, and the relay frequency tracking mechanism was intentionally disabled in order to test the response of both protection and PMU functions under frequency errors.

The top three traces show current waveform recorded by the relay. The next three traces are voltages, with the A and B voltages dropping to zero during the fault.

The last trace shown in Figure 9 is the operand of the 87L function. As expected, the integrity of this key function is not jeopardized by either the external fault, off nominal frequency, or PMU function operational on the same IED platform. Similarly other protection functions respond correctly. For example, the neutral directional reverse-looking overcurrent element picks up during the fault and stays operated for the entire duration of the fault.

The "PMU1 Va Mag" trace shows the magnitude of the phase A voltage as measured by the synchrophasor algorithm. The value is steady and accurate regardless of the off nominal frequency (signal at 59Hz, relay sampling at 60Hz). The "PMU 1 Va Angle" trace is the angle measurement. This value is recorded at 60 times / second and makes one full revolution every second. This is

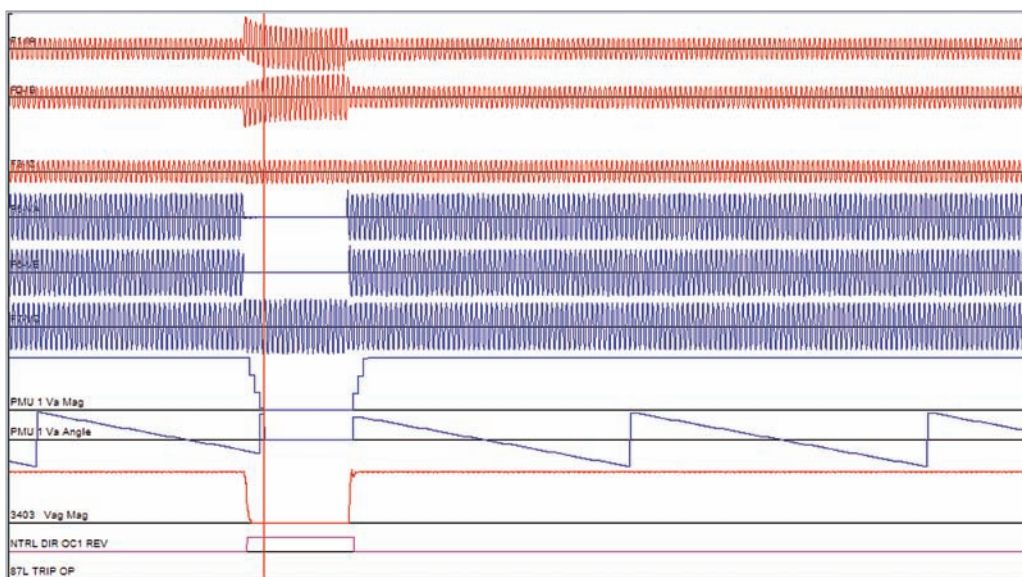


Figure 9.
Sample record of a line-current differential relay containing both oscillography data (samples) and PMU data (synchrophasors).

expected as the signal is at 59Hz, thus recorded 60 times a second it changes at $(60-59)*360\text{deg/sec}$.

For comparison the "3403 Vag Mag" trace is the voltage magnitude as measured for protection purposes. The synchrophasor version (PMU1 Va Mag) and the relay version (3403 Vag Mag) are better shown in Figure 10. The synchrophasor measurement is implemented using an algorithm optimized for accuracy. As such this trace does not show the ripple distinctive for the off nominal frequency situation, and is accurate to within 1% of TVE. The protection measurement is affected by the off nominal frequency (visible ripple and the average value slightly off). This is because the relay was configured with frequency tracking disabled for the purpose of the test. Even with tracking disabled this particular relay shows only 2-3% of error in voltage for every Hz of frequency difference.

Figure 10 also illustrates that the synchrophasor values are recorded every 1/60th of a cycle (user setting), while the protection values are refreshed 8 times a cycle or every 1/480th of a second. Also, having less filtering and being optimized for speed rather than accuracy, the protection version of the voltage measurement responds much quicker to the voltage changes, exhibiting a short lasting overshoot when the voltage recovers after clearing this external fault. At the same time the synchrophasor measurement is very well controlled showing no overshoot or other problems.

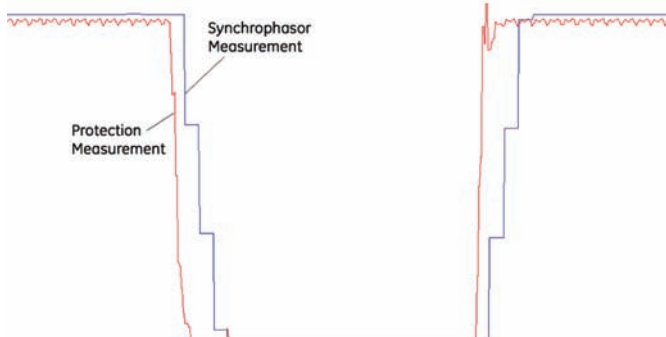


Figure 10.
Synchrophasor and protection measurements on the same voltage signal in the record of Figure 9.

Figure 11 shows an internal fault occurring under off nominal frequency (59Hz while the relay intentionally tracked to 60Hz). The fault is cleared by the 87L function as expected. Other protection, such as zone 2 shown in the Figure, operate as expected and stay picked up for the entire duration of the fault.

This test was done as a closed loop test resulting in opening the breaker. Once the breaker opened, the line-side VTs measure the voltage oscillating between the line capacitance and shunt reactors. The phase C voltage decays exponentially and the frequency measured by the relay changes from 59Hz in the pre-fault period, to about 50.3Hz being the resonating frequency between the line and its shunt reactors (Figure 12).

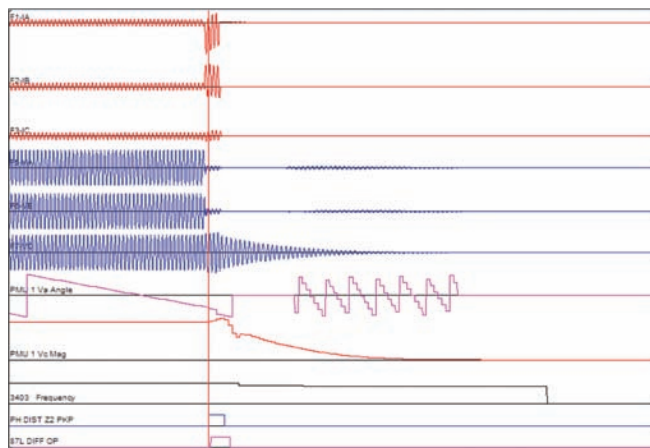


Figure 11.
Sample record of a line-current differential relay containing both oscillography data (samples) and PMU data (synchrophasors).

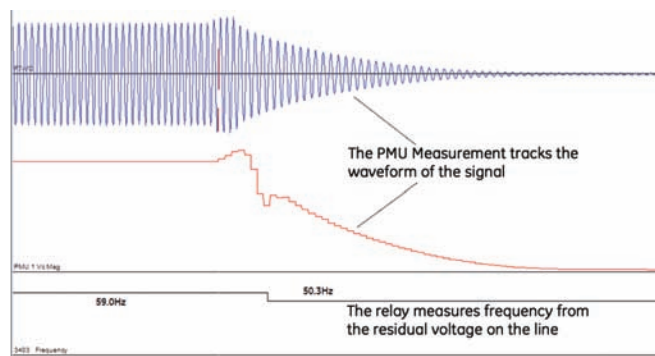


Figure 12.
Phase C voltage decays after the breaker opens. The PMU measurement tracks the dynamic of this signal. The measured frequency registers the actual 50.3Hz resonant frequency between the line and its shunt reactors.

The phase A voltage registers small values coupled via the shunt reactors after the breaker is opened and the fault removed. It is worth observing the phase angle of this voltage as measured via the synchrophasor algorithm. Figure 13 displays the phase A voltage angle. Before the fault the angle changes at the rate of 360deg/sec because it is reported at 60 times a second while the signal is of 59Hz ($(60-59)*360\text{deg/sec}$). When the voltage is driven by the 50.3Hz resonant frequency on the disconnected line, the angle changes much faster at $(60-50.3)*360\text{deg/sec} = 3500\text{deg/sec}$, or one full revolution every in less than 100ms.

Examples presented in this section demonstrate the power of synchronized measurements to post-mortem analysis, including faults. Also, they depict secure co-existence of protection and PMU functions on the same IED platform.

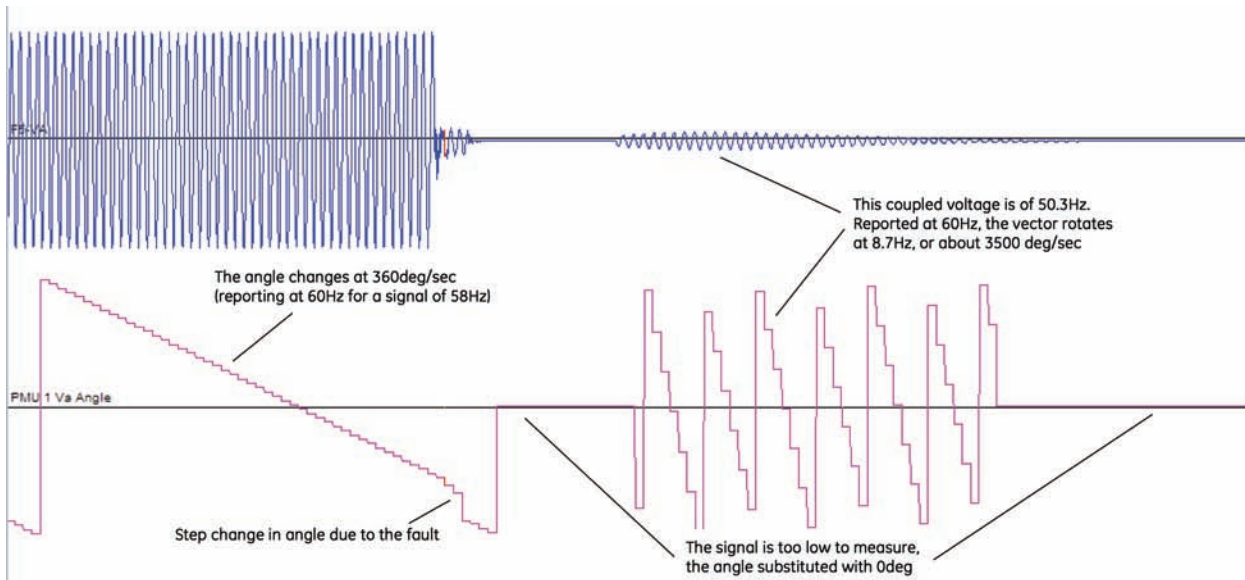


Figure 13.
Phase A voltage coupled after the breaker opens. The PMU measurement reflects the frequency of this signal (seen as the rotating phase position of the voltage vector).

13. Testing Recommendations for PMUs integrated with Protective Relays

Protection and control platforms integrating PMU functions should be tested in both protection and PMU modes of operation.

The protection functionality shall be tested given specific evaluation and approval philosophy for protection and control relays. During those tests the PMU functions should be enabled and configured in a way representative for a typical or worst-case future application. Similarly, the PMU functionality should be tested with a set of protection functions enabled and configured to reflect typical or worst-case future applications.

Having both sets of functions enabled and configured allows identifying any natural or unintended interactions between the two functionalities.

While the above general rules are followed, a few specific tests are worth recommending as follows:

- Speed of response of key protection function shall be checked during PMU-related activities. This includes normal PMU operation and extra activities such as coincidence of a system fault with a PMU command issued towards the IED from the PDC, local recording being initiated or in progress, retrieval of local records, and so on.
- Accuracy and integrity of key protection functions shall be checked during increased PMU activity.
- Accuracy and speed of response of key protection functions shall be checked during off-nominal frequencies. This includes steady state frequency deviations as well as frequency ramps. Modern protective relays are typically designed to retain full functionality under steady state off nominal frequencies, and exhibit only slightly degraded performance under frequency ramps, with the extent of degradation depending on the rate

of frequency change. Increased demand on PMU accuracy under abnormal frequency conditions may result in shifting the design targets - potentially impacting performance of the core protection functions of the device.

- PMU functionality shall be checked under fault conditions. This includes any impact on accuracy after the fault is cleared, as well as integrity during the fault condition. For example, are all data frames produced during the fault or some of them may be lost? Is the post-fault steady state accuracy as expected or is the disturbance is having a long lasting impact on the accuracy of subsequent measurements?
- Integrity of both protection and PMU functions shall be checked under periods of simultaneous activity. For example, a command frame can be issued toward the IED just before a fault is applied – response to the fault should be checked as well as response to the command frame.
- Integrity of protection functions should be checked under impairments of IRIG-B input signal. Having to correlate measurements with the absolute time, IEDs implementing PMU functions may become affected by impairments of the IRIG-B timing signal. Adding noise, particularly to generate spurious 1pps patterns, or invalidating the time and date code is a meaningful check when overlaid on fault conditions. Step changes in time and date generated at the IRIG-B clock, or leap seconds, are good tests as well. Overall integrity of protection – both speed and selectivity – should be verified under such abnormal activities of the IRIG-B input.
- Communication impairments related to the PMU-PDC data exchange should be tested with respect to integrity of key protection functions. Classical channel impairments such as bit error rates corrupting the packets, multiple requests, invalid requests, etc. should be placed simultaneously with fault conditions. Selectivity and speed of protection should not be compromised.

- Dynamic response of the synchrophasor measurements under fault conditions should be tested and understood. The C37.118 standard does not mandate any specific performance under dynamic conditions, such as during system faults. However, PMU records will be a valuable source of information for post-mortem fault analysis. Response of a particular synchrophasor algorithm under fault condition needs to be tested and understood before the records can be used for fault analysis.

14. Synchrophasor Measurement Algorithm

This paper describes implementation of synchrophasors on modern relay platforms. Our particular implementation uses an optimized algorithm aimed at measurements under dynamic conditions.

Under steady-state operation of a power system at a constant known frequency, the appropriate definition of a synchrophasor is intuitive and obvious, and is the one specified by the C37.118 standard [3]. However, during dynamic conditions, it is not as clear what the definition should be. Also it is well known that off-nominal frequency operation [5] or power swings [6] can cause issues in the accuracy of the results of a classical phasor computation. For example, a power swing is actually equivalent to at least two closely spaced, distinct power frequencies with comparable amplitudes. Which one should be reported? Our implementation uses a multi-parameter model that resolves these issues, as well as matching the classical model under steady state operation at a single frequency.

Under steady-state conditions, a synchrophasor is the cosine and sine projections of a power system signal, at whatever frequency the power system is operating [3]. It is not necessary or likely for the power system to be operating exactly at the nominal frequency. The phase angle of a synchrophasor is defined to be the angle between the reporting time-tag and the peak of the signal, at the actual frequency [3], so the issue of steady state off-nominal frequency does not arise in the definition of synchrophasors, only in their implementation [5].

The question arises how to define a synchrophasor during changing conditions? A logical approach is to define the power system signals to be projections of phasors that themselves are changing in time:

$$\begin{aligned}
 x(t) &\approx \sqrt{2} \cdot \text{Real}(\overline{\mathbf{X}}(t) \cdot e^{j2\pi \cdot f \cdot t}) \\
 x(t) &= \text{instantaneous current or voltage} \\
 t &= \text{time} \\
 \overline{\mathbf{X}}(t) &= \text{time varying phasor}
 \end{aligned}
 \tag{1}$$

Definition (1) encompasses both changes in phase angle as well as changes in amplitude, so it models both the off-nominal frequency case, as well as power swings. The value of a phasor at a time-tag is simply the value of the time varying phasor in (1) when the time is equal to the value of the time-tag of the reported synchrophasor.

It is well known that the classical algorithms for computing phasors on a per-phase basis from sequences of samples incur errors during off-nominal frequency operation [5], [7] or during power swings [6]. Most of the errors cancel out in positive sequence phasors that are computed from per-phase phasors, provided that the negative sequence value is equal to zero. If there is some negative sequence, the errors in per-phase phasors do not exactly cancel, so there is residual error in the positive sequence phasor.

It is impossible in principle to tell the difference between off-nominal frequency operation and a constant time rate of change of the phase angle of the phasor. In either case, if the sampling rate is not matched to the power system frequency, errors arise [5], [7] in the classical algorithms. For constant amplitude and phase angle signals, the computed per-phase phasors trace an elliptical trajectory [7]. The eccentricity of the ellipse can be predicted from the frequency. If the frequency is known, the errors in the per-phase phasors can be exactly compensated, though there will still be an issue of incomplete harmonic rejection. Two other solutions to the off-nominal issue include frequency tracking and re-sampling.

The off-nominal frequency effect is equivalent to a backward rotating error [6]. If the underlying phase signals are balanced, the backward rotating errors cancel in the positive and zero sequence phasors computed from phase values, although there will be an apparent negative sequence component. If the phase signals are not balanced, there is trouble in general.

The power swing case has been analyzed in [6], and one method for greatly improving the accuracy using a raised cosine windowing function has been described.

Another method, described here, uses a Taylor's series expansion to represent a time varying phasor to address both the off-nominal frequency effects as well as power swing issues with a simple extension of the classical algorithms for computing phasors.

To solve this problem our implementation assumes both the magnitude and "phase" of a phasor to be linear function of time, and estimates such varying phasors to fit them best to the measured waveforms. As a result our model gives much better response under dynamic system conditions.

15. Conclusions

This paper discusses various implementation issues related to integration of synchrophasor measurements and PMU functionalities on microprocessor-based relay platforms.

The paper alerts prospective users to possible pitfalls of the integration and allows making a more informed decision based on the understanding of both the synchrophasor and relay technologies.

The paper discusses sample tests that could be used to probe the robustness of the integrated PMU/relay implementation.

We presented one particular way of implementing synchrophasors that calls for practically no changes to the underlying relay architecture. The sampling, frequency tracking, data collection and

manipulation processes have been preserved with no changes. All the synchrophasor related calculations and operations are kept completely separated within a framework of object-oriented programming. The only change is the addition of one new interrupt between the CPU and DSP. This interrupt is not used at all by any of the protection functions, thus minimizing any danger of unintended changes.

The presented implementation is based on a novel multi-parameter algorithm for estimating synchrophasors under dynamic system conditions. The approach assumes slow transients in the estimated phasors and solves the assumed multi-parameter signal model accordingly to provide for both accurate and fast synchrophasor measurements.

Test and simulation results prove equivalency with classical algorithms under steady states, and superior performance under system transients.

Test results on the actual hardware allow claiming accuracy of approximately twice as good as the most stringent requirements of the IEEE Std. C37.118.

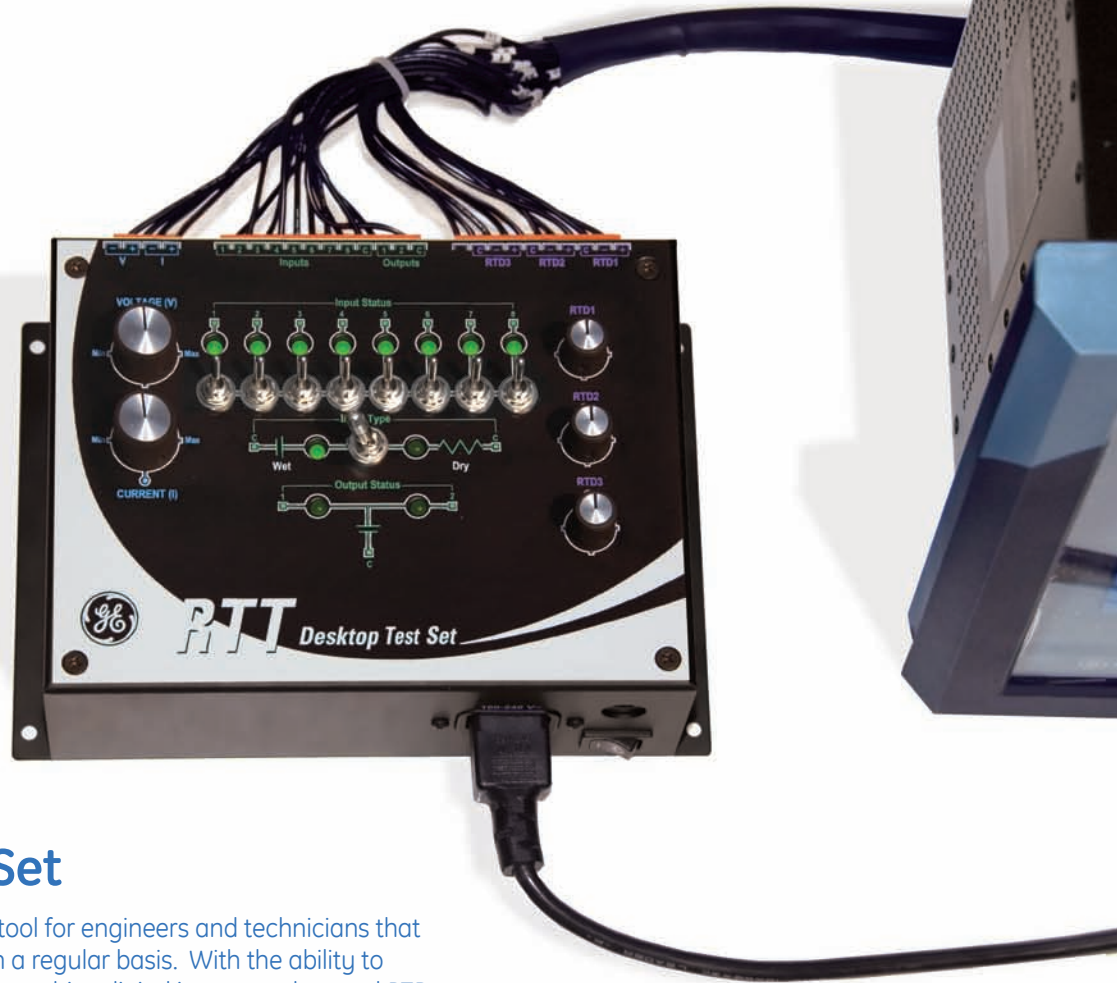
It is justified to assume that synchrophasors will follow SOEs, DFRs, RTU and metering functions and become universally integrated on modern relay platforms. This is not only possible with future new platforms, but also within existing presently used relays. Careful engineering allows safe implementations and the accuracy equal if not better than standalone PMUs.

Integrated PMUs will allow wider penetration of this new technology, faster learning curve, and cost savings related to purchasing, installing and operating the equipment.

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Application of Modern Relays to Dual-Breaker Line Terminals

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1. Introduction

Standard practice today with respect to protecting dual-breaker line terminals – breaker-and-a-half or ring-bus – is to sum the two breaker currents externally and feed a single-input line relay (distance, line current differential or phase comparison) with the total current flowing into the protected line. Breaker failure protection requires monitoring the two breakers and currents separately, and is typically implemented as a stand-alone device out-side of the main protection relay. Reclosing and synchrocheck control functions require monitoring and controlling both breakers as well as measuring two pairs of voltages for the purpose of synchrocheck, are also – in majority of cases – implemented outside of the main line protection device.

This paper discusses several protection and control aspects in relation to dual-breaker line terminals.

First, breaker failure and reclosing functions are discussed as applied to dual-breaker configurations.

Second, the paper talks about protection security as related to saturation of Current Transformers (CTs) under fault currents flowing locally through the two breakers. When the two currents are summated externally, the CT errors – if significant – can override the potentially low actual line current, and cause stability problems for the main line protection. Not only sensitive ground overcurrent functions are jeopardized, but also distance, current differential, or phase comparison. The paper explains the problem and presents solutions.

Stub bus protection is also discussed as pertaining to dual-breaker configurations.

The paper looks at the above applications from the point of view of a modern micro-processor-based relay. New generation of line relays support dual CT inputs to monitor both breakers individually, and three voltage points to provide for the main line protection, and synchrocheck across both breakers. These relays often include two breaker failure, two synchrocheck, and dual-breaker autoreclose functions. This allows integrating protection, breaker failure and reclose functions into a single relay. The paper points to advantages and disadvantages of such integration, and provides some guidance regarding dual-breaker line applications.

2. Capabilities of Modern Line IEDs

Modern microprocessor-based line protection relays (or Intelligent Electronic Devices, IEDs) allow for protection and control of the dual-breaker line arrangement from a single device. Application of separate breaker failure and/or synchrocheck relays is no longer dictated by limitations of the main protection relay, but driven by the user's protection philosophy to either combine the required functions, mostly for the for cost benefit, or to keep them separate for security, retaining present testing and maintenance practices, avoiding re-training the personnel, etc.

With reference to Figure 1, a modern IED capable of the dual-breaker application supports two three-phase current inputs in order to measure both the currents individually for the breaker failure protection (50BF), backup overcurrent protection (51P), and associated metering functions. The two currents are added internally in the relay's software to become the input for the distance (21) or high-set overcurrent (50) functions. When properly implemented, the line current differential (87L) and phase comparison (87PC) functions use individual currents for stability under through fault conditions.

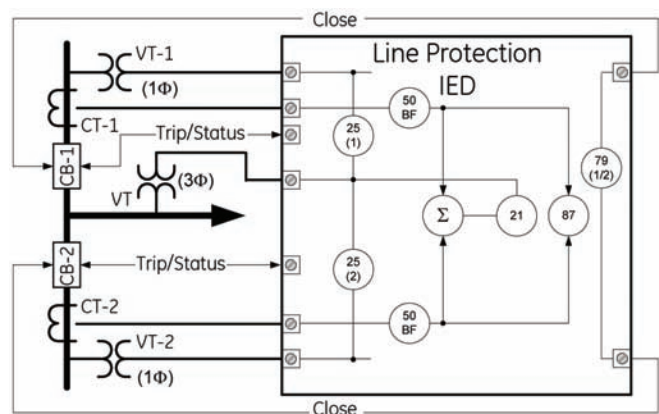


Figure 1.
Modern dual-breaker line IEDs.

Such modern IED typically support one three-phase voltage input required for the main (distance) or backup protection (distance backup on line current differential or phase comparison relays), and at least two single-phase voltage inputs in order to facilitate synchrocheck (25) across both the breakers. A dual-breaker autorecloser (79) controlling both breaker simultaneously and capable of advanced reclose modes (sequential, simultaneous, breaker out of service, etc.) completes the application. A suite of backup and auxiliary functions are typically attached to the voltages and the three currents (breaker 1, breaker 2, line).

In addition to the required AC inputs these IED are designed to support enough binary inputs (breaker status, external breaker fail initiate) and output contacts (trip for both breakers, reclose per breaker, breaker fail re-trip and trip, etc.) to facilitate protection and control of a dual-breaker line terminal from a single IED.

3. Breaker Failure Considerations

Being a backup function, the BF protection may be required to use a different CT core, an independent current path, independent relay hardware, and a separate tripping path. This requirement is naturally met when using a stand-alone BF relay, but can as well be accomplished on multi-function relays without a separate BF device, at the expense of extra signaling between the relays.

Figure 2 presents four approaches to distributing the Fault Detection (FD) and BF functions between multiple relays.

Figure (a) is a traditional scheme with a dedicated BF relay.

Figure (b) presents a simple scheme with an integrated BF function per each fault detection function. No external BFI signals are used.

Dependability is directly proportional, while security is adversely proportional, to the number of operational copies of a given

protection function. Predominately, we deploy one BF function per breaker, and the associated performance characteristics primarily in terms of spurious operations, are closely related to this practice. Currently this performance is considered satisfactory.

Wide penetration of simple integrated BF schemes that follow the approach of Figure 2a with codependency on the common signal path and relay hardware, and with 2 to 4 BF elements per each breaker, may significantly elevate the risk of large outages due to BF misoperations.

This danger can be alleviated while integrating the BF functions but at price of increased complexity.

Figure (c) shows a crosscheck scheme. Each fault detection function initiates its own BF function. This BF function is placed on the other relay so that a crosscheck is made between detecting the fault and detecting the BF condition. This scheme calls for wiring the BFI signals, and cross-monitoring of relay fail safe outputs so that upon the failure of one of the relays the other relay could switch to its own internal BF function.

Figure (d) presents a solution with a single BF allocated statically to one of the relays.

Figure (e) shows an integrated and single BF but in a switchover scheme. Normally both relays initiate the same integrated BF (one internally and one externally). Upon the failure of the relay that normally performs the BF function, the other relay switches to its own integrated BF element.

The configuration of a stand-alone BF relay (Figure 2a) fits naturally the past protection practice with external summation of CTs for the line relay. Traditional line relays did not measure the two currents individually and could not integrate the BF function for both the breakers anyway.

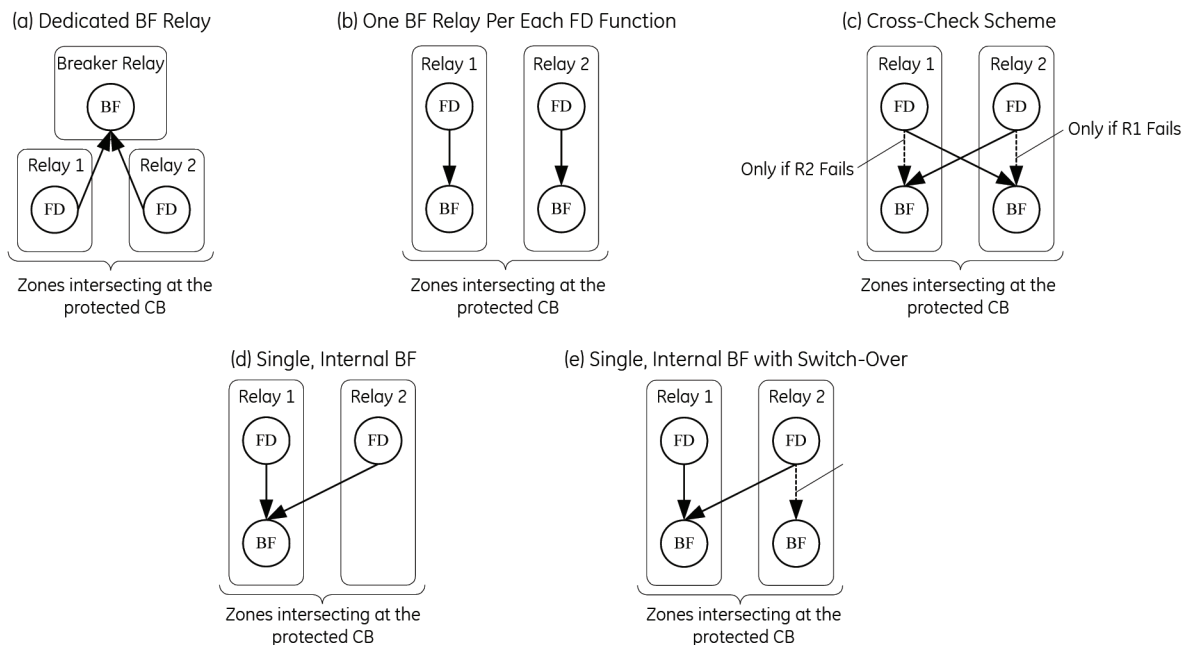


Figure 2. Allocations of the fault detection (FD) and BF functions between relays.

With modern line relays the BF for dual-breaker terminals can be integrated using any of the approaches outlined in Figure 2. For example, Figure 3a shows the “one BF per each fault detection function” approach of Figure 2b; and Figure 3b shows an implementation of the crosscheck scheme of Figure 2c.

Note that with the BF initiation from the adjacent zone for one of the two breakers, the other breaker of the dual breaker arrangement needs to be tripped. With this respect the solution of Figure 3a requires wiring the BF Trip signals while avoiding wiring the BFI signals; and solution of Figure 3b calls for wiring more BFI signals, but some BF trips are routed internally in the relays.

Advantages of integrating BF in dual-breaker applications are:

- Cost and space advantage by eliminating stand-alone Breaker Failure relay(s).
- Simplified wiring and interlocking. Every wiring termination is a potential point of failure, so reducing the amount of wiring increases reliability.
- BF simpler and easier to test thus reducing probability of spurious BF trips due to human errors during maintenance.
- More flexible initiation logic such as from voltage or frequency triggered trips.
- Easier application of multiple setting groups (banks) to adapt the BF function to changing system conditions.
- Direct access to the existing DTT/pilot channels via line relays for tripping re-mote breakers.

Disadvantages of utilizing integrated BF in dual-breaker applications are:

- Impact on security: The BF function uses same current inputs, hardware and software, and the tripping paths as the fault detection function. This minor disadvantage can be addressed by crosschecking as explained in Figures 2c and 3b.

- Impact on security: Multiple copies of the BF function operational for the same breaker potentially increase the probability of misoperation. As a backup function, the BF should not be duplicated or quadrupled. This problem can be solved by using a switchover scheme of Figure 2e or a pre-selected BF location of Figure 2d.

The above advantages and disadvantages should be weighted accordingly taking into account other factors, relaying philosophy and maintenance practice in particular. Factors to consider are:

- Preferred degree of security and reliance on remote versus local backup.
- Degree of integration of primary (fault detection) and backup (BF) functions on a single multifunction relay.
- Existing maintenance/testing practice, willingness and capacity to adjust.
- Preferences with respect to simplicity and cost targets.

4. Automatic Reclosing Considerations

Similarly to the BF protection function, the Autoreclosure (AR) control function can reside in a standalone dedicated breaker control relay, one per each breaker; or can be integrated in a multifunction line relay.

In any case, fundamental AR issues are the same; initiation, blocking, lockout, switch onto the fault logic, dead time for different types of the faults and different shot counts, tripping during evolving faults in single-pole tripping and reclosing applications, and the master-follower logic.

Proper treatment of the middle breaker is yet additional factor specific to dual-breaker applications. The middle breaker is controlled from both the line zones that intersect at the breaker.

In the case of integrated BF, multiple BF functions for the same breaker may not be viewed as beneficial from the security point of view, but are certainly acceptable as a simple solution.

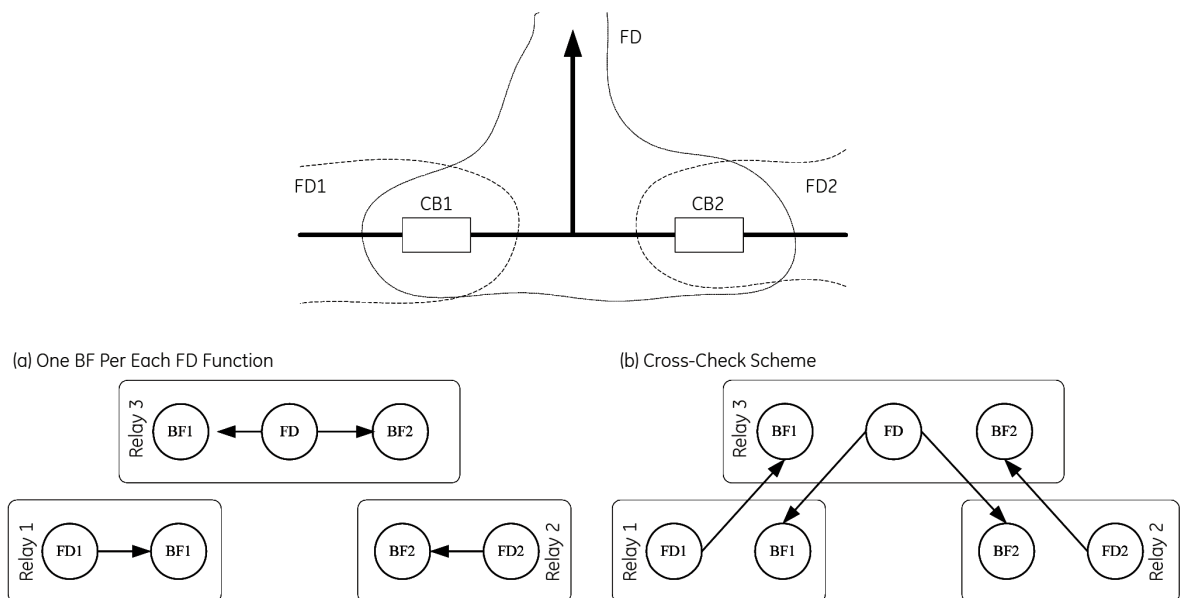


Figure 3. Selected BF schemes of Figure 2 as applied to dual-breaker line terminals.

On the other hand, multiple copies of the AR function for the same breaker are typically considered not acceptable. The AR is a complex and sequential controller. Paralleled, not synchronized instances of the AR would cause performance problems and pose testing and maintenance challenges. As a result, solutions depicted in Figure 2a (stand-alone AR), 2c (single preselected internal AR) or 2d (internal AR in a switch-over scheme or “hot stand-by”) can be considered.

The “one AR at a time” philosophy applies to multiple possible allocations of the AR function (A and B systems, 2 adjacent zones).

Beyond the common requirements ARs for dual-breaker applications should support the following features:

- Allowing choosing sequence of reclosing (1-2, 2-1 or simultaneous reclose operation).
- Ability to transfer the close command from one breaker to another if the breaker pre-selected to close first is taken out of service or failed to close.
- Ability to recognize that breaker was open prior to the line fault either manually or by adjacent protection. If used, lockout relays solve this problem. If the operational philosophy relies on the reclosers to lockout under the time-extended trip commands, the dual breaker AR needs to be designed/configured accordingly to lockout one breaker while permitting to control the other.
- If required for a given system topology, ability to check synchronism across each breaker individually, as the transmission system may become electrically isolated across each breaker and/or remote terminals.
- When required, ability to perform single-pole operation including tripping and reclosing under evolving faults considering simultaneous or near simultaneous faults on the parallel line that call for tripping and reclosing of the common (middle) breaker.

5. Protection Security under CT Saturation

Fed with externally added currents (Figure 4a) a typical line relay responds to a vectorial sum of the two local currents. If both the CTs operate with no errors, the sum of the currents is an accurate representation of the line current at this terminal. If one of the CTs saturates, the produced error signal will effectively superimpose on the true line current and cause potential problems for the protection security. The situation is particularly dangerous if the feed through the line is weak, and the CT carrying the reverse current saturates on a close in external fault (Figure 4b). A portion of the missing reverse current will leave the forward current not balanced, and appear to the relay in the forward or tripping direction.

It may appear that line current differential relays would not have problems with saturated CTs. This is true only if a given relay measures all currents of its differential zone individually and produces proper restraint or other countermeasures to the problem of CT errors. If fed with externally summated currents a line current differential relay produces the restraint signal as per its design equations based on the summation of the two local

currents. Because the relay does not respond to the individual currents, but to the sum of thereof, a combination of restrained and unrestrained differential principles is effectively applied, and as such, it may face stability problems. For example, with weak feed from the remote terminal(s), and a large through fault current along the breaker-and-a-half diameter, CT saturation errors would manifest themselves as a spurious differential current while relatively small restraint would be produced from the small, remote-end currents (high through-diameter current not seen by the relay, low through-line current seen by the relay as depicted in Figure 4b).

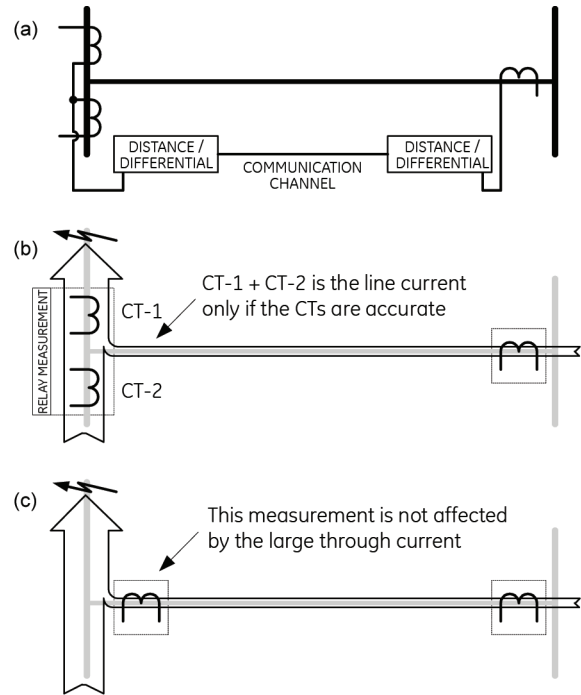


Figure 4. Dual-breaker arrangement: external CT summation (a), through fault under weak remote and strong local systems (b), through fault in a single-breaker application (c).

This problem does not exist in single breaker applications (Figure 4c). With the line current measured directly in single-breaker applications there is no danger of producing a large error signal even if the line CT saturates. If an error occurs due to CT saturation, it is properly restrained by the principle of percent differential protection.

The problem in the dual-breaker configuration demonstrates itself not only under severe CT saturation, but could become significant under relatively small CT errors, including linear errors related to the CT accuracy class. As long as the through current of the line is considerably higher compared with the error current produced by the CTs, there is no danger of the CT error signals overriding the actual through line current. When the error current is comparable with the through current, the protection system is in danger of misoperation. The through current could be low for long lines and/or when the remote system is relatively weak. The short circuit level of the local system alone controls the current flowing along the dual-breaker diameter. With the local terminal strong, and the remote terminal weak, any relay could be brought to its design limits by saturating one or more CTs on the diameter.

Distance relays are also exposed to this problem. During close-in reverse faults, the volt-age is depressed to very low levels, and stability of the relay is maintained solely by the directional integrity of the currents as measured. If, under such circumstances, CT that carries the current away from the terminal saturates (CT1 in Figure 4b), an error current appears in the direction of the line. With enough error current, the through line current becomes over-ridden, and the actual reverse fault direction may be seen as forward by the relay. As a result, with the voltage depressed and the current elevated and flowing spuriously in the for-ward direction, distance functions may pickup inadvertently. This includes a directly trip-ping under-reaching zone 1, as well as an overreaching zone 2 typically used by communication-assisted schemes. In both cases, a false trip could occur.

Current-reversal logic, application of a blocking or hybrid permissive schemes, or similar approaches, may enhance the performance and solve the problem partially. These approaches, however, often rely on a reverse-looking distance zone 4. The latter may spuriously drop out when the effective current gets inverted from the true reverse to a false for-ward direction due to CT errors. Extending the blocking action by using timers is a crude solution, but would jeopardize dependability and speed of operation on evolving external-to-internal faults.

Ground directional overcurrent functions, neutral and negative-sequence specifically – being both fast and sensitive – are good supplements enhancing performance of communication-assisted schemes [4]. They, however, face similar security problems in the dual-breaker applications. With reference to Figure 5 consider an external line-to-line fault on the diameter. In this case performance of all four CTs (A1, A2, B1 and B2) affects the neutral current. With any of the CTs saturating, a spurious neutral current will be created. There is no real neutral current through the line for this type of fault. Therefore, the operating signal for the Neutral Directional Overcurrent function is entirely driven by CT errors. The remote terminal will see the fault via its distance function and key permission to trip, unless separate pilot channels are used to key from distance and ground directional functions. Combined with the spurious operation of the neutral directional function at the local terminal, the received permission would cause a false trip.

The above problem with sensitive ground directional overcurrent functions also exists in single-breaker applications. However, in single-breaker applications the relay would measure the elevated phase currents. Modern relays allow for positive-sequence restraint in neutral or negative-sequence directional overcurrent functions, effectively solving the problem [4]. In a dual-breaker terminal with external CT summation, the positive-sequence restraint would not work.

Phase comparison relays supplied with the external sum of the currents would face the same stability problems in dual-breaker applications. Contrary to the commonly understood immunity of the phase comparison principle to CT saturation, the 87PC function requires all currents of its zone to be measured individually and included in its coincidence timing. Only by looking at the two local currents individually, a phase comparison relay would have a chance to recognize the through fault condition and develop a proper countermeasure as per the principle of phase comparison.

6. Supervision Logic for Impedance-based Protection

This section outlines a simple supervisory logic to ensure security of the main line protection during through current conditions on the dual-breaker diameter with weak feed through the line. The logic can be programmed from a number of standard Instantaneous Overcurrent elements (IOCs) and Phase Directional (Ph Dir) elements of a relay.

The supervisory logic has been developed to meet the following requirements:

- The supervision should not penalize the speed of response to internal faults (trip time) or sensitivity of the relay to high-resistance internal faults. Therefore, permission to trip should be given all the time unless a through fault condition is detected.
- Permission to trip should be maintained during transitions from load conditions, possibly a reverse load, to internal faults.
- The supervision should allow the relay to trip an evolving external-to-internal fault, in particular with both faults present at the same time, i.e. before the external fault is cleared by the associated protection system.
- The supervision should respond to elevated phase currents as the high phase currents cause CT errors and the latter could jeopardize security of the line protection. Responding to sequence components is not preferred because under evolving faults flows of negative-sequence and neutral currents may be considerably changed from expected.
- The supervision shall be easily applied to distance, differential, and overcurrent directional functions.

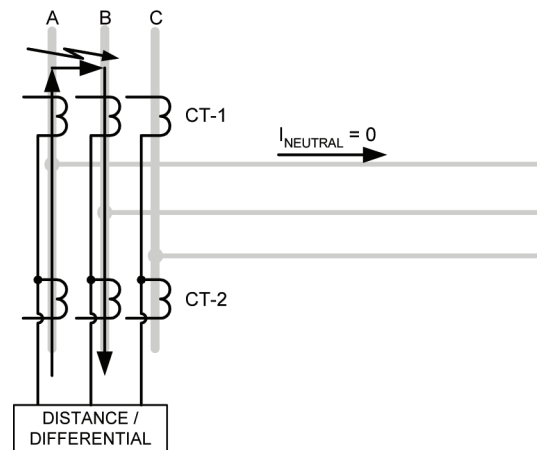


Figure 5. Danger of a spurious neutral current in a dual-breaker line application.

6.1 Protection Elements Used by the Supervisory Logic

With reference to Figures 1 and 6 the following elements are used:

- IOC 1 to respond to forward current of CT-1. The element shall be set at 2-3 times the nominal of CT-1, and is used to unblock the relay on external-to-internal evolving faults.
- IOC2 to respond to elevated current of CT-1; set at 1.5-2 times the nominal of CT-1 and used to supervise the blocking action.
- PHS DIR 1 to respond to reverse current direction at CT-1.
- IOC3 – similar to IOC1, but for CT-2.
- IOC4 – similar to IOC2, but for CT-2.
- PHS DIR 2 – similar to PHS DIR 1, but for CT-2.

The directional functions in one particular application [1-3] use quadrature polarization with memory action, if required.

6.2 Supervisory Logic

A reverse direction for CB-1 (Figure 6a) is declared if both currents are elevated (IOC2 and IOC4) and the directional element sees a reverse direction (PHS DIR 1 BLK). Similar logic is implemented for CB-2, and phases B and C. The reverse direction flags will be asserted only if an elevated current is flowing through the diameter, and the direction is re-verse in one of the breakers.

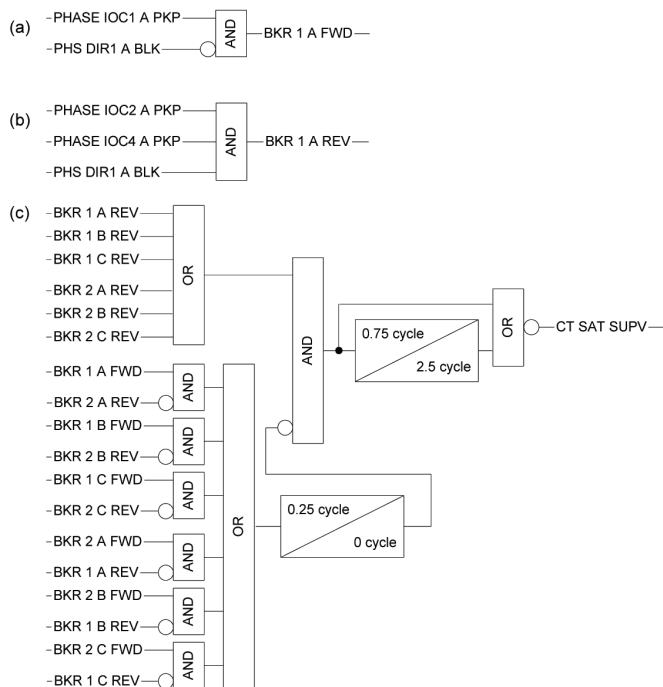


Figure 6.
Supervisory logic to cope with CT errors in the dual-breaker configuration.

A forward direction for CB-1 (Figure 6b) is declared if the current is elevated in the CB-1 leg and appears in the forward direction. Declaration of the forward direction is not impacted by the situation in the second leg of the diameter. Similar logic is implemented for CB-2, and phases B and C.

As shown in Figure 6c, the blocking action is established if any of the three phases shows a through current flowing outside of the zone, either through CB-1 or CB-2.

For security, the blocking action gets artificially extended for extra 2.5 cycles after being present for 0.75 of a cycle (switch off transient logic to cope with clearance of the external fault).

The blocking action gets cancelled if any of the currents is elevated, appears in the forward direction, and is not accompanied by the reverse direction in the other breaker in the same phase. A 0.25 cycle delay is added for security.

6.3 Performance Analysis and Explanation

During load conditions (current below some 1.5 times CT nominal) none of the IOCs is picked up and the trip permission is asserted permanently.

During internal fault conditions with very weak feed from the local terminal, the current is not elevated and may appear in the reverse direction as dominated by the load – permission is maintained as none of the IOCs picks up.

During high current internal faults, none of the directional elements operates in the re-verse direction, and the trip permission is maintained.

During external faults with one breaker opened, the blocking action is not established, but it is not needed either.

During external faults with both breakers closed, the blocking action is established as long as both the currents flowing through the diameter are above the pickup of IOC2 and IOC4.

During evolving external-to-internal faults in different phases, the blocking action is first established (phase A for example), and then canceled when the second fault appears in the forward direction in a different phase (phase B for example).

The output flag, CT SAT SUPV of Figure 6c, shall be used to supervise distance and ground directional functions of a distance relay, and the differential function of a line current differential relay, if required.

6.4. Transient Response Examples

Figure 7 presents an external fault example. The trip supervision is removed in 0.5 of a power cycle when using one particular IED [1-3] to implement the logic of Figure 6c.

Figure 8 shows an evolving fault example. The trip supervision is removed in 1 cycle after the external fault, but is re-established in 0.75 of a cycle after the fault evolves into internal.

7. Line Current Differential Solution

This section presents a description of a line current differential algorithm [5-6], but ex-tended to dual-breaker applications.

The concept [5-6] has been originally implemented for a single-breaker arrangement. In such an application, each relay [2] sends phasors of local current in all three-phases calculated using a half-cycle estimator (6 numbers) as well as dynamic terms used for adaptive restraint (3 numbers). Some extra data is appended to this core of the packet such as relay ID, virtual I/Os for teleprotection, time stamps to facilitate synchronization with the use of the ping-pong algorithm [6], GPS-driven time stamps to facilitate channel asymmetry compensation [7], CRC-check, etc.

The presented solution targets communications channels of 64kbps. The baud-rate of the channel imposes certain limitation for the packet size. Application to dual-breaker configurations calls for producing a proper restraining signal out of all the currents of the zone. For example, in three-terminal applications with each of the terminals being breaker-and-a-half or ring-bus, 6 three-phase currents surround the line differential zone. Exchanging all these currents between the terminals would increase the packet size.

The following design targets have been stated for the line current differential function capable of secure operation at multi-breaker terminals:

- The packet size should remain unchanged. A total of 9 numbers must represent currents at each terminal in terms of phasors (real, imaginary) and static and dynamic restraint factors.
- Window resizing shall be applied for fast relay operation.
- Proper restraint shall be produced to secure the differential system on external faults through the local terminal's breakers.
- Up to four currents could be used at each terminal in order to facilitate combined bus and line protection for small buses.

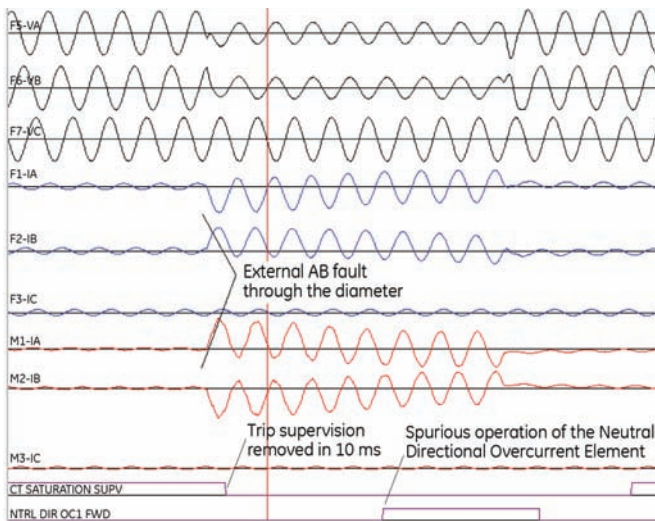


Figure 7. External Fault. Phase-to-phase fault through the diameter causes enough CT error to operate spuriously the Neutral Directional OC function. The CT logic blocks in 0.5 cycle.

- Backwards compatibility of the operating principle shall be maintained if the relay is applied in a single breaker configuration.

The following subsections address the above design constraints and goals.

7.1 Phasor Estimation

The input currents are sampled at 64 samples per cycle and pre-filtered using an optimized MIMIC filter aimed at removing dc component(s) and other low-frequency oscillations. The optimized filter is a Finite Response Filter (FIR) with the window length of approximately 1/3rd of a power system cycle.

The digitally pre-filtered currents are converted into phasors by applying half-cycle Fourier algorithm. The half-cycle values are either used as calculated, or two consecutive half-cycle measurements are combined into an equivalent full-cycle measurement. The operation of switching from full- to half-cycle upon detecting disturbance in currents is referred to as “window resizing” and is implemented to speed up operation of the relay. The differential system transmits half-cycle values, and the resizing is done independently at each terminal of the line.

Half-cycle magnitudes are also calculated and transmitted in order to reflect properly through fault conditions at each terminal of the line.

In addition “a goodness of fit” factor is calculated for each current in order to measure the error between the waveform and its Fourier-estimated phasor [7]. The goodness of fit factor is further used to produce an extra restraint to countermeasure the estimation error, and increase security of the relay. Conceptually, the goodness of fit factor is proportional to the following value:

$$\delta_{(k)} = \sum_{n=0}^{N-1} \left| x_{(k-n)} - X_{(k)} \cdot \cos\left(\frac{2 \cdot \pi \cdot n}{N} + \Theta_{(k)}\right) \right|^2 \quad (1)$$

In equation (1), the present magnitude and phase estimate (X,Q) at the k-th sample is compared with the actual waveform (x) over the duration of the data window (N), and the sum of squares error measure is calculated.

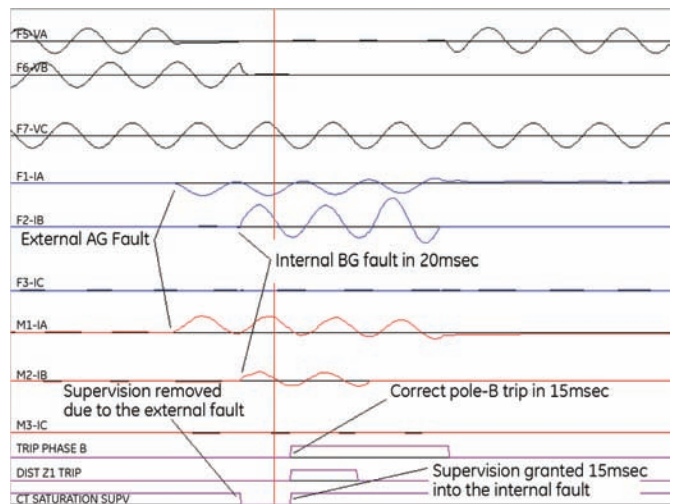


Figure 8. External-to-Internal Evolving Fault Example. The relay trips single-pole the correct phase despite the pre-existing external fault. The CT logic unblocks in 0.75 of a cycle.

7.2. Consolidating Local Currents – the Outgoing Packet

Each terminal of the current differential system consolidates the local signals into an outgoing packet. Compression of information takes place in order to reduce the packet size and distribute the calculations between the two or three relays of the line current differential system. This is possible without compromising operating equations or accuracy if the operating equations are shaped accordingly.

First, the phasors (real, imaginary) of all the local currents are summated to give a sub-sum of the total differential current of the protected line:

$$I_{LOC_RE_A} = I_{1_RE_A} + I_{2_RE_A} + \dots \quad (2)$$

Equation (2) is applied to up to four local current inputs and holds true for both real and imaginary parts, in all three phases. Equation (2) is not a differential current, but a portion of the differential current that involves the local currents only.

Second, the measure of a through fault current is estimated locally using magnitudes of all the local currents via the following equation:

$$(I_{LOC_TRAD_A})^2 = \max((I_{1_MAG_A})^2, (I_{2_MAG_A})^2, \dots) \quad (3)$$

Equation (3) selects, on a per phase basis, the largest among the local currents to be a measure of the local restraint.

Figure 9 illustrates the principles behind equations (2) and (3).

Third, the protection system applies differential characteristic locally to each of the re-restraining currents. The presented system does not use an explicit restraining characteristic, but the total operating and restraining value [5-6]. The latter incorporates values of the pickup, slopes (S_1 , S_2) and breakpoint (B). The following equations are used to accommodate the characteristic:

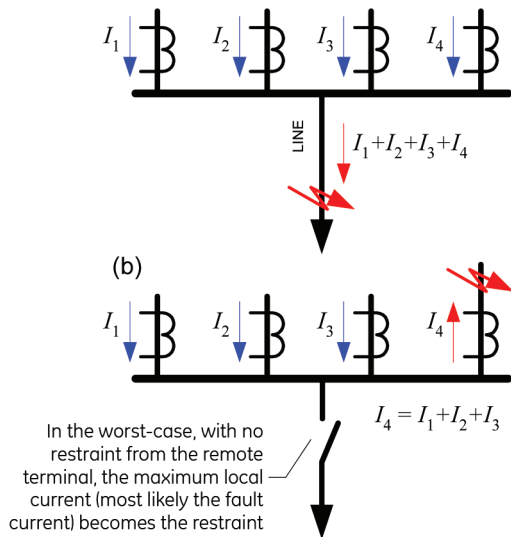


Figure 9. The differential current is created from partial sums of all the local currents (a). The restraining current is created based on the maximum local current (b).

- In two-terminal applications:

$$\text{If } (I_{LOC_TRAD_A})^2 < B^2$$

Then

$$(I_{LOC_REST_TRAD_A})^2 = 2 \cdot (S_1)^2 \cdot (I_{LOC_TRAD_A})^2 \quad (4a)$$

Else

$$(I_{LOC_REST_TRAD_A})^2 = 2 \cdot ((S_2)^2 \cdot (I_{LOC_TRAD_A})^2 - (S_2 \cdot B)^2) + 2 \cdot (S_1 \cdot B)^2 \quad (4b)$$

- In three-terminal applications:

$$\text{If } (I_{LOC_TRAD_A})^2 < B^2$$

Then

$$(I_{LOC_REST_TRAD_A})^2 = \frac{4}{3} \cdot (S_1)^2 \cdot (I_{LOC_TRAD_A})^2 \quad (4c)$$

Else

$$(I_{LOC_REST_TRAD_A})^2 = \frac{4}{3} \cdot ((S_2)^2 \cdot (I_{LOC_TRAD_A})^2 - (S_2 \cdot B)^2) + \frac{4}{3} \cdot (S_1 \cdot B)^2 \quad (4d)$$

The adaptive portion of the restraint is a geometrical sum of errors derived from equation (1) and a measure of the clock synchronization error [5-6]. The traditional and adaptive restraints are combined geometrically using a concept of an extra arbitrary multiplier:

$$I_{LOC_RESTRIANT_A} = \sqrt{(I_{LOC_REST_TRAD_A})^2 + MULT_A \cdot (I_{LOC_ADA_A})^2} \quad (5)$$

The multiplier increases the impact of signal distortions on the restraint, and is used to provide better restraint during CT saturation conditions on through line faults.

Values defined by equations (1-5) are based on half-cycle windows, and constitute the following outgoing packet:

$$I_{LOC_RE_A}, I_{LOC_RE_B}, I_{LOC_RE_C}, I_{LOC_IM_A}, I_{LOC_IM_B}, I_{LOC_IM_C}, \dots \\ \dots, I_{LOC_RESTRIANT_A}, I_{LOC_RESTRIANT_B}, I_{LOC_RESTRIANT_C} \quad (6)$$

7.3 Total Differential and Restraint Currents

The local and remote data when received are used to calculate the total differential and restraining signals for the current differential system.

Before the data is used, a decision is made to either use the full- or half-cycle measurements. The half-cycle data is used one time after detecting a fault. After such half-cycle window is used, the relay switches back to the full-cycle version when proceeding into the fault. Also, when a packet is lost, the next packet that arrives triggers window resizing. This is simply to enable protection using the latest packet even though the previous packet required to calculate the full-cycle quantities is lost due to the communication channel impairments.

The following equations are used to combine the half-cycle values into full-cycle measurements:

$$I_{LOC_PHASOR_RE_A} = 0.5 \cdot (I_{LOC_RE_A(present)} + I_{LOC_RE_A(previous)}) \quad (7a)$$

$$(I_{LOC_PHASOR_RESTRAINT_A})^2 = 0.5 \cdot [(I_{LOC_RESTRAINT_A(present)})^2 + (I_{LOC_RESTRAINT_A(previous)})^2] \quad (7b)$$

Equation (7b) is accurate; equation (7b) is a good approximation. Equations (7) apply to both local and remote signals, all three phases, and real and imaginary parts.

Next, the relay calculates the total differential and restraint currents:

$$I_{DIFF_RE_A} = I_{LOC_PHASOR_RE_A} + I_{REM1_PHASOR_RE_A} + I_{REM2_PHASOR_RE_A} \quad (8a)$$

$$(I_{REST_A})^2 = (I_{LOC_PHASOR_RESTRAINT_A})^2 + (I_{REM1_PHASOR_RESTRAINT_A})^2 + (I_{REM2_PHASOR_RESTRAINT_A})^2 \quad (8b)$$

And applies the so-called fault severity equation in order to decide if the line should not be tripped [5-6]:

$$S_A = (I_{DIFF_A})^2 - (P^2 + (I_{REST_A})^2) \quad (9)$$

The relay (87L function) operates if the fault severity, S, is positive.

P is the pickup of the characteristic (the slopes and breakpoints were already accommodated before sending the data in equations (4)).

As indicated by all the equations, the algorithm is fully phase-segregated.

7.4 CT Saturation Detection

The algorithm has a built-in immunity to saturated CTs owing to the concept of the dynamic restraint. The goodness of fit (1) becomes degraded on saturated waveforms, producing a measure of error (1), which added to the restraining signal allows for extra security.

In order to boost this natural effect, the system is using an adaptive multiplier in order to increase further the impact of the dynamic portion of the restraint (5) on the overall performance of the relay.

The multiplier is calculated adaptively per phase as follows:

$$MULT_A = \max(MULT_{1A}, MULT_{2A}) \quad (10)$$

The first component is based on local currents only, and as such is instantaneous. This component is meant to detect through fault condition on the local diameter of the breaker-and-a-half or ring-bus configuration.

The second component is based on local and remote currents, and as such is lagging the real time by the channel propagation time. This component is meant to detect through fault conditions between terminals of the line.

The first multiplier is calculated as follows:

Step 1. Select the greatest current from the local currents. The selection is based on half-cycle magnitudes: I1_MAG, I2_MAG, I3_MAG, I4_MAG. Assume the largest current is in the k-th circuit (k = 1,2,3 or 4).

Step 2. Calculate two auxiliary currents:

$$I_{X_RE} = I_{k_RE} \quad (11a)$$

$$I_{X_IM} = I_{k_IM} \quad (11b)$$

$$I_{Y_RE} = I_{1_RE} + I_{2_RE} + I_{3_RE} + I_{4_RE} - I_{X_RE} \quad (11c)$$

$$I_{Y_IM} = I_{1_IM} + I_{2_IM} + I_{3_IM} + I_{4_IM} - I_{X_IM} \quad (11d)$$

The X-current is the maximum current among the local currents. The Y-current is the sum of all the local currents but the maximum current. Note that during through faults with no feed from the remote terminals IX = -IY if no CT saturation. With CT saturation the currents differ, but remain approximately out of phase.

Step 3. Calculate the multiplier as follows:

$$\text{If } |I_X| > 3pu \quad \& \quad |I_Y| > 3pu \quad (12a)$$

$$\text{Then } \text{abs}(\text{angle}(I_X, I_Y)) > 90^\circ \quad (12b)$$

$$\text{Then } MULT := \text{abs}(\text{angle}(I_X, I_Y)) \cdot \frac{5}{180^\circ} \quad (12c)$$

$$\text{else } MULT := 1 \quad (12d)$$

$$\text{Else } MULT := 1 \quad (12e)$$

Equations (12) check if both currents (the maximum among the local currents, and the sum of all the other local currents) are large enough to cause significant CT saturation. If so, the relative direction of the two currents is checked. If the angle is less than 90 degrees, the multiplier stays at the "neutral" value of 1.00. If the angle is larger than 90 degrees, the multiplier is proportional to the angle difference and could reach the maximum value of 5.00 if the currents are exactly out of phase.

The second multiplier is calculated applying exactly the same procedure, but instead of using local currents, the procedure uses the sum of the local currents, and the remote currents. In other words the currents into the line at each of up to three terminals of the line, regardless of the number of local currents at each terminal of the line. The second multiplier detects through fault conditions of the entire line.

Figure 10 illustrates operation of the presented algorithm under through fault conditions. In this example the traditional restraint of 15pu, is additionally augmented by adding the dynamic factor. The dynamic restraint is naturally increased by saturated CT, and artificially multiplied by the multiplier. In this example, the T3 terminal sees CT saturation in the circuit carrying the current out of the line toward the fault. This CT saturation will jeopardize stability of all terminals. However, all terminals will use high values of the multiplier to boost the effect of dynamic restraint, and will not misoperate.

7.5 Field Example

A permanent AG fault occurred on line L2 in the system of Figure 11. The line was tripped and reclosed from the A2 breaker. Shortly after a line current differential relay protecting the L1 line misoperated. Note that this installation used line current differential re-lays fed with externally summated currents.

Figure 11 shows traces of the phase A currents at both ends of the L1 line. The remote end current is not distorted. The local current is heavily distorted and suspicious. Detail analysis reveals that the A1 and A2 breakers carried about 22kA of fault current, or $22\text{kA}/0.8\text{kA} = 27.5$ times rated when A2 closed onto the fault. The CTs saturated quickly due to a combination of large ac current, remnant flux due to the original fault, and dc off-set. The through current in the L1 circuit was only 1.36kA. Relatively minor errors of the CTs carrying 22kA augmented considerably the true “1.36kA reverse” signal causing a false operation.

The remote end relay measured $1.36\text{kA} \angle -20^\circ$ (correct) while the local relay measured $1.77\text{kA} \angle -112^\circ$ (incorrect, due to CT saturation).

As a result, the differential signal appeared to be 2.19kA. The restraining signal calculated by the relays was 1.73kA (assuming a pickup of 0.16kA and a slope setting of 50%). The operating (differential) signal was far above the restraining signal, hence the spurious trip.

Should the L1 relay at the A terminal be deployed in a dual-breaker manner, and measured the A1 and A2 current separately, it would apply the restraint of:

$$0.16\text{kA} + 0.5 * (\max(23.3\text{kA}, 21.9\text{kA}, 1.36\text{kA})) = 11.8\text{kA}.$$

The above restraint is several times higher than the operating signal resulting in no operating for this external fault case.

8. Phase Comparison Solution

As explained in section 5, phase comparison principle would face security problems when fed from externally summated currents in dual-breaker applications. In order to maintain the excellent immunity to CT saturation of the original (“single-breaker”) phase comparison principle, one needs to process the two currents individually and use both the phase and magnitude information to detect the through fault condition.

The dual breaker logic consolidates two pieces of information: fault detector flags signaling the rough current levels, and the “phase” pulses signaling current direction [8].

The fault detector flags (Fault Detector Low and Fault Detector High) are OR-ed between the two breakers (breakers 1 and 2):

$$FDL = FDL_1 \text{ OR } FDL_2, \quad FDH = FDH_1 \text{ OR } FDH_2 \quad (13)$$

The rationale behind it is that regardless which breaker, or both carry a current; the elevated current condition (FDL) shall be declared to signal permission or blocking as per the scheme type, and fault location; similarly with the trip supervision condition (FDH).

It is the “pulse” combination logic that ensures security and dependability of the 87PC function. With this respect a distinction must be made between tripping and blocking schemes.

For tripping (permissive) phase comparison schemes, a positive polarity is declared for the terminal if one breaker displays positive polarity when its FDL flag is set, while the other breaker either does not show the negative polarity or its FDL flag is dropped out (Figure 12a). This is similar to a Hybrid POTT scheme when a given terminal sends a permissive signal unless is restrained locally by a reverse fault condition. Note that this logic displays the following desirable features:

- Under through fault conditions, when both currents are elevated and out of phase, the positive pulses in one breaker get “erased” by the negative pulses in the other breaker.
- Under reverse or forward fault with one breaker opened or its current below the lower fault detector, the logic behaves as for a single breaker. The elevated current in the closed breaker drives the response of the scheme. In this way a small out-feed can be tolerated and will not impair dependability of the scheme.
- Under forward fault with both breakers closed and both currents above the fault detection level, the two-breaker logic effectively creates a coincidence pulse out of the two individual pulses (logical AND). This corresponds to a multi-terminal phase comparison where all individual current pulses are AND-ed before feeding the trip integrators.

The above logic is used for keying in permissive schemes, and regardless of the scheme type for derivation of local pulses sent to the trip integrators of the phase comparison relay.

Transmission logic for the blocking logic follows a different reasoning (Figure 12b). Here, a blocking action must be established if any of the two breakers sees a reverse direction. It must be kept in mind that the positive and negative pulses do not necessarily complement each other, and therefore one must not substitute the “not positive polarity” by “negative polarity”.

Figure 13 shows a sample response of the permissive logic to a through fault condition at a two-breaker terminal. The terminal does not produce permissive pulses and inhibits as expected.

Figure 14 shows a case of an internal fault with strong feed from both the breakers.

More information on modern implementations of the phase comparison principle, including dual-breaker applications and the CT saturation issue, can be found in [8].

9. Stub Bus Protection and Issues

In dual-breaker applications a line disconnect can be opened while the two breakers are closed to facilitate continuous service of other circuits. At the same time the line may be energized from the other end or ends, to service tapped loads or transmit power between the other two line terminals (Figure 15).

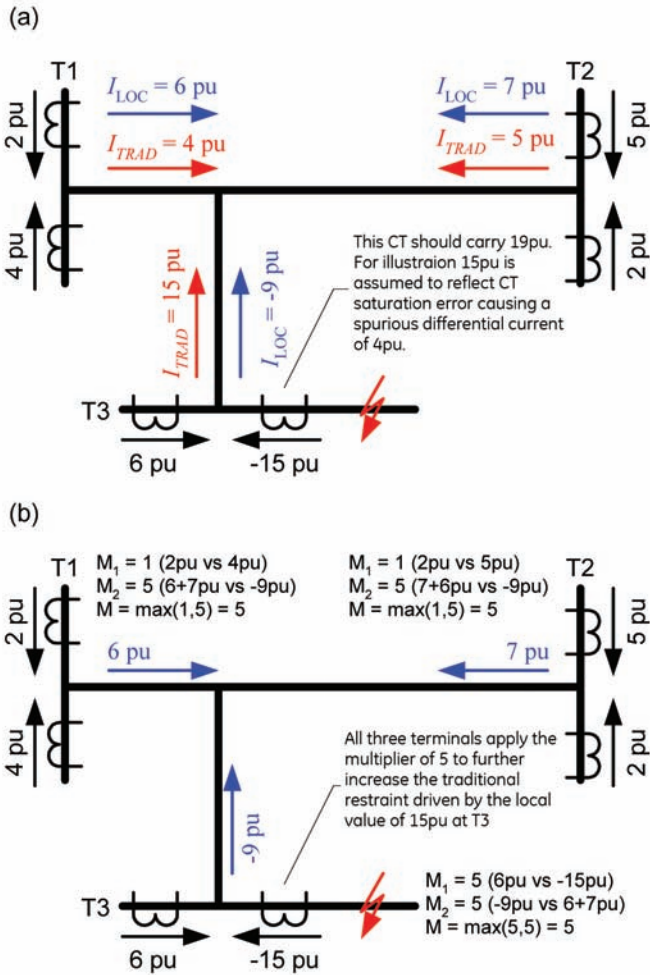


Figure 10.
 An example of calculating the restraints (a) and multipliers for CT saturation algorithm (b).

Under such circumstances the following needs to be assured:

- The stub bus zone between the two breakers and the opened disconnect is properly protected. In single-breaker application a simple overcurrent function supervised with the “disconnect opened” signal is sufficient. In dual-breaker applications such simple solution would face security problems under through fault conditions and saturated CTs as explained in section 5. Either a differential-type stub bus protection is implemented with the use of proper restraint to counterbalance the impact of saturated CTs, or the supervisory logic presented in section 6 is adopted for trip-ping.
- When tripping on stub bus faults, no DTT is to be sent to the remote end(s) as they are already isolated from the fault by the opened disconnect switch. Upon failure of one of the breakers, no BF trip is to be sent to the remote ends either.
- A fault in the stub bus zone must not result in tripping the remote line terminals. Solutions to this requirement depend on the applied protection principle, as explained below.
- Permissive directional comparison schemes typically do not have a problem. A permanent permission is keyed under the circumstances (disconnect opened while the breakers are closed); an echo scheme is used; or an overreaching zone

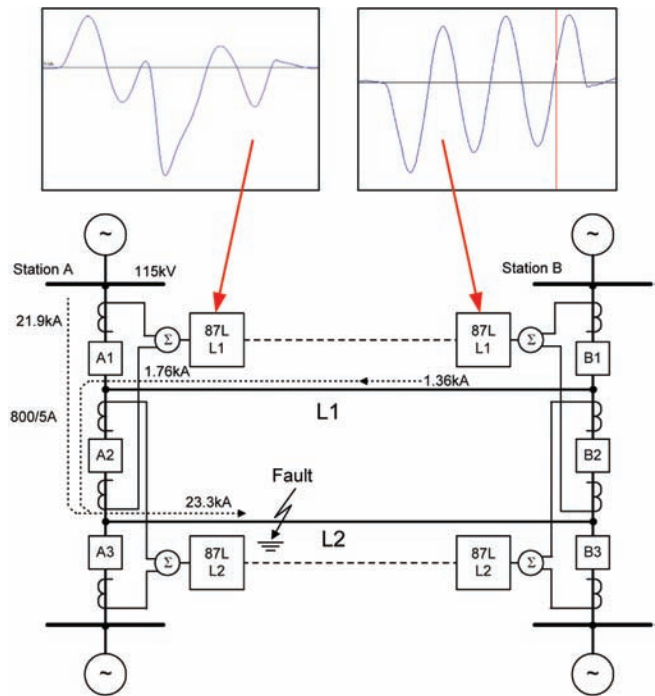


Figure 11.
 System configuration for the presented filed case.

1 is applied at the remote end under the circumstances. In three-terminal applications or with tapped loads, it may happen that the remote end will “see” the fault in the stub bus zone despite the opened disconnect (Figure 16). This creates security problems if permanent permission or an echo scheme is used. If the fault current closes through the third line terminal, no permission will be sent from that terminal. But if the line closes via an unmonitored tapped load, the problem remains. Avoiding too sensitive overreaching functions at the remote end solves the problem.

- Under the circumstances blocking directional comparison schemes are practically equivalent to permissive schemes with permanent permission or echo as described above. Making sure the overreaching forward looking fault detectors never pickup for faults in the stub bus zone solves the problem.
- With the respect of the stub bus protection and application phase comparison relays can be dealt with as the same way as direction comparison schemes.
- Line current differential schemes require the relay under the stub bus condition to transmit zero currents regardless of its actual measurements. In this way under the stub bus fault, the 87L function will not trip the line at the remote terminal(s).

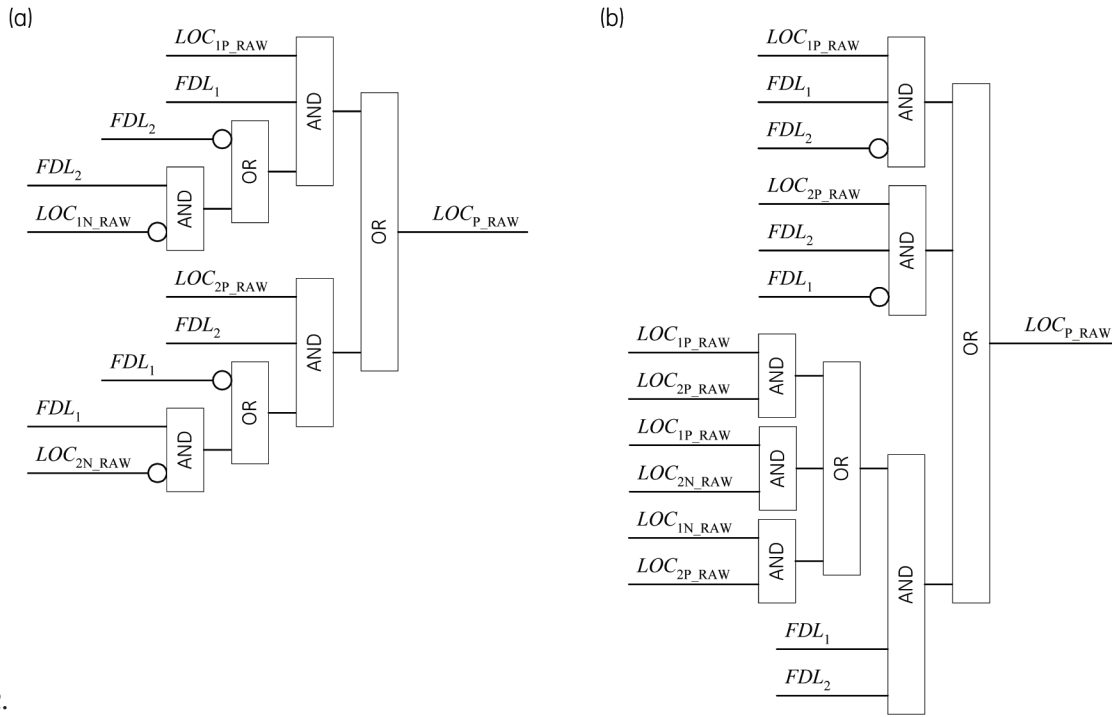


Figure 12.
Dual-breaker logic for the phase comparison relay [8]:
Permissive (a) and blocking (b) transmit schemes.

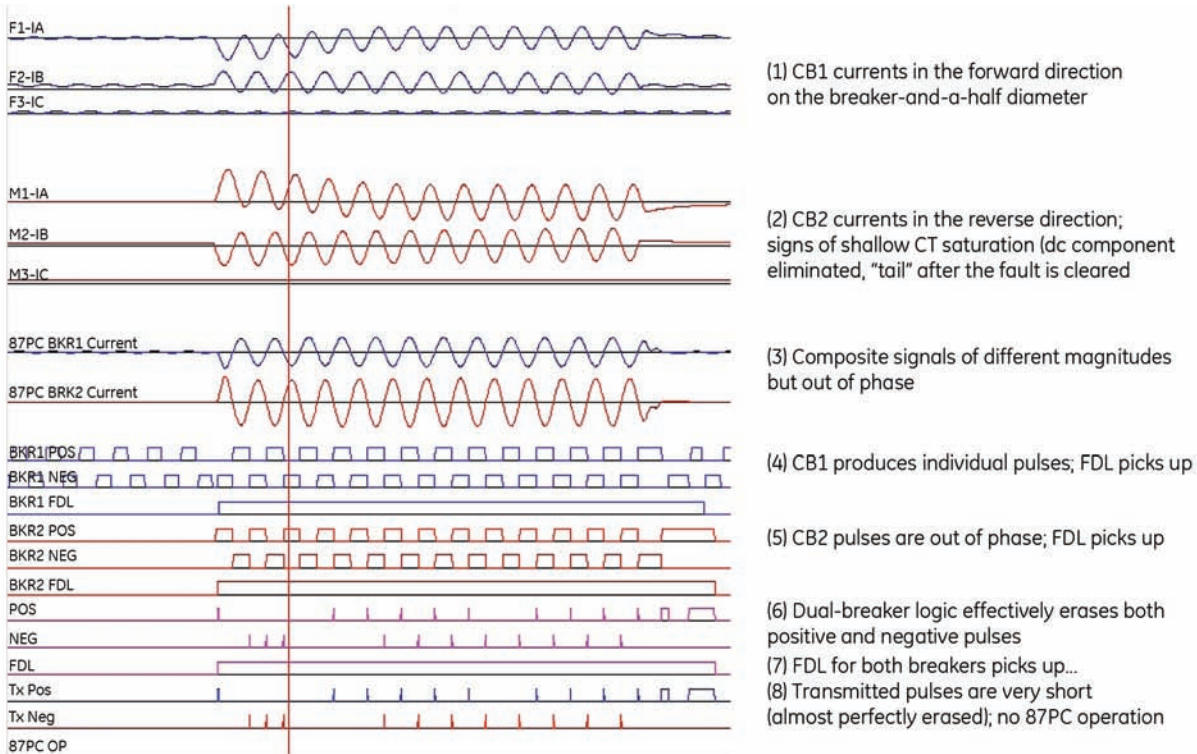
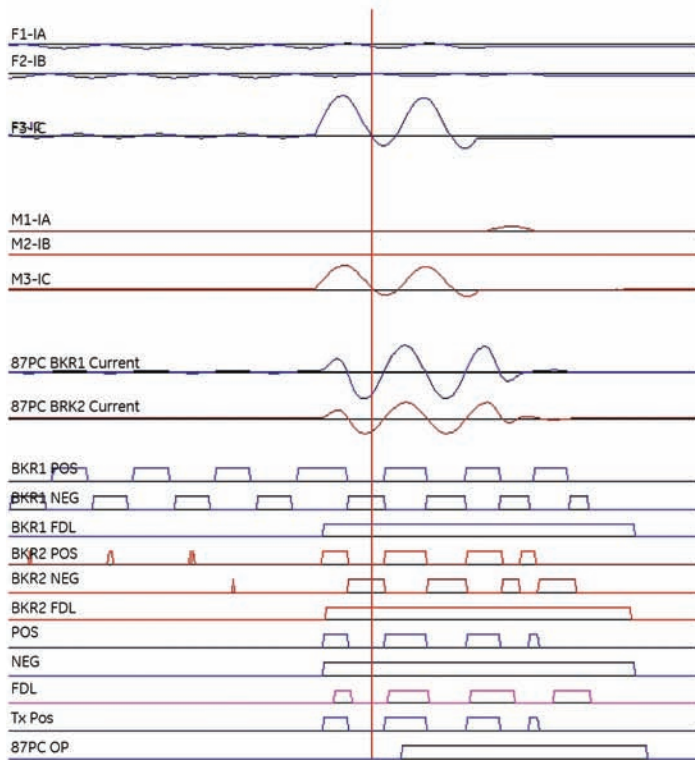


Figure 13.
Illustration of the dual-breaker logic: permissive, dual-comparison scheme, through fault condition (relay [3] COMTRADE record).



- (1) CB1 currents (internal CG fault)
- (2) CB2 currents
- (3) Composite signals of different magnitudes but out of phase
- (4) CB1 picks up its FDL and produces its positive and negative pulses
- (5) CB2 picks up the FDL; its pulses are in phase with the CB1 currents
- (6) Dual-breaker logic yields the two set of pulses coincided (logical AND); FDL picks for the entire terminal
- (7) Received and transmit signals
- (8) Trip on the second coincidence; first RX too short

Figure 14. Illustration of the dual-breaker logic: permissive single-comparison scheme, internal fault condition (relay [3] COMTRADE record).

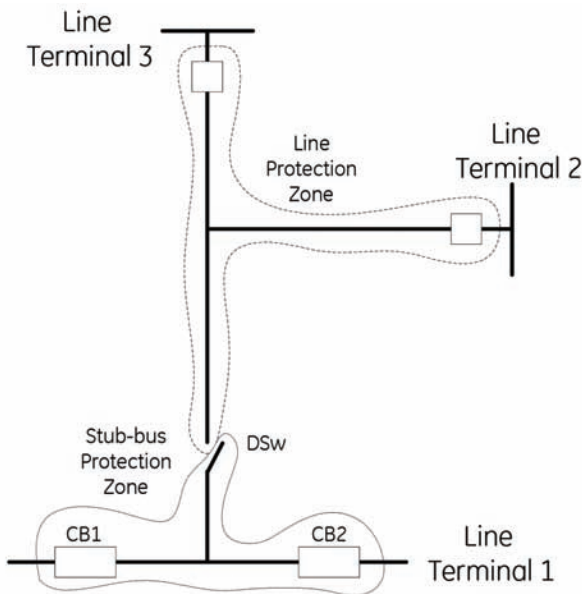


Figure 15. Stub bus situation (three-terminal line).

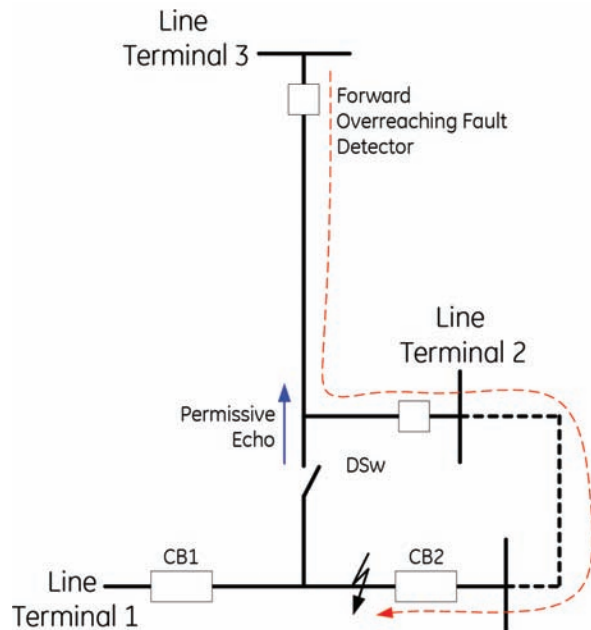


Figure 16. Example of fault detectors too sensitive and causing problems under remote stub bus faults.

10. Conclusions

This paper presents practical application solutions for protection of lines in dual breaker applications.

Integration of breaker failure and autoreclose is discussed first.

Next a problem of stability under CT saturation when using externally summated currents for protection is described.

A simple supervisory logic that could be implemented on modern line relays is presented to ensure security under CT saturation during through faults on the breaker-and-a-half or ring-bus diameter.

A novel line current differential system is described suitable not only for dual-breaker configurations, but also for applications with up to four local inputs at each of the up to three terminals of the line. The solution is designed to produce correct restraining signal as per the principle of differential protection without sending all the raw local currents between all terminals of the line.

Phase comparison algorithm addressing the security concern related to CT saturation in dual-breaker applications is also presented.

Finally notes are included on stub bus protection as related to dual-breaker applications.

Modern multi input multifunction line protection relays allow more sophisticated applications on dual-breaker line terminals.

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A Utility's Experience in the Implementation of Substation Automation Projects

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1. Introduction

eThekweni Electricity has embarked on substation automation projects since the early introduction of substation specific communications standards and is presently in the process of implementing substation automation projects based on the IEC61850 standard at eight new substations.

This paper describes actual substation projects to illustrate the evolution of the introduction of substation automation in terms of objectives, applicable standards and specification methodology. Positive and negative outcomes of the various evolutionary phases are highlighted.

The positive and negative outcomes of the use of substation automation solutions for the various projects are discussed and compared with the initial objectives. The paper concludes with the envisaged adoption of the full IEC61850 model for substation automation.

2. History

Prior to 2000, eThekweni Electricity substations were designed with the protection and control arrangement shown in Figure 1.

All signals were transmitted between the primary plant and the protection and control system by means of hard-wired secondary cabling. Protection and control panels located in control rooms were equipped with protection relays, panel mimics and control switches. The primary plant and protection and control panels were hard-wired to a supervisory remote terminal unit (RTU) via a supervisory junction board. The RTU was networked to eThekweni Electricity's supervisory control and data acquisition (SCADA) system. After the introduction of microprocessor based protection relays with communications facilities, simple multi-drop networks were included to permit remote protection setting and engineering.

The protection and control system was normally included with one of the primary plant contracts and the secondary cabling and testing carried out by the applicable primary plant contractor.

While this arrangement provided most of the protection, control and monitoring functionality required of the more modern substation automation systems, it suffered from several disadvantages. The arrangement is not easily factory tested and is susceptible to on site wiring errors resulting in longer commissioning times. The secondary cabling is time consuming and costly to install. The provision of protection and control systems via a primary plant supplier often led to problems due to the indirect relationship with the system supplier.

During the 1990's bay controllers and protection relays with inherent bay control functionality became available. These products could provide SCADA functionality by being networked with an RTU master, which could act as a data concentrating SCADA RTU. The main drawback of these systems was that they predominantly used proprietary communications protocols that were limited to the "master/slave" topography. Each manufacturer's system was unique with the result that utilities would either be locked into the use of one manufacturer's product or would need to have the resources to maintain many unique solutions, each of which could only be extended by that particular manufacturer's products.

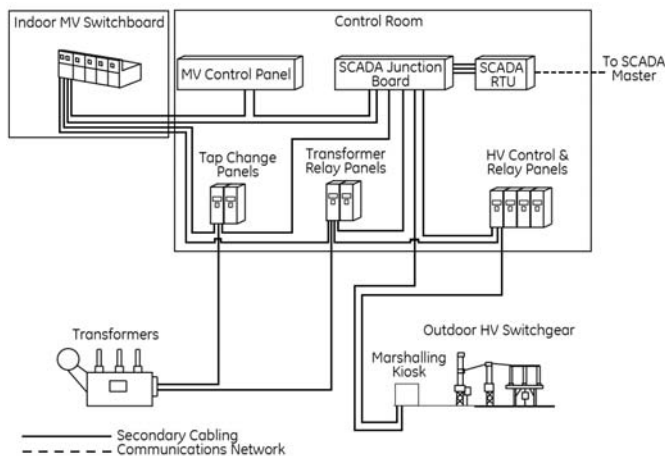


Figure 1.
Legacy protection and control automation.

While eThekweni Electricity recognized the potential benefits offered by the use of communication networks to replace hard-wired secondary cabling, the problems associated with the use of proprietary protocols resulted in the decision to maintain the status quo. During the late 1990's products that made use of a "standard" communication protocol (UCA2.0) over a standard physical layer (Ethernet) became available. Work on the IEC61850 standard had commenced but was far from complete. Based on the assumption that much of the UCA2.0 protocol would find its way into the IEC61850 protocol and that the IP transport layer and Ethernet physical layer would definitely be used for IEC61850, two pilot projects using communication networks between protection relays for substation automation were embarked upon.

3. Pilot Project 1 :

3.1 Quarry 132kV Switchyard

In 2000, a tender was advertised for a 132 kV switchyard consisting of eight 132kV feeder bays. The protection and control aspect of the specification was based on a non-networked, hardwired ("legacy") system and "legacy" wiring schematics were used to indicate the requirements. Tenderers were requested to offer a UCA2.0 based solution and to rationalise the "legacy" arrangement accordingly.

The solution provided made use of a combination of the UCA2.0 and DNP3.0 protocols. UCA2.0 was used to implement peer-to-peer messaging (UCA GOOSE or GSSE) for interlocking and tripping purposes. The Ethernet physical layer for UCA2.0 was also used for protection setting and engineering. A DNP3.0 master/slave network over RS485 was used for SCADA purposes. The solution did not make use of a human machine interface (HMI) computer. A traditional mimic and control switches were provided as part of the protection panels.

While the solution provided the required functions perfectly, several important lessons were learned from this pilot project:

- The use of "legacy" protection and control specifications and drawings resulted in requirements being misinterpreted and philosophy decisions needing to be made by the system integrator.
- The SCADA RTU selected for this project was provided by the existing SCADA Master Station supplier and did not have a means of communicating with the protection relays using TCP/IP over Ethernet. Although the relays were capable of communicating using UCA2.0 or DNP3.0 over Ethernet, the final solution used DNP3.0 over RS485. There were products from other manufacturers available that could have used DNP3.0 over Ethernet and so minimized wiring.
- GOOSE messaging was used for trip and breaker-fail signals between the Busbar Protection scheme and feeder bays. This required a dual redundant Ethernet network for reliability purposes with associated additional costs. The use of GOOSE messaging resulted in there being no simple means of isolating Busbar Protection and associated Breaker Fail tripping which is normally required when testing on a live system. The reliability and speed of GOOSE messaging was, however, proven. The objective of minimizing on-site secondary cabling was achieved in this project.

4. Pilot Project 2 :

4.1 Plangweni 132/11kV Substation

In 2002, tenders were advertised for a 132/11kV substation consisting of two 132kV bays, two 132/11kV 30MVA transformers and an eighteen panel indoor 11kV switchboard. A Protection tender was advertised separately from the primary plant tenders for the first time in order that a "first-hand" relationship could be established with the Protection supplier and to ensure that the overall responsibility for the substation automation system remained with a single party. Protection relays were free issued to the 11kV switchgear supplier for installation in the 11kV switchboard.

A new Protection And Control specification was drawn up from scratch for this project. An arrangement similar to that shown in Figure 2 was specified.

The specification called for a Human Machine Interface (HMI) computer to provide substation control of primary plant and a SCADA Gateway to facilitate remote control. The HMI and the SCADA Gateway were required to communicate with protection relays over an Ethernet physical layer. As the IEC61850 standard had not yet been published, the HMI was specified to make use of the UCA2.0 protocol and the SCADA Gateway was specified to make use of the DNP3.0 protocol. The protection relays were required to handle these protocols simultaneously over Ethernet.

UCA2.0 was also specified to provide peer-to-peer messaging (UCA GOOSE or GSSE) for interlocking and indication. Peer-to-peer messaging was not used for protection tripping due to the lessons learnt in Pilot Project 1. Protection setting and engineering were required to be carried out over the Ethernet physical layer.

Due to the dramatic reduction in secondary cabling, the Transformer Protection and Tap Change Control schemes were specified to be accommodated in one physical panel.

In an attempt to reduce the cost of protection relays and the communications network, the use of one protection relay to provide protection and control for more than one 11kV feeder was allowed. A multi-feeder system comprising one relay for three 11 kV feeders was offered and accepted.

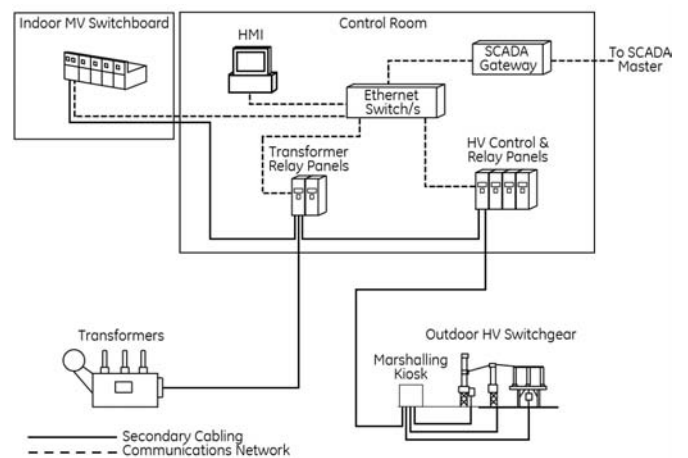


Figure 2. Present protection and control arrangement.

The supplier provided a system compliant with the specification and, for the first time, all communication within a substation (other than time synchronisation) was provided by one physical network. The main objective of minimizing hardwired secondary cabling had been achieved. The number of panels to be accommodated in the control room was vastly reduced allowing the physical size of the control room to be reduced.

The lessons learned from this pilot project were:

- The HMI hardware failed shortly after commissioning apparently due to over-heating. This was despite the specification calling for an “industrial grade” PC. The hardware was replaced but concerns remain over its expected lifespan in comparison with the remainder of the equipment supplied.
- A conventional office/home operating system or a UNIX based operating system were specified as options for the HMI. The conventional home/office operating system was offered and accepted. This operating system has proved unreliable.
- The HMI software used an unproven third-party UCA2.0 driver arrangement which has been unreliable. On many occasions when the system has been left unattended for a number of weeks it has been found in a “crashed” state by operators.
- The arrangement of one protection relay providing protection and control for more than one 11kV feeder was found to be limiting in terms of the allocation of electricity customers and distributor substations to feeder circuits. Customers and distributor substations were required to be fed on circuits which did not share a protection relay to avoid protracted loss of supply for a common source of failure.

5. Development of a specification for substation automation project based on IEC61850

During 2005, a specification was developed for Protection And Control equipment for eight new substations. The specification for Pilot Project 2 was used as a basis, but was modified to conform to the IEC61850 standard and to eliminate problems identified in the pilot projects. The main features and philosophies are detailed below:

6. Scheme Drawings

Traditionally, tender drawings showed proposed wiring schematics with discrete functional devices to convey protection and control philosophy. These drawings were used by suppliers to develop protection and control schemes using their products.

With the introduction of microprocessor based relays, much of the protection scheme functionality was programmed into the relays instead of being implemented with discrete wired components. With modern substation automation systems virtually all of the scheme functionality is programmed into the relays and only inputs and output contacts are physically wired. Scheme drawings were thus split into wiring schematics and logic schematics.

Wiring schematics were used to indicate all hard-wired connections between the protection and control schemes and the primary plant. These included analogue inputs such as CT's and VT's, digital inputs such as switchgear auxiliary switches and alarm contacts and contact outputs for closing and tripping switchgear. These wiring schematics were also used for the primary plant specifications.

Logic schematics showed how inputs and protection functions were to be marshalled through logic gates, latches and timers to operate virtual and contact outputs. These schematics also indicated which logical nodes need to be linked to the HMI and the SCADA Gateway and which were to be available for peer-to-peer links (GOOSE messages).

Issuing logic schematics with the specification proved to be invaluable when addressing queries and approving protection designs.

7. Communications Arrangement

The specification called for an arrangement similar to that for Pilot Project 2, shown in Figure 2. The HMI computer and SCADA Gateway were to communicate with protection relays by means of the IEC61850 protocol over the Ethernet physical layer. Peer-to-peer (GOOSE) messaging was to be carried out according to IEC61850. Protection setting and engineering were required to be carried out over the Ethernet physical layer and could make use of an alternative standard protocol.

All Ethernet links to protection relays were to be by means of optic-fibre (100baseF). The Ethernet switches were required to be suitable for use in a substation environment. They were to have no moving parts such as fans and be powered from the substation battery.

Time synchronisation was to be achieved using a separate IRIG-B time synchronisation network. Other options are available that achieve this using the Ethernet network.

8. The SCADA RTU

The existing eThekweni Electricity SCADA Master Station uses the DNP3.0 protocol for communication with substation SCADA RTU's. The SCADA Gateway was therefore required to provide a DNP3.0 database that could be polled by the Master Station. In previous specifications the SCADA Gateway communicated with protection relays on a substation DNP3.0 network.

This network was over an RS485 physical layer for Pilot Project 1 and over Ethernet for Pilot Project 2.

With the introduction of IEC61850, several manufacturers produced devices capable of populating a DNP3.0 database by communicating with protection relays using the IEC61850 protocol. This functionality was specified for the SCADA Gateway.

9. The Human Machine Interface (HMI)

The HMI was required to provide a graphical user interface to allow an operator to view status and carry out control of the primary plant. The HMI was also required to maintain an event record database which could be viewed using the graphical user interface. Operator interaction was required to be via a touch screen. A locked keyboard was to be provided for maintenance of the HMI by select personnel only.

The HMI was required to have a default screen showing an overall substation mimic depicting the status of all primary plant, selected measured values and indication of the presence of alarm conditions and their location(s). The default screen was also required to display an overall event record window showing all substation events and their time stamps in chronological order.

From the overall screen, it was to be possible to “drill-down” into any bay to show the detailed mimic for the bay with measured values and status of alarms. Operation of primary plant was to be carried out from this bay-level screen. The bay-level screen was also required to display a bay-specific event record window showing all events related to the particular bay and their time stamps in chronological order.

Pilot project 2 provided valuable experience regarding the reliability of hardware, operating system and software for the HMI. During the preparation of the latest specification, static electronic HMI products having no moving parts such as fans and hard drives became available. These HMI’s make use of more robust embedded operating systems scaled down to the minimum overhead for the application and are designed specifically for substations in that they make use of the IEC61850 protocol, are designed for DC supplies and conform to the same IEC specifications as normal protection relays. An HMI with the above characteristics was requested as an option in the tender and was offered and accepted. In future specifications static electronic systems will be specified.

Suppliers have often marketed the many additional features that HMI systems can provide such as data-logging and trending, condition monitoring, interlocking and operation sequencing. eThekwini Electricity’s philosophy is that the primary function of the HMI is to provide a point of control and monitoring of the substation plant and that the HMI system should not be burdened with secondary “nice-to-have” functionality that could result in reduced reliability of the primary function. “Mission critical” functionality such as tripping should not be routed via the HMI and important functionality such as interlocking and operation sequencing can be carried out at relay level which is deemed to be more secure.

Many HMI systems offer complex options for operators. eThekwini Electricity’s philosophy is that operators are not required to have a high level of computer literacy and should thus be able to interact with the HMI via a touch screen using simple buttons to navigate and operate the system. The logging in of users was even excluded to improve ease of use. This “shallow learning curve” approach is believed to more likely to gain the acceptance and “buy-in” of operators.

Some HMI systems are able to provide both HMI and SCADA RTU functionality in one device. eThekwini Electricity’s philosophy is that both points of remote control (HMI and SCADA) for the entire substation should not be disabled for a single device failure. Separate devices were thus specified for the HMI and SCADA Gateway. The same device was offered for both applications, the only difference being the provision of a touch screen and keyboard with the HMI device. The benefit arising from this is that the HMI and SCADA Gateway have a common configuration, have common spares and can perform each other’s functions allowing both functions to be available after a single device failure.

It is envisioned that vastly improved reliability will be achieved with the HMI offered over that supplied for Pilot Project 2.

10. The IEC61850 Substation Configuration Language (SCL)

IEC61850-6 defines a substation configuration language allowing all IEC61850 communication within a substation to be configured with a substation configuration tool.

The substation configuration tool, which could be provided by any party, comprises software that imports the capability data of protection relays in a standard format, carries out substation communication configuration and produces configuration files that are sent to the relays or other devices to fully configure them for the required communications arrangement.

This substation configuration tool effectively configures all relays to serve the appropriate information from their available logical nodes to the HMI and SCADA Gateway clients. It configures the HMI and SCADA Gateway to subscribe to this information and it configures all relays for the required peer-to-peer (GOOSE or GSSE) requirements.

It needs to be stressed that the substation configuration tool is only required to configure the communications arrangement and in no way affects logic configuration or settings within a device. Configuration and settings are performed by the device manufacturer’s configuration software using proprietary methods.

For most IEC61850 compliant HMI and SCADA Gateway systems available, the substation configuration tool forms part of the HMI or Gateway configuration software. All relays that are IEC61850 compliant are supplied with an IED Capability Description (ICD) file. All the ICD files for the relays in the substation can be imported into the substation configuration tool. When the substation configuration is complete a Substation Configuration Description (SCD) file is produced by the substation configuration tool. For most relay manufacturers, this file is then imported by the relay configuration software, which applies the necessary configuration to the relays. This file is also used within HMI or SCADA Gateway configuration software to configure these devices.

Configuration using an IEC61850-6 compliant substation configuration tool was specified, offered and accepted.

11. Peer-To-Peer Messaging Using IEC61850 GOOSE And GSSE

The specification required peer-to-peer GOOSE or GSSE messaging to be used where information is required to be transmitted from one relay to another. Examples of applications of peer-to-peer messaging are interlocking schemes, automatic switching sequence schemes and indication.

The speed and reliability of GOOSE messaging was proven in Pilot Projects 1 and 2. A frequently overlooked feature of GOOSE is the fact that it is continuously supervised. In between changes of state initiating the sending of a message, the message is continuously sent at configurable intervals indicating no change of state. A subscribing relay that does not receive the message within the configurable interval can assume a loss of communication and initiate an appropriate alarm. The subscriber can also be configured to assume a default state if the message is not received.

GOOSE messages were not to be used for any tripping signals. In feeder and transformer protection schemes GOOSE messaging is of little use for tripping purposes as each protection relay issues a hard-wired trip to the associated circuit breaker/s. For bus bar protection and breaker fail protection schemes there was scope for using GOOSE messaging. eThekwini Electricity has adopted a philosophy not to use this option due to the inability to easily isolate tripping for testing purposes as learnt in Pilot Project 1. A bus-zone and breaker-fail scheme using hard-wired bus wires for tripping signals was specified.

12. Integration Of Non- IEC61850 Compliant Devices

There are many instances where relays that are not IEC61850 compliant are required to be integrated into substation automation systems. The most common instance is the inclusion of a feeder differential protection relay that is required to match with an existing remote end.

One option of including such devices into a substation automation scheme is by means of a proxy server comprising an IEC61850 compliant device that communicates with the non-compliant devices by means of another (typically master/slave) protocol. This would add another, normally non-standard, communications network with its associated hardware into the substation. The proxy server does not fall into the category of a protection relay, a point of control or a standard communications device, which are the categories of devices that have been allocated to divisions in eThekwini Electricity's organizational structure in terms of maintenance responsibility. eThekwini Electricity thus does not have a division who could logically be assigned to maintain such a system. This option is not accepted by eThekwini Electricity.

In all cases where non-compliant devices have been required there is an associated relay in the protection scheme that is required to be IEC61850 compliant. eThekwini Electricity's preferred

integration method is thus for the relevant contact outputs from the non-compliant relay to be hardwired to digital inputs of the compliant relay. These inputs are assigned to logical nodes within the compliant relay that are then available for inclusion in the substation automation system. This method was specified, offered and accepted.

13. Implementation Conformance Statements

IEC61850 specifies a standard format for device conformance statements.

Protocol Implementation Conformance Statements (PICS) provide information regarding the features of the IEC61850 standard included in the device. Model Implementation Conformance Statements (MICS) provide details on the device's available logical nodes and how they are implemented. This information allows the client to raise questions on how the specified arrangement will be implemented with the available features.

The specification required conformance statements to be included with tenders for all IEC61850 compliant devices and assisted immensely during adjudication.

14. Relay Mimics, Controls and LED's

All modern protection relays are provided with LCD screens. It has been found that, for a marginal price increase, many models can be ordered with screens large enough to display bay mimics. This feature provides a backup mimic in the event of the failure of the HMI. This functionality was specified, offered and accepted.

Many relays are now provided with front-face push-buttons for circuit breaker control. eThekwini Electricity's philosophy is that operators do not interact with relays in any way except to observe information displayed on LED's and LCD's and to reset the relay when required after a protection trip. This results from the vast number of different relay models in use and the inability to train operators on the functionality of each and every relay model. The use of relay push buttons for local control of indoor switchgear would result in the loss of local control in the event of a relay failure. Hard-wired panel mounted local control switches are thus specified for local control and all remote control is via either the HMI or SCADA.

The specification required all alarm states within a relay, whether from internal or external sources, to be displayed by means of LED's. This provides backup indication in the event of the failure of the HMI and has previously proven invaluable during testing. Although relays that have insufficient LED's can often display this information by scrolling through relay menus this solution is not accepted due to the philosophy that operators do not interact with relays. To date the solutions accepted have always had sufficient LED's.

15. Integration Of Substation Automation Into The Utility Organizational Structure

With the introduction of the new technologies and methodologies associated with Substation Automation an exercise needed to be performed to determine how these systems would be implemented and then maintained by the resources available in the organizational structure.

The resources used for project implementation remained the same as for previous schemes. The HV Projects division remained responsible for the specification, bid adjudication and project management. The Protection & Test division will continue to provide assistance with testing and protection settings while the HV Operations division will assist with testing the SCADA system.

The protection systems will continue to be maintained by the Protection & Test division which is the only division authorised to re-configure relays. The communication network, including all Ethernet switches and communications links whether galvanic or optic fibre, is to be maintained by the Communications division. This division requires no knowledge of protection or control systems and is required to maintain standard non-configurable components only.

The SCADA Gateway remains the responsibility of the HV Operations division. The new component in substation automation systems, the HMI, is to be maintained by the HV Operations division. In the latest contract the SCADA Gateway and the HMI consist of the same hardware and software platform, justifying this arrangement. Where applicable, specific training has been organized with solution providers for the various components of the substation automation systems.

16. IEC61850 Based Protection and Control Projects

During the second half of 2005 the new specification was used in a tender for protection and control equipment for eight new substations. By the end of 2005 tenders had been adjudicated and a contract awarded.

Only one tender offered products that could implement the substation automation systems as specified. The tender was also the cheapest and was recommended and accepted. Several products offered by other manufacturers were either not compliant or not fully compliant with IEC61850. These solutions required additional hardware such as proxy servers for their implementation, which increased the complexity and probably the price of the solutions.

Most of these non-compliant manufacturers indicated a proposed "road map" to full compliance with IEC61850 for their products. It is anticipated that fully compliant tenders will be received in future which will result in a more competitive environment for suppliers and hopefully savings for utilities. Most of the systems to be supplied have passed the approval phase and are in the factory testing phase. To date it appears that the philosophies and methodologies required by the specification have been followed.

17. Financial Implications

An exercise has been carried out to determine the financial impact of the new philosophy. This exercise has produced some better than expected results.

One of the 132/11 kV substations included in the latest protection and control tender having four transformers and twenty 11 kV feeders was used as an example. The tendered prices for the new philosophy protection and control equipment and contracts currently in place for legacy protection and control equipment were used to determine the value of "take-out" and "add-in" items as follows:

An exercise for a 132 kV Switchyard having nine feeders and a bus-section indicated little difference in price between the legacy and new philosophy protection and control equipment. The reduction in costs of the secondary cabling and the omission of the legacy supervisory equipment is cancelled by the additional costs of the communications network and HMI. The improved functionality achieved through substation automation is therefore achieved for no extra cost in these cases.

It was noted that the addition of IEC61850 functionality has not increased the prices of protection relays.

Take-Out Items	
Secondary Cabling	R 200 000
Remote Control Panels	R 160 000
Tap Change Control Panels	R 500 000
11 kV Bus-Zone Scheme	R 20 000
Supervisory Junction Board	R 15 000
Supervisory Outstation	R 115 000
Reduction in Control Room size	R 220 000
TOTAL	R 1 230 000

Add-In Items	
11 kV Bus-Zone Scheme with bay processing for bus-sections and coupler	R 55 000
SCADA Gateway	R 80 000
HMI	R 130 000
Communications Network	R 165 000
TOTAL	R 430 000

The savings are thus	
Take-Out Items	R (1 230 000)
Add-In Items	R 430 000
SAVING	R 800 000

18. Envisaged Adoption of the Full IEC61850 Model for Substation Automation

It is envisaged that the development of the IEC61850 process bus will revolutionise substation communication with links between primary plant such as outdoor circuit breakers and instrument transformers and IED's being provided by communication networks with traditional secondary cabling being eliminated completely.

It is hoped that in the near future our specification will be developed further to incorporate a process bus. The envisaged substation arrangement is shown in Figure 3.

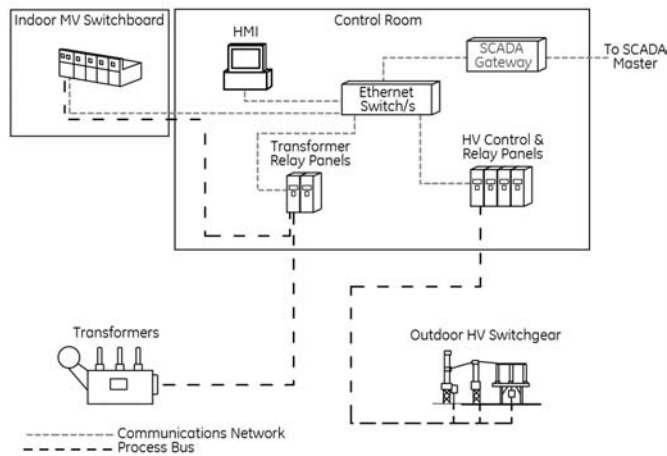


Figure 3.
Envisaged process bus protection and control arrangement.

19. Conclusion

The substation automation pilot projects and the subsequent contract for eight substations currently underway have allowed eThekweni Electricity's philosophies and specifications to evolve from systems that used relatively low technology solutions to ones using the latest communication technologies.

The "legacy" systems were heavily dependant on on-site hard-wired secondary cabling with associated disadvantages. The new systems allow for factory tested components to be delivered and connected together via communication networks with only a minimum of on-site secondary cabling.

The reduction in secondary cabling and the rationalization of functionality in relays made possible by substation automation has enabled significant cost savings to be achieved.

The adoption of the IEC61850 standard has allowed utilities to avoid being locked into proprietary communications standards by allowing the interoperability of devices from different manufacturers. This has contributed to a more competitive environment for suppliers resulting in savings to utilities.

It is envisaged that future protection and control relays and products will be provided with IEC61850 compliance as standard with no price premium for this functionality.

The IEC61850 standard which has predominantly been driven by suppliers will be increasingly influenced by feedback from utilities and system integrators as more projects are implemented.

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Wireless Radio Application Guide

Steel McCreery
GE Multilin

1. Introduction

The age of modern industrial radio data communications was ushered in when it was proven that digital data could be economically and reliably transmitted from one device to another using a voice radio set known as narrow band radio fitted with a modem. Packet radio is a term coined by amateur radio enthusiasts that refers to this type of digital radio communications equipment. The modern MDS 9700 and 9710 radios that are applied to similar applications can trace their design heritage back to the days of the first packet radios. Over the years technological advancements in the area of digital radio communications have allowed companies such as MDS to develop a wide range of radio equipment for applications ranging from simple voice communications to the simultaneous transmission of multiple high-speed data channels over a wide band radio link. The intent of this application note is to serve as a guide for the correct selection and configuration of MDS radios for common industrial and utility protective relaying applications using GE Multilin relays.

Currently at the physical layer GE Multilin relays and MDS radios share two interface standards: RS485 and 10BaseT Ethernet. The MDS TransNet radios support RS232 and RS485 making them an excellent choice for SCADA applications involving relays that have only a RS485 networking port. The iNET 900s and iNET-II 900's support RS232 and Ethernet making them an excellent choice for Ethernet enabled SR and Universal Relays. Table 1 is a summary of MDS radios, interfaces, on air speeds, supported protocols and typical distances.

1.1 Typical Protective Relaying Applications Suitable for MDS Radio links

Within the scope of protective relaying LAN architectures there are three areas of application that are appropriate for the use of radio links: SCADA, LAN extension and digital I/O status information exchange. The DNP3 protocol is very popular in wide area SCADA applications. The DNP3 unsolicited response mode of operation allows for the optimization of the communications link while at the same time provides very fast updates of status changes. For this reason, it is a very desirable mode of operation for DNP3 slave devices. It should be noted that the system architect must ensure that there is a mechanism in place to resolve the issue of media contention. When using a Ethernet LAN media, DNP3 unsolicited messaging via TCP/IP resolving the contention issue and provides confirmable messaging.

1.2 Terminology

Here are the definitions of some common terms that will be used through the rest of this application note.

Spread Spectrum Radios: Radio transmission using the spread spectrum technique was originally developed to provide jam-resistant military communications. Spread spectrum uses a modulation technique that distributes a transmitter's signal over a very wide bandwidth, making it virtually undetectable to a conventional radio receiver. Today the two primarily methods that are used by spread spectrum technology to transmit messages

Radio	Interface	Supported Protocols	On-air-Speed	Type of Radio	Typical Maximum Distances
MDS TransNET	RS485, RS232	DNP3, Modbus	160 kbps	Spread spectrum: No license required	30 miles (terrain permitting)
MDS iNET 900	10BaseT	DNP3 via TCP/IP, Modbus via TCP/IP, IEC61850	0.5Mbps	Spread spectrum: No license required	30 miles (terrain permitting)
MDS iNET-II 900	10BaseT	DNP3 via TCP/IP, Modbus via TCP/IP, IEC61850	1.0 Mbps	Spread spectrum: No license required	15-20 miles (terrain permitting)

Table 1.

are “Frequency Hopping Spread Spectrum” and “Direct Sequence Spread Spectrum.”

Narrowband Radios: In communications, narrowband is a relative term. For these applications, this term refers to voice channel radios or the modern equivalent of the old packet radios. With baud rates of up to 9.6k they are typically used in SCADA applications supporting a single protocol such as DNP or ModBus. The 9790 and 9710 are licensed MDS narrow band radios that can be used in applications involving distances of up to 50 miles while the TransNET radios are unlicensed spread spectrum radios used in applications where the distance can be up to 30 miles at serial baud rates up to 115.2 kbps.

Wideband Radios: In communications, wideband is also a relative term. Within MDS this term applies to radios such as the LEDR 900 which have a bandwidth of 200 KHz allowing multiple channels of data to be transmitted at the same time.

Access Point Radio: The radio that connects the remote radios together to form the wireless network. The access point radio usually connects to a wired network, and can relay data between the remote radios and devices on the wired network. Sometimes it is referred to as the Wireless Access Point (or WAP).

DB (Decibel): A measure of the ratio between two signal levels. Frequently used to express the gain (or loss) of a system.

DBi: Decibels referenced to an “ideal” isotropic radiator in free space. Frequently used to express antenna gain.

DBm: Decibels referenced to one milliwatt. An absolute unit used to measure signal power such as a transmitters output power.

Equivalent Isotropically Radiated Power (EIRP): the amount of power that would have to be emitted by an isotropic antenna to produce the peak power density observed in the direction of maximum antenna gain. EIRP can take into account the losses in the transmission line and connectors and includes the gain of the antenna. The EIRP is often stated in terms of decibels over a reference power level, that would be the power emitted by an isotropic radiator with an equivalent signal strength.

FCC: Federal Communications Commission

Standing-Wave Ratio (SWR): A parameter related to the ratio between the forward transmitter power and the reflected power from the antenna system. As a general guideline, reflected power should not exceed 10% of the forward power.

2. iNET-II 900 Radio Applications

This section documents the hardware and software configure procedures that are required to apply the iNET-II radios to the applications identified earlier.

2.1 Application: Point to Point or Point to Multi-Point SCADA

In this first example we will look at the configuration procedure and performance of the radio link in a SCADA application. The application layer protocols that are supported include ModBus via TCP/IP and DNP3 via TCP/IP.

Notes:

1. All tests were conducted with iNET-II 900 radios.
2. For correct operation a switch was required between the iNET 900 radio and the relay.

2.1.1 Hardware Configuration:

Figure 1 shows the typical equipment that would be deployed at each site. It consists of a relay, radio and an antenna. At least one of the radios must be capable of operating as the access point radio.

Note: For the lab tests the radios were equipped with whip antennas and 50 ohm loads.



Figure 1.

The pin out for the cross over cable (sometimes referred to as a patch cable) used to connect the iNET-II radio to the Universal Relay’s 10BaseT Ethernet port is shown in Figure 2 while Figure 3 shows the cable pin out for the transceiver configuration cable.

RJ45 Pin # (END 1)	Wire Color	Diagram End #1	RJ45 Pin # (END 2)	Wire Color	Diagram End #2
1	White/Orange	1	1	White/Green	1
2	Orange	2	2	Green	2
3	White/Green	3	3	White/Yellow	3
4	Blue	4	4	Blue	4
5	White/Blue	5	5	White/Blue	5
6	Green	6	6	Yellow	6
7	White/Brown	7	7	White/Brown	7
8	Brown	8	8	Brown	8

Figure 2.

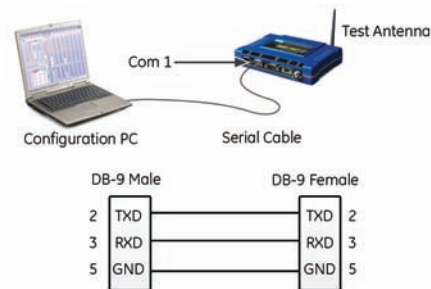


Figure 3.

2.1.2 Configuration

The following is the minimum steps required to configure the radios for the application. It is recommended that the engineer read the entire instruction manual to become familiar with all of the options that are available

1. Connect the computer to the access point radio via the serial transceiver configuration cable and then launch a terminal emulation program such as HyperTerminal with the following communication port settings:
 - 19,200 bps data rate
 - 8 data bits, no parity
 - One stop bit, and no flow-control
2. Press the enter key to receive the login: prompt

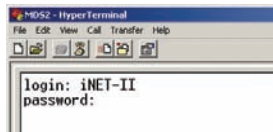


Figure 4.

3. Enter the default password "admin" in lower case and then press the enter key.
4. You will be presented with the main menu shown in Figure 5. Type the letter G on the keyboard to access the main menu.
5. Note that the default "Device Node " is set to "Access Point".

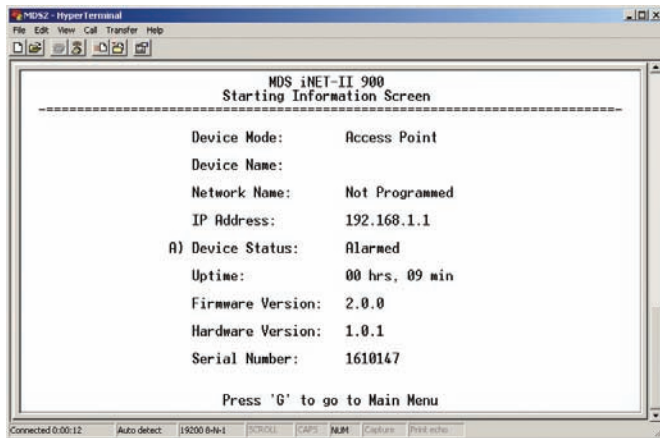


Figure 5.

There should be only one access point per network and so we will set this as the access point. The access point radio, is the radio that controls the information exchange between all radios on the network. The operating mode of all other radios within the network must be set to remote. Enter B to configure the unique network name. In this example we will use "steel". The same network name must be programmed into all radios within the network. To support remote management of the radio, a unique IP address and subnet mask must also be assigned to each radio. You should contact your IT department for a valid range of IP addresses and a subnet mask. For our test network we will use the IP address range 3.94.247.1 to 3.94.247.254 and a subnet most of 255.255.255.0.

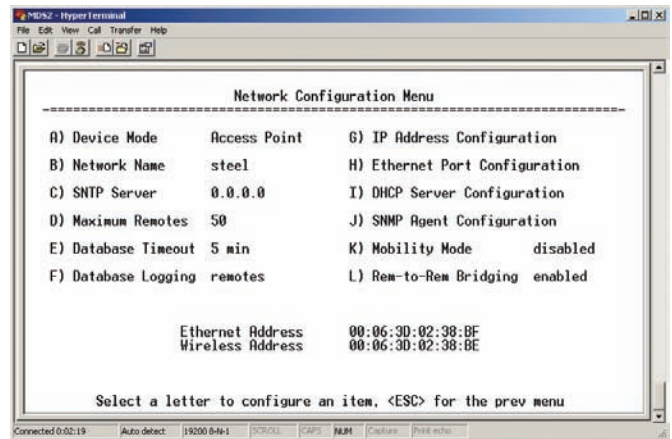


Figure 6.

6. Once a unique IP address and the subnet mask have been entered select E to store these settings and then select the escape key to go to the previous menu. The access point has been configured. Note all radios within the network will have the same subnet mask.

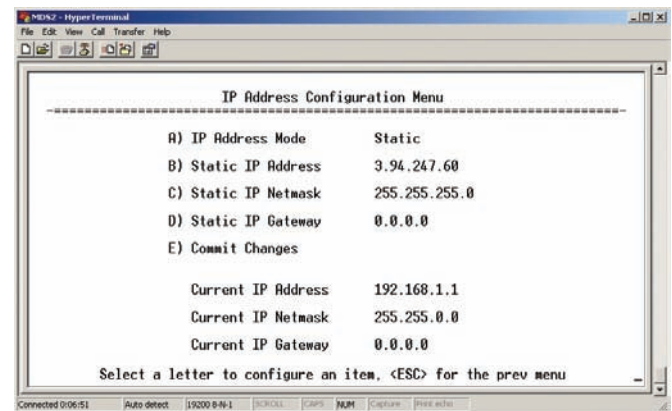


Figure 7.

7. The above procedure is repeated for each additional radio in the network. Each of these radios must be set for the Device Mode "Remote".

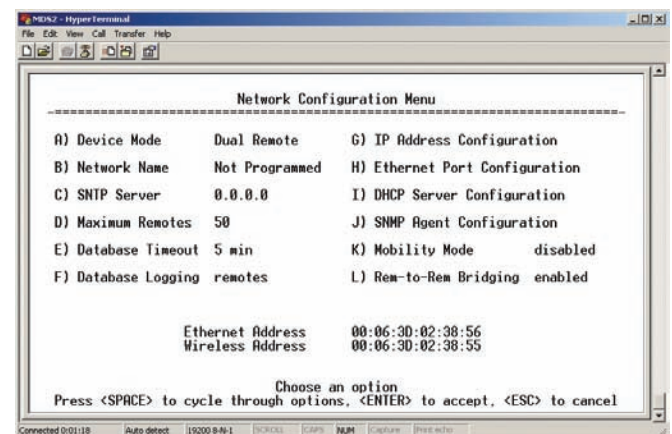


Figure 8.

8. Configure each of the Universal Relay's Ethernet ports. Using the specified cable, connect the Universal Relays to the radios.

- The ping instruction should be used to test connectivity to both the radios and the Universal relays.

2.1.3 Performance Tests:

Once the network of three UR's and INET-II radios were configured the performance of the network was tested using EnerVista UR setup software. With an effective "on air" bit rate of approximately 1Mbps the performance of the INET II radio link from a users perspective seemed to be comparable to the performance of a hardwired Ethernet network utilizing 10 Mbps Ethernet switches.

- Once operation is verified, refer to the site installation and commissioning section of this document for addition information and guidelines.

2.2 Application: Automation I/O via IEC61850 GSSE and MDS iNET-II radios

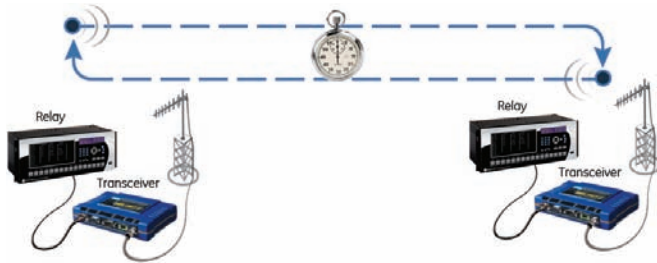


Figure 9.

The reliability and latency of the radio link are the two performance characteristics we will examine in the investigation of the suitability of the MDS radio link to transport IEC61850 GSSE messages between two universal relays

Topology: Point-to-Point

Protocol: IEC61850 GSSE

2.2.1 Configuration:

- To improve performance, modifications to the default radio configuration settings are required. From the main configuration screen type C to select the Radio Configuration Menu shown in Figure 10. Set the Beacon Period to Slow and the Dwell Time to 32.8 milliseconds as shown.

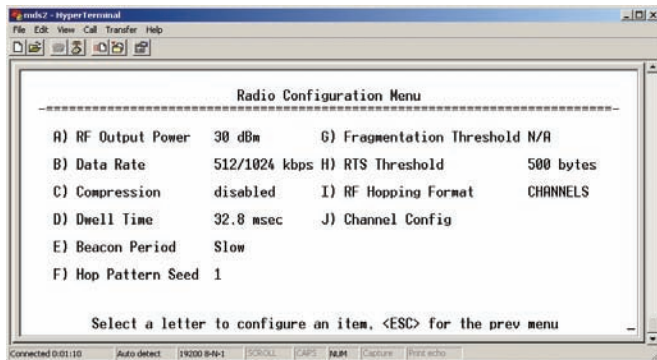


Figure 10.

- The two Universal Relays are configured such that a GSSE message would be transmitted from the first relay to the second relay which would cause the second relay to immediately send a GSSE message back to the first relay. The first relay's FlexLogic would measure the total time for the sequence of these two messages and then increment one of four counters based on the round trip time. The counters represent the following round trip times:

- less then or equal to 20 milliseconds
- greater then 20 and less then or equal to 30 milliseconds
- greater then 30 and less then or equal to 40 milliseconds
- greater then 40 and less then or equal to 80 milliseconds

If we assume that the time to travel from one relay to the other is approximately half the round trip time we have an indication of the latency of the communication link between the two relays. A fifth counter was used to count the total number of message sequences generated. This number was checked to ensure it was equal to the sum of the other four counters to ensure all message sequences generated were measured. The FlexLogic used in this evaluation is as shown in section 6.0.

2.2.2 Test Results:

The following are the test results based on the point-to-point topology and the measurement of 29672 consecutive message sequences.

Round trip times:

- Percentage of messages with a round trip time less than 20 milliseconds: 0.78% (232)
- Percentage of messages with a round trip time between 20 to 30 milliseconds: 98.79% (29303)
- Percentage of messages with a round trip time between 30 to 40 milliseconds: 0.43% (127 messages)
- Percentage of messages with a round trip time between 40 and 80 milliseconds: 0.03% (10).
- Percentage of messages with a round trip time greater then 80 milliseconds 0% (0).

The transmission latency for point-to-point I/O exchange is such that this configuration is suitable for many distribution and automation applications. We should note that when topologies are expanded beyond a point-to-point topology the number of variables that impact latency become too numerous to be able to accurately predict latency without testing.

3. Site Installation and Commissioning Procedures

The following is a brief description of recommended commissioning procedures and measurements that should be taken during the commissioning process.

3.1 Site Selection-Basic Requirements

For optimum radio performance, the installation sites for the access point and remote stations must be carefully considered. Suitable sites should provide:

- Protection of the radio equipment from direct weather exposure
- A source of adequate and stable power supply
- Suitable entrance for antenna cable
- Interface or other required cabling
- Antenna location that provides an unobstructed transmission path in the direction of the associated station(s) often referred to as “a line of sight path” were the access points antenna has a clear path to the remote location(s). The next section expands further on this point.

3.2 Evaluating Path Quality

A line-of-sight path is ideal and provides the most reliable transmission in all cases. However, minor obstructions in the signal path will not necessarily block communication. In general, the need for a clear path becomes greater as operating frequency and transmission distance increases. With the exception of short-range paths that can be visually evaluated, a path study is generally recommended for new installations. A path study predicts the signal strength, reliability and fade margin of a proposed radio link. While terrain, elevation and distance are the major factors in this process, a path study must also consider antenna gain, feedline loss, transmitter power, and receiver sensitivity. MDS provides this service and it is recommended in all applications.

3.3 Antenna Selection and Orientation

The most important item affecting radio performance is the antenna system. Careful attention must be given to this part of an installation, or the performance of the entire system will be compromised. High quality, gain antennas should be used at all access point radios and remote radios. The antennas should be specifically designed for use at the intended frequency of operation.

Communication antennas are made by a number of manufacturers and fall into two general categories, omni-directional, and directional. An omni-directional antenna (Figure 11) provides equal radiation and response in all directions and is therefore appropriate for use at the access point radio, which must communicate with an array of remote radios scattered in various directions. At remote radios, a directional antenna such as a Yagi (Figure 12) is typically used. Directional antennas allow greater communication range, and reduce the chance of interference to and from other radio networks. It is necessary to aim the remote radio antennas in the desired direction of communication. The

end of the antenna (furthest from the support mast) should face the access point radio. Final alignment of the antenna heading can be accomplished by orienting it for maximum received signal strength. Most radio equipment includes provisions for measuring the receive signal strength.

3.4 Antenna Mounting Considerations

The antenna manufacturer’s installation instructions must be strictly followed for proper operation of a directional or omni-directional antenna. Using the proper mounting hardware and bracket ensures a secure mounting arrangement with no pattern distortion or de-tuning of the antenna. The following recommendations apply to all antenna installations:

- Mount the antenna in the clear, as far away as possible from obstructions such as buildings, metal objects, dense foliage, etc. Choose a location that provides a clear path in the direction of the associated station.
- Polarization of the antenna is important. Most systems use a vertically polarized omni-directional antenna at the master station. Therefore, the remote antennas must also be vertically polarized (elements perpendicular to the horizon). Cross-polarization between stations can cause a signal loss of 20 decibels (dB) or more.

Omnidirectional Antennas

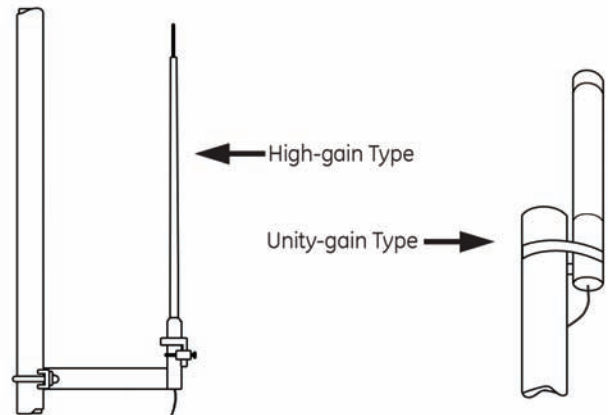


Figure 11.

The above omnidirectional antenna is a typical antenna that would be use by the access point radio.

Yagi Antenna

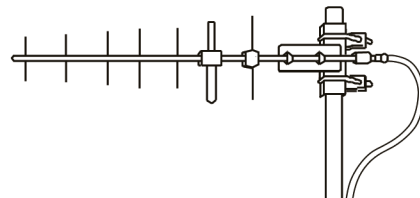


Figure 12.

The Yagi antenna is a typical antenna that would be used at the remote radio. Note: The polarization of the Yagi antenna in Figure 12 is correct if used with either of the above omni-directional antennas of Figure 11.

3.5 Feedlines

The choice of feedline used with the antenna should be carefully considered. Poor-quality coaxial cables should be avoided, as they will degrade system performance for both transmission and reception. The cable should be kept as short as possible to minimize signal loss. For cable runs of less than 20 feet (6 meters), or for short-range transmission, an inexpensive feedline such as Type RG-8A/U are acceptable. Otherwise, we recommend using a low-loss cable type suited for 900 MHz, such as Heliax®

Length vs. Loss in Coaxial Cable at 900 MHz				
Cable Type	10 Feet (3.05 m)	50 Feet (15.24 m)	100 Feet (30.48 m)	500 Feet (152.4 M)
RG214	.76 dB	3.8 dB	7.6 dB	Unacceptable Loss
LMR-400	.39 dB	1.95 dB	3.90 dB	Unacceptable Loss
1/2" HELIAX	.23 dB	1.15 dB	2.29 dB	11.45 dB
7/3" HELIAX	.13 dB	.64 dB	1.28 dB	6.40 dB
1-1/4" HELIAX	.10 dB	.48 dB	.95 dB	4.75 dB
1-5/8" HELIAX	.08 dB	.40 dB	.80 dB	4.00 dB

Table 2.

3.6 Setting the Output Power

The transceiver is normally supplied from the factory set for a nominal +30 dBm (+29 dBm for iNET-II) RF power output. This is the maximum transmitter output power allowed under FCC rules. The power must be decreased from this level if the antenna system gain exceeds 6 dBi. The allowable level is calculated and is based on the antenna gain, feedline loss, and the transmitter output power setting.

Note: In some countries, the maximum allowable RF output may be limited to less than the Figures referenced here. Be sure to check for and comply with the requirements for your area.

Example:

To determine the maximum allowable power setting of the radio, perform the following steps:

1. Determine the antenna system gain by subtracting the feedline loss (in dB) from the antenna gain (in dBi). For example, if the antenna gain is 9.5 dBi, and the feedline loss is 1.5 dB, the antenna system gain would be 8 dB. (If the antenna system gain is 6 dB or less, no power adjustment is required.)
2. Subtract the antenna system gain from 36 dBm (the maximum allowable equivalent isotropically radiated power or (EIRP). The result indicates the maximum transmitter power (in dBm) allowed under the rules. In the example above, this would be 28 dBm.
3. If the maximum transmitter power allowed is less than 30 dBm, set the power to the desired level (Main Menu>>Radio Configuration>>RF Output Power Setpoint). For convenience, Table 3 lists several antenna system gains and shows the maximum allowable power setting of the radio. Note that a gain of 6 dB or less entitles you to operate the radio at full power output: 30 dBm for iNET and 28.7 dBm for iNET-II's.

Antenna System Gain vs Power Output Settings			
Antenna System Gain (Antenna Gain in dBi ² minus Feedline Loss in dBt)	Maximum Power Setting (PWR Command) iNET Radio	Maximum Power Setting (PWR Command) iNET-II Radio	EIRP (In dBm)
Omni 6 (or less)	30	28	36
Omni 9	27	26	36
Yagi 12	24	23	36
Yagi 14	22	Not allowable	36
Yagi 16	20	Not allowable	36

Table 3.

3.7 SWR of the Antenna System

A proper impedance match between the transceiver and the antenna system is very important. It ensures the maximum signal transfer between the radio and antenna. By measuring the SWR (standing-wave ratio) of the antenna system the impedance match can be checked. The reflected power should be less than 10% of the forward power (≈2:1 SWR). Higher readings usually indicate problems with the antenna, feedline or coaxial connectors. If the results are normal, record them for comparison for use during future routine preventative maintenance. Abnormal readings indicate possible trouble with the antenna or the transmission line that will need to be corrected.

4. TransNET Radios Applications

As stated earlier, the TransNet radios support both RS232 and RS485 physical interface standard. Both the ModBus and DNP3 protocols can be used over the TransNet radio link. Most GE Multilin relays have at least one RS485 networking port making the MDS TransNet radios an ideal choice for applications involving relays supporting either protocol and having an RS485 networking port.

4.1 Application: Point to Point or Point to Multi-Point SCADA Hardware Configuration:

The following diagram depicts the typical equipment that would be deployed at each site. It consists of a relay, a radio, and an antenna. Note that one of the radios must be capable of acting as the access point radio.

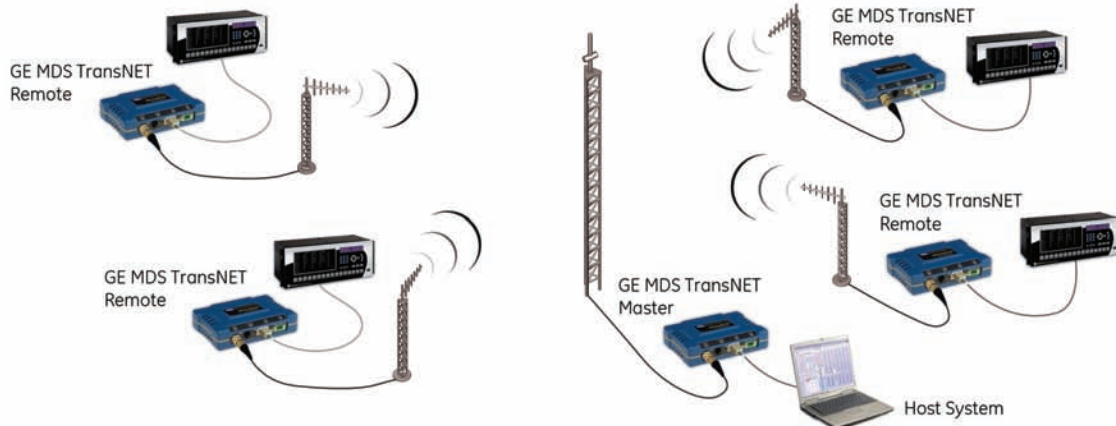


Figure 13.

Note: For the lab tests, the radios were equipped with whip antennas and 50 ohm loads.

4.2 Configuration:

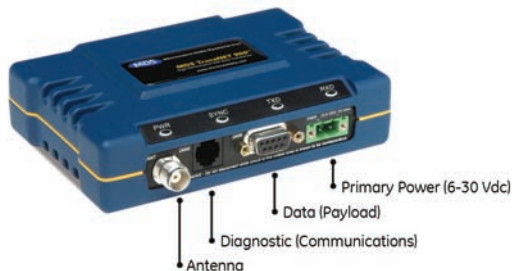


Figure 14.

1. The easiest way to configure the radio is with the TransNET configuration software while connected to the diagnostic port with a serial cable consisting of an RJ11 to DB9 female adapter part number 73-2434A02 and a cable 03-3246A01.
2. With the antennas connected to the radios, power the radios and connect to the access point radio and launch the software.

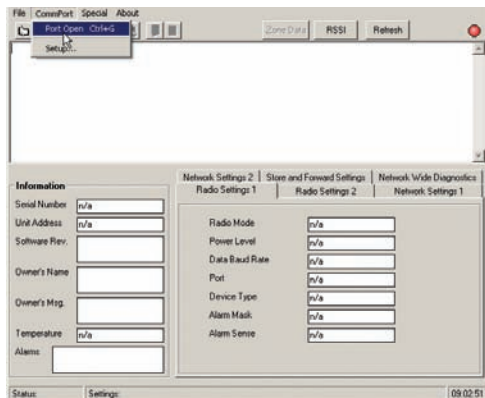


Figure 15.

3. Select Commport and then Port open
4. Connect to the radio by clicking on the connect icon. (see Figure 16). Select the Radio Settings tab1 and ensure that the Radio Mode is set to M for master (this radio will be the access point radio). If the Radio Mode is not set to M double click and

enter MODE M to set the radio to master. This radio's port will be connected to the computer with the SCADA software and so the radio port should be set to RS232. We will be using the Universal Relays configuration software to talk to a Universal Relay which has one of its RS485 ports set to 9600 baud, 8, no parity and one stop bit. Therefore this radio's port baud rate, data bits, parity and stop bits must be set to 9600, 8, no parity and one stop bit respectively. Figure 16 shows these settings.

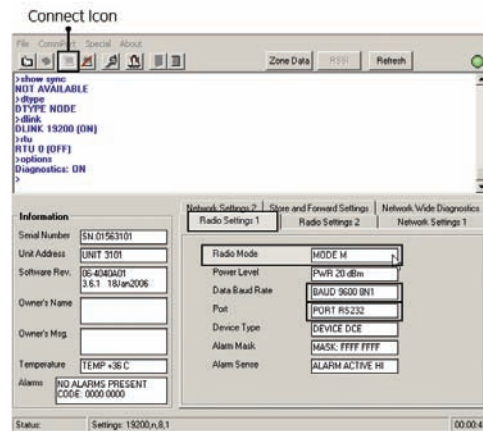


Figure 16.

5. Select the Network Settings tab 1. Set the Network Address to a unique number. This same number must now be set in all radios that are to be used in this network.

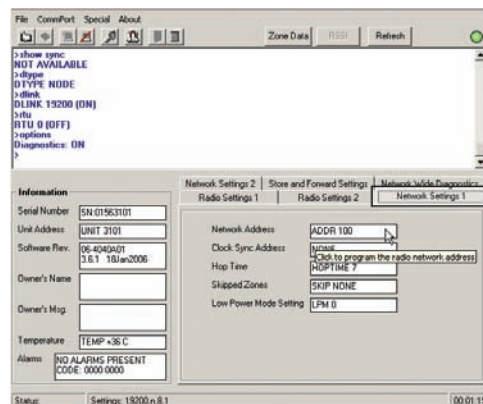


Figure 17.

- The EnerVista UR Setup software uses the ModBus RTU protocol to communicate to the Universal Relay. ModBus RTU has strict rules with respect to the time between characters in a valid command. To ensure this timing is maintained the "Data Buffering" option within the radio must be enabled. To do this, select the Network Settings 2 tab and enable data buffering by setting the Data Buffering to Buff ON. To stop the communication to this radio, select the Com Port menu at the top of the screen and then select Close or left click on the close icon (see Figure 18)

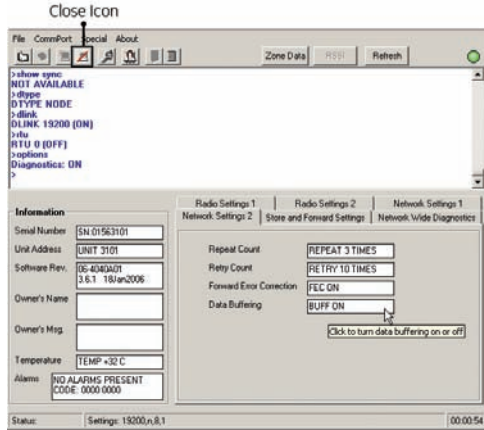


Figure 18.

- Connect to the first remote radio and open communications. Select the Radio Setting tab 1 and set the radio mode to remote with the command MODE R. If the serial port of this remote is to be connected to a relay's RS485 port, set the port mode to RS485 by typing the setting "PORT RS485" in the window labeled Port. Set the baud rate, bits per character, parity, and stop bits as described earlier.

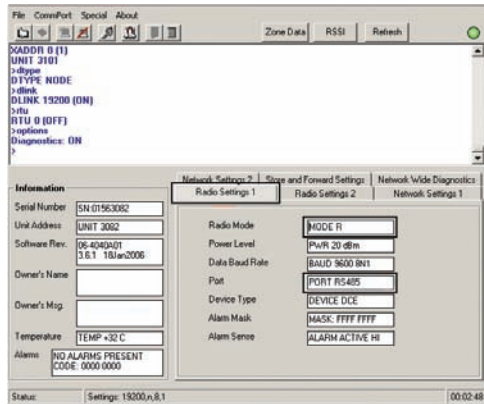


Figure 19.

- Select the Network Settings tab 1 and set the network address to the same value as the access point radio. Repeat this procedure for each slave.

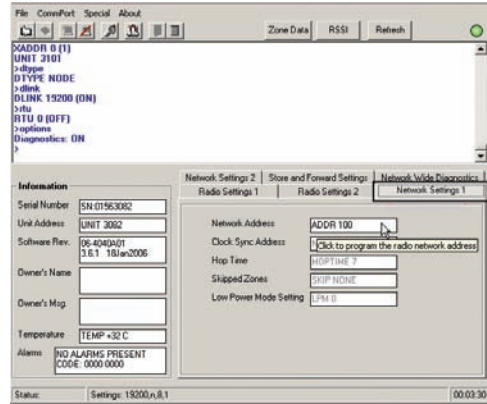


Figure 20.

- Once all radios have been configured, connect the computer running the EverVista UR Setup Software to the access point radio's RS232 port and then connect the remote radio's port configured for RS485 to the Universal Relay's port using a cable with a pin configuration corresponding to that of Figure 21. The ability to configure and monitor the Universal Relay via the computer and radio network verifies the correct operation of the radio network.

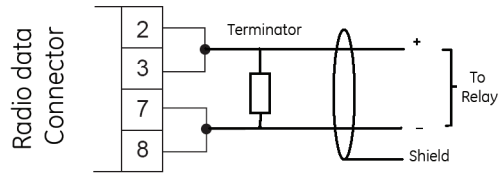


Figure 21.

5.0 Security of MDS Spread Spectrum Radios

For protective relaying applications engineers there are three areas of concern:

- Freedom from mis-operation
- Data corruption and
- Cyber Security

The robust nature of modern data communications technology implemented within the radios and the error checking of the protocols ensure end to end error free transmission. This negates the possibility of mis-operation and data corruption. The increasing focus on Cyber Security has led MDS to ensure the radios are compatible with current security software and standards such that the radios fit into the customers' cyber security just as any other compliant IT devices would. The common cyber security concerns and issues addressed by MDS radios are:

- Protection of privacy: prevent data from being reviewed by people who are not authorized to do so.
- Protection from unauthorized access from the network. Prevent people from accessing the network who shouldn't have access.

- Protection against or mitigation of denial of service attacks: A denial of service attack is to make the network not do what it is supposed to do. Typical strategies include redirection of traffic, overloading the network with messages or control commands. The next few paragraphs describe how MDS addresses these issues within the design of the radio equipment.

5.1 Protection of Privacy:

Spread spectrum technology was developed during World War II and used subsequently by the military because of its ability to reject jamming and the difficulty it presents to the enemy attempting to intercept its transmissions. At the RF level or physical layer a signal with the information is being emitted from the radio's antenna. The first concern is that someone can intercept this information and gain access. The term "AirSnort" refers to a device used by hackers located close to the facility, that receives the RF signal. Upon successful reception of the signal the hacker would then use typical encryption cracking software to gain access to the network. MDS radios are not interoperable with WIFI RF signals and so WIFI hardware cannot be used as an "AirSnort", making MDS unlicensed spread spectrum radios inherently secure against this type of attack. The RF or physical layer is MDS proprietary. If the hacker was able to obtain a MDS radio, the radio's design is such that it cannot be put into a promiscuous mode such as a laptop WIFI card can. Lets explain this a little further: There are no software divers that reside in an external device such as a computer to make the MDS radios work, as is the case with WIFI. Therefore, hackers cannot get access to the data stream as they would be able to do with WIFI technology. This fact also aids in the protection against a denial of service. Let's assume that the hacker has obtained or stolen MDS radio in an attempt to use it to eavesdrop and intercept messages. The MDS radios support both the AES-128 and RC4 encryption standard. Both of these encryption standards use a key. This key is required to decrypt the data. Unlike earlier encryption technology the key isn't static, rather it is rotated with other keys after a short period of operation. Both of these encryption techniques are industry standard for cyber security. The stolen radio is useless without the key.

5.2. Protection From Unauthorized Access:

This next level of security assumes that a hacker is already connected to the network using a stolen radio (This is a big assumption). To prevent break-ins in the case of this unlikely event the network uses a method of authentication before the radio is allowed access to the network. There are several cyber security authentication standards. For standard IT equipment such as routers, switches, and WIFI, the authentication standard that applies is 802.1x RADIUS authentication. Larger organizations that choose to implement authentication will implement 802.1x RADIUS. 802.1x RADIUS is quite complex and requires servers, so smaller organizations may not have chosen to implement authentication due to the company's size, cost of implementation and the likelihood that unobserved access to the network could be obtained. If 802.1x RADIUS has been implemented, MDS radio's comply with this standard. The same radios will also work without 802.1x RADIUS and have local authentication that will provide the user with a high level of security.

5.3 Protection From Denial of Service Attacks:

There are many different attacks, including an attempt to redirect traffic. The predominant strategy against denial of service attacks is to prevent unauthorized people from configuring the radios. To protect against dictionary attacks, which a hacker may try to use to break the password, MDS radios have a feature were after three login failures the transceiver ignores login requests for 5 minutes.

There are network configuration tools that allow the network administrator the ability to configure the entire network from one location using telnet sessions as opposed to configuring each managed device, such as a switch, locally. If there exists, in the network, unprotected remote access points a hacker could use an Ethernet packet sniffer such as Ethereal and see the telnet sessions and gain the passwords which would allow remote access to the radios. With this information the hacker could reconfigure radios remotely through this interface and enter bad parameters that could potentially bring the network down. This is a concern for any network whether it uses radios as part of the network medium or not To counter this attack, larger organizations may insist upon implementing remote login to network managed devices with SSH management or HTTPS. The SSH or HTTPS management standard is basically an encrypted telnet for IT equipment configuration. This would prevent someone who is monitoring the network with a sniffer from an unsecured access point from seeing the data within the telnet session.

In addition, MDS radios are compliant with SNMP version 3 which may be implemented on larger systems. SNMP version 3 is an interoperable standards-based protocol for network management. SNMPv3 provides secure access to managed devices by a combination of authenticating and encrypting packets over the network. The security features provided in SNMPv3 are:

- Message integrity—Ensuring that a packet has not been tampered with in-transit.
- Authentication—Determining the message is from a valid source.
- Encryption—Scrambling the contents of a packet to prevent it from being seen by an unauthorized source.

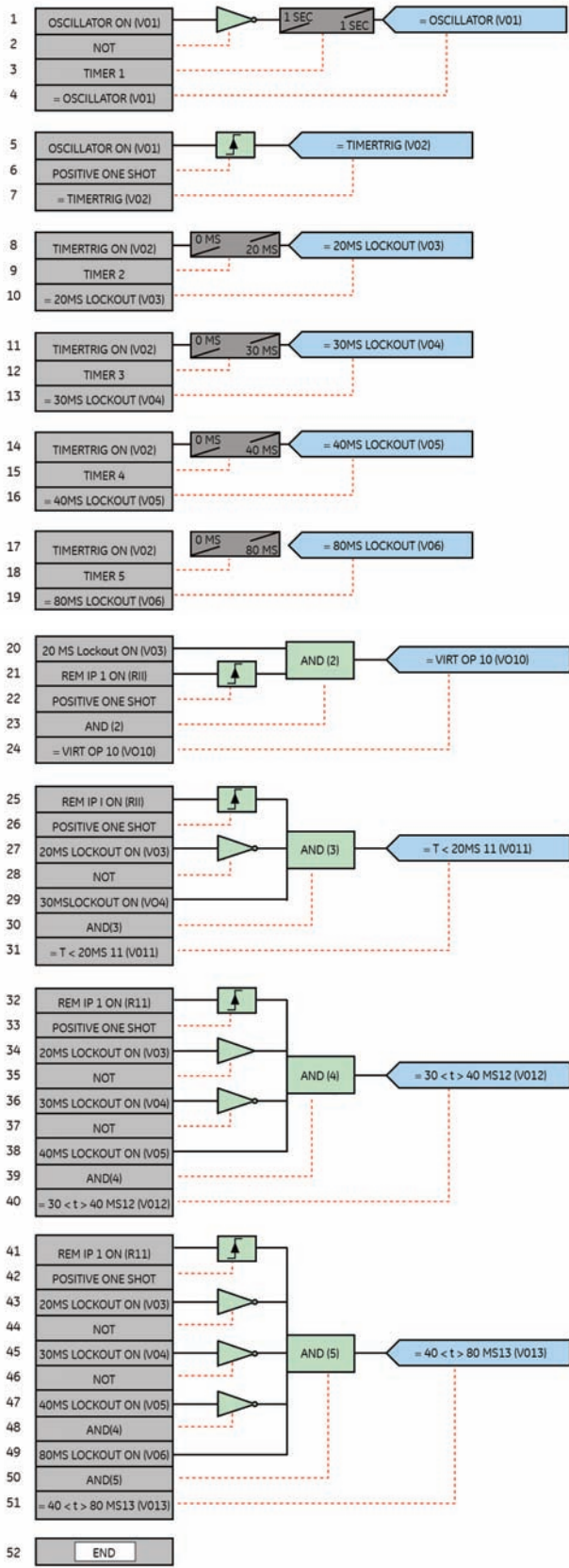


Figure 22.

6.0 Latency FlexLogic for IEC61850 GSSE Flexlogic Operation:

This section outlines the FlexLogic for iNet-II 900 application in section 2.2. In Figure 22, FlexLogic Timer #1 acts as a 2 second oscillator with a 50:50 duty cycle that initiates each transmission as follows. Every off to on transition of Virtual Output #1 changes the status of User Remote Output #1. Each change in User Remote Output #1's status causes UR #1 to transmit a GSSE message containing the status of all of the Remote Outputs including User Remote output#1. UR#2 is configured to store the status of User Remote Output #1 in its local Remote Input#1 and it's User Remote Output #1. The change in status of UR#2's Remote Output #1 will initiate the transmission of a GSSE message from UR#2. UR#1 will receive this transmission. As seen in Figure 23, depending on the round trip time UR#2's Remote Output#1 will increment one of the counters 1 through 4 in UR#1 which corresponds to the round trip time being less then 20, 30, 40 or 80 milliseconds respectively. Counter#5 is used to count the total number of messages sent. If no messages have been lost or have a round trip time greater then 80 milliseconds, the total of counters 1 through 4 should equal the accumulated count in counter #5.

Setting	Parameter
Digital Counter 1 Function	Enabled
Digital Counter 1 Name	Trip < 20ms
Digital Counter 1 Units	
Digital Counter 1 Preset	0
Digital Counter 1 Compare	0
Digital Counter 1 Up	Vrt Op 10 On (V010)
Digital Counter 1 Down	OFF
Digital Counter 1 Block	OFF
Digital Counter 1 Set To Preset	OFF
Digital Counter 1 Reset	CONTROL PUSHBUTTON 1 ON
Digital Counter 1 Freeze/Reset	OFF
Digital Counter 1 Freeze/Count	OFF
Digital Counter 2 Function	Enabled
Digital Counter 2 Name	Trip < 30ms
Digital Counter 2 Units	
Digital Counter 2 Preset	0
Digital Counter 2 Compare	0
Digital Counter 2 Up	T<20ms 11 On (V011)
Digital Counter 2 Down	OFF
Digital Counter 2 Block	OFF
Digital Counter 2 Set to Preset	OFF
Digital Counter 2 Reset	CONTROL PUSHBUTTON 1 ON
Digital Counter 2 Freeze/Reset	OFF
Digital Counter 3 Function	Enabled
Digital Counter 3 Name	Trip < 40ms
Digital Counter 3 Units	
Digital Counter 3 Preset	0
Digital Counter 3 Compare	0
Digital Counter 3 Up	30 <T>40ms 12 On (V012)
Digital Counter 3 Down	OFF
Digital Counter 3 Block	OFF
Digital Counter 3 Set To Preset	OFF
Digital Counter 3 Reset	CONTROL PUSHBUTTON 1 ON
Digital Counter 3 Freeze/reset	OFF
Digital Counter 3 Freeze/Count	OFF
Digital Counter 4 Function	Enabled
Digital Counter 4 Name	Trip < 80ms
Digital Counter 4 Units	
Digital Counter 4 Preset	0
Digital Counter 4 Compare	0
Digital Counter 4 Up	40 <T> 80ms 13 On (V013)
Digital Counter 4 Down	OFF
Digital Counter 4 Block	OFF
Digital Counter 4 Set To Preset	OFF
Digital Counter 4 Reset	CONTROL PUSHBUTTON 1 ON
Digital Counter 4 Freeze/Reset	OFF

Figure 23.

Protection Basics: Introduction to Symmetrical Components

1. Introduction

Symmetrical components is the name given to a methodology, which was discovered in 1913 by Charles Legeyt Fortescue who later presented a paper on his findings entitled, "Method of Symmetrical Co-ordinates Applied to the Solution of Polyphase Networks." Fortescue demonstrated that any set of unbalanced three-phase quantities could be expressed as the sum of three symmetrical sets of balanced phasors. Using this tool, unbalanced system conditions, like those caused by common fault types may be visualized and analyzed. Additionally, most microprocessor-based relays operate from symmetrical component quantities and so the importance of a good understanding of this tool is self-evident.

2. Positive, Negative and Zero Sequence Components

According to Fortescue's methodology, there are three sets of independent components in a three-phase system: positive, negative and zero for both current and voltage. Positive sequence voltages (Figure 1) are supplied by generators within the system and are always present. A second set of balanced phasors are also equal in magnitude and displaced 120 degrees apart, but display a counter-clockwise rotation sequence of A-C-B (Figure 2), which represents a negative sequence. The final set of balanced phasors is equal in magnitude and in phase with each other, however since there is no rotation sequence (Figure 3) this is known as a zero sequence.

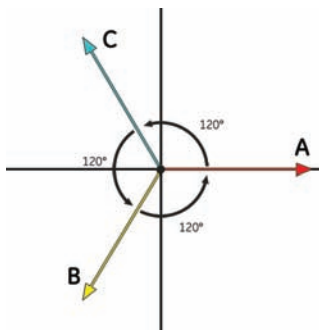


Figure 1.
Positive Sequence Components;
A-B-C

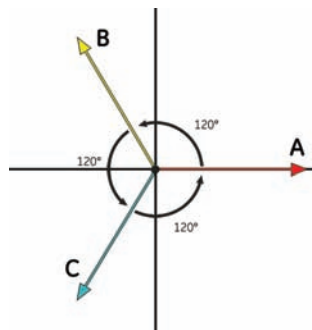


Figure 2.
Negative Sequence Components;
A-C-B

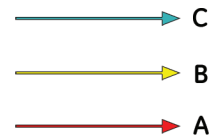


Figure 3.
Zero Sequence Components

3. Introduction to Symmetrical Components

The symmetrical components can be used to determine any unbalanced current or voltage (I_a, I_b, I_c or V_a, V_b, V_c which reference unbalanced line-to-neutral phasors) as follows:

$$\begin{aligned} I_a &= I_1 + I_2 + I_0 & V_a &= V_1 + V_2 + V_0 \\ I_b &= a^2 I_1 + a I_2 + I_0 & V_b &= a^2 V_1 + a V_2 + V_0 \\ I_c &= a I_1 + a^2 I_2 + I_0 & V_c &= a V_1 + a^2 V_2 + V_0 \end{aligned}$$

The sequence currents or voltages from a three-phase unbalanced set can be calculated using the following equations:

Zero Sequence Component:

$$I_0 = \frac{1}{3} (I_a + I_b + I_c) \quad V_0 = \frac{1}{3} (V_a + V_b + V_c)$$

Positive Sequence Component:

$$I_1 = \frac{1}{3} (I_a + a I_b + a^2 I_c) \quad V_1 = \frac{1}{3} (V_a + a V_b + a^2 V_c)$$

Negative Sequence Component:

$$I_2 = \frac{1}{3} (I_a + a^2 I_b + a I_c) \quad V_2 = \frac{1}{3} (V_a + a^2 V_b + a V_c)$$

The independence of the symmetrical components and their resultant summation follow the principle of superposition, which is the basis for its practical usage in protective relaying.

Before proceeding further, a mathematical explanation of the "a" operator is required. Within Fortescue's formulas, the "a" operator shifts a vector by an angle of 120 degrees counter-clockwise, and the "a²" operator performs a 240 degrees counter-clockwise phase shift. According to Fortescue, a balanced system will have only positive sequence currents and voltages. For example, as

shown in Figure 4, the calculation of symmetrical components in a three-phase balanced or symmetrical system results in only positive sequence voltages, $3V_1$. Similarly, the currents also have equal magnitudes and phase angles of 120 degrees apart, which would produce a result of only positive sequence and no negative or zero sequence currents for a balanced system.

For unbalanced systems, such as an open-phase there will be positive, negative and possibly zero-sequence currents. Referring to the open-phase example in Figure 5, it can be seen that the calculation of the symmetrical components results in positive, negative and zero sequence currents of $3I_1$, $3I_2$, and $3I_0$. However, since the voltages are balanced in magnitude and phase angle, the result would be the same as the balanced system in Figure 4, which produces only positive sequence voltage.

Similarly for a single phase to ground fault as shown in Figure 6, there will be positive, negative and zero sequence currents ($3I_1$, $3I_2$, and $3I_0$) and voltages ($3V_1$, $3V_2$, and $3V_0$).

4. Summary

Under a no fault condition, the power system is considered to be essentially a symmetrical system and therefore only positive sequence currents and voltages exist. At the time of a fault, positive, negative and possibly zero sequence currents and voltages exist. Using real world phase voltages and currents along with Fortescue's formulas, all positive, negative and zero sequence currents can be calculated. Protective relays use these sequence components along with phase current and/or voltage data as the input to protective elements.

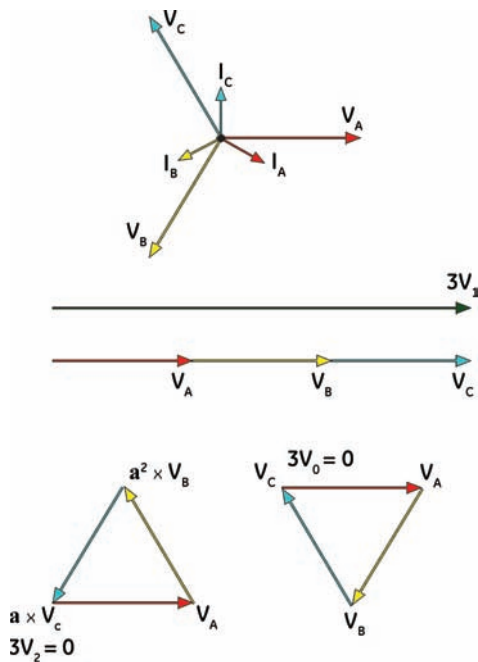


Figure 4.
Three-Phase Balanced / Symmetrical System

5. References

- [1] J. L. Blackburn, T. J. Domin, 2007, "Protective Relaying, Principles and Applications, Third Edition," Taylor & Francis Group, LLC, Boca Raton, FL, pp.75-80
- [2] GE Publication, "Fundamentals of Modern Protective Relaying," Instruction Manual, Markham, Ontario, 2007

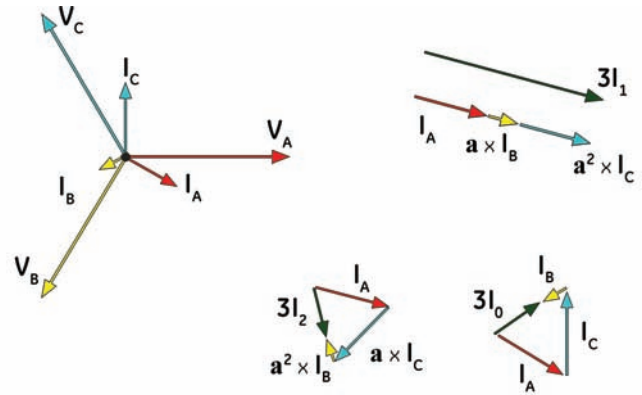


Figure 5.
Open-Phase Unbalanced / Non-Symmetrical System

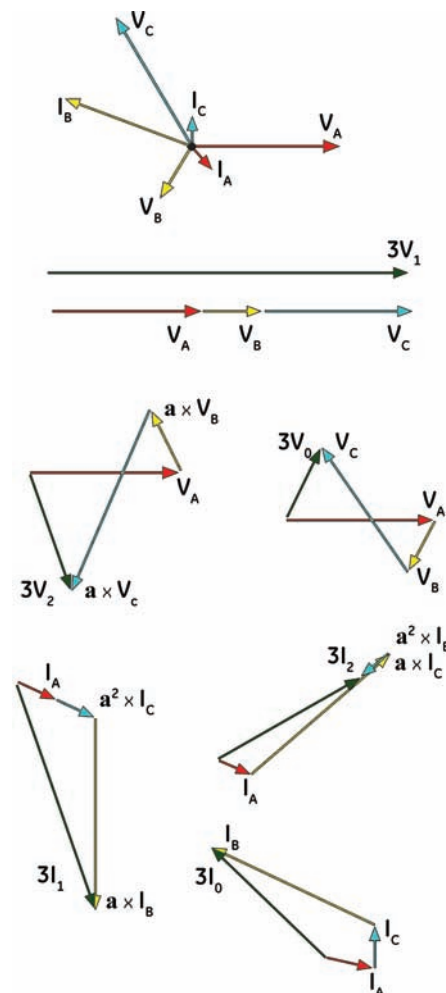


Figure 6.
Single Phase-Ground Fault Unbalanced / Non-Symmetrical System

Remote control

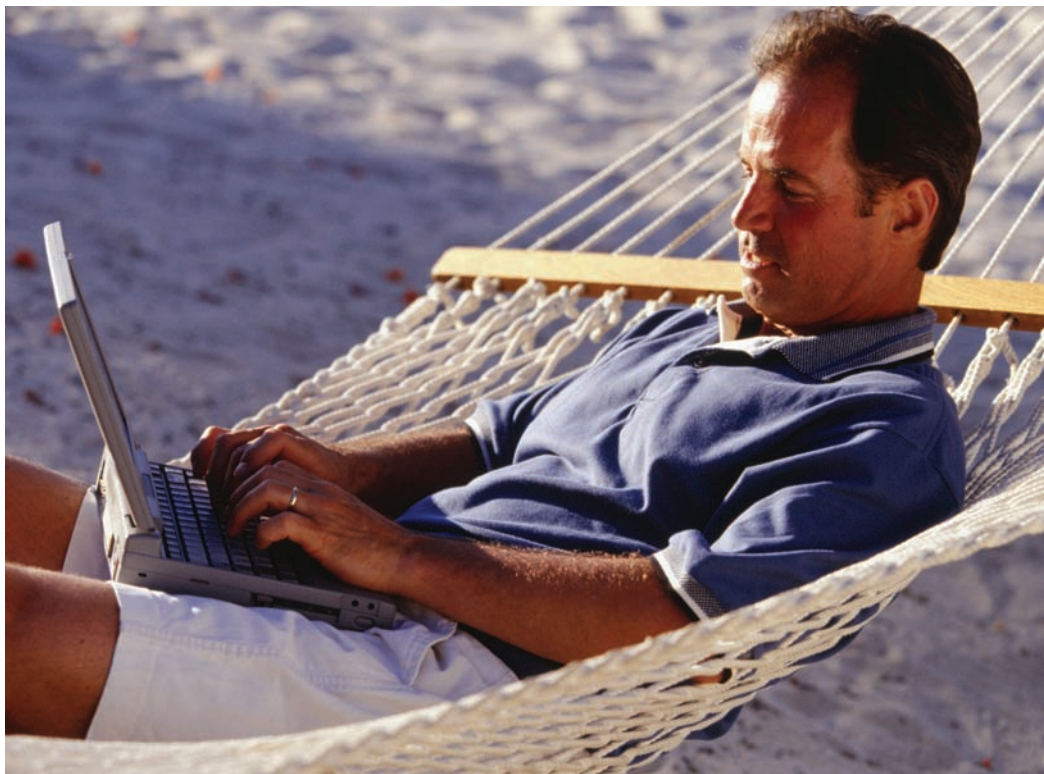
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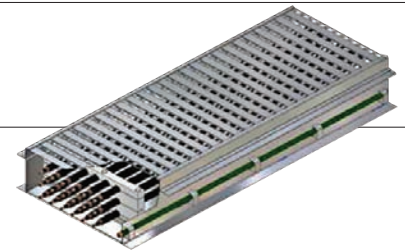
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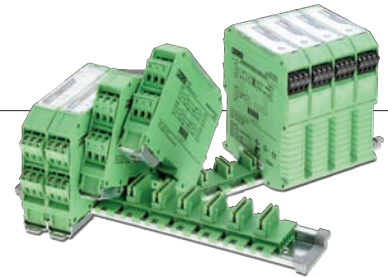
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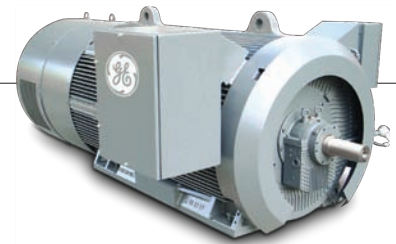
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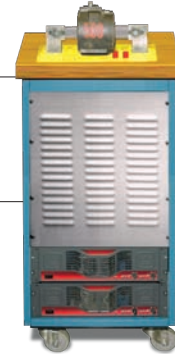
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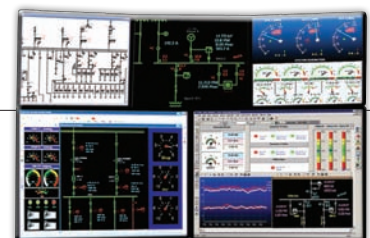
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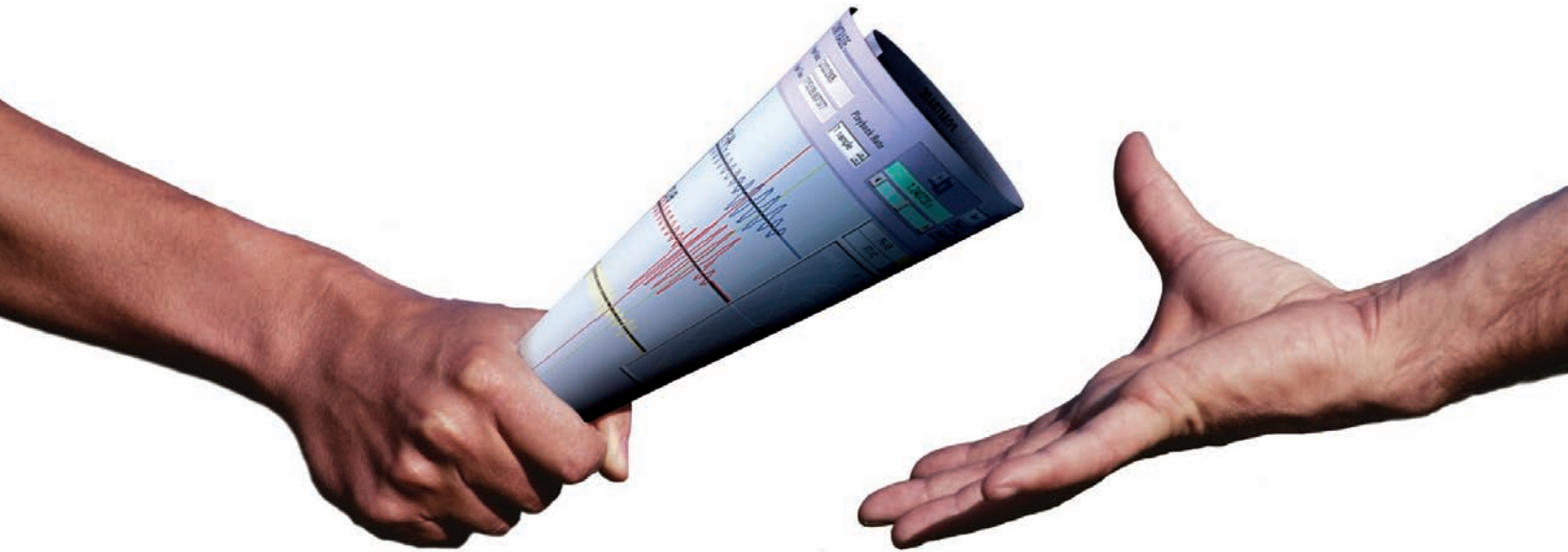
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www.pamerindo.com/2007/electric/ele07exh.htm

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